

512M-BIT 3V SPI-NOR MCP FLASH MEMORY

Descriptions

The H7A5FM26B7CX (2 X 256M-bit) Serial MCP Flash offers the highest memory density for the low pin-count package, as well as Concurrent Operations in Serial Flash memory for the first time. It is ideal for small form factor system designs, and applications that demand high Program/Erase data throughput.

The H7A5FM26B7CX introduces a new “Software Die Select (C2h)” instruction, and a factory assigned “Die ID#” for each stacked die. Each H7A5EM die can be accessed independently even though the interface is shared. The stack feature only allows a single die to be Active and have control of the SPI interface at any given time to avoid bus contention.

The H7A5FM26B7CX maintains all the SPI Flash features and functions, with the support for standard SPI (Serial Peripheral Interface), Dual I/O SPI, and Quad I/O SPI read operations through the shared SPI interface: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2, and I/O3.

Each H7A5EM memory array is organized into 131,072 programmable pages of 256-Byte each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

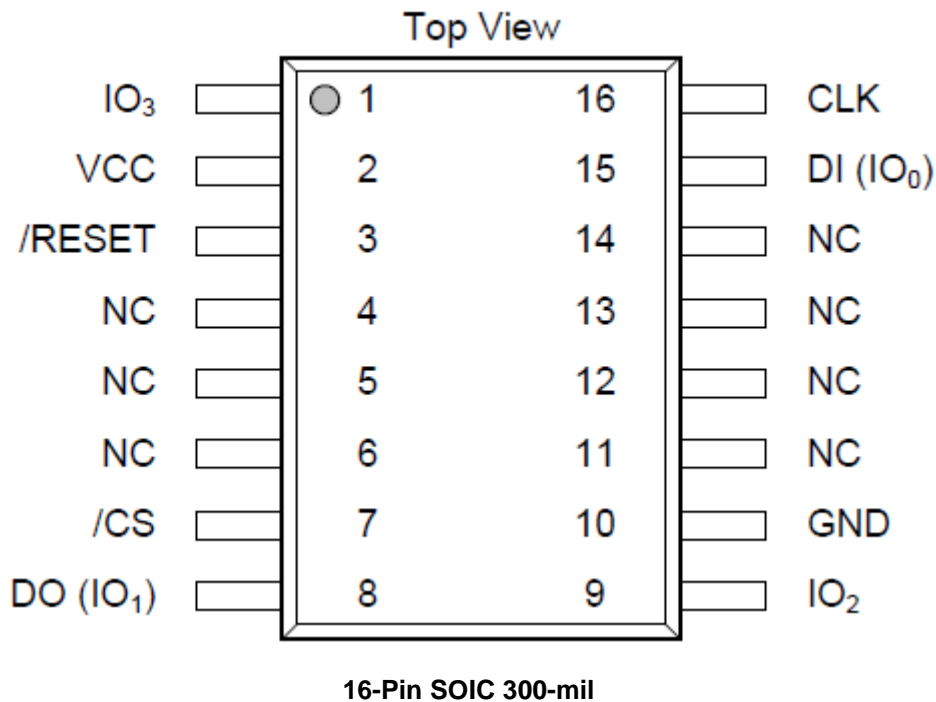
Features

- **Basic Features**
 - Density : 2X256M-bit / 2X32M-byte
 - Standard SPI: CLK, /CS, DI, DO
 - Dual SPI: CLK, /CS, IO0, IO1
 - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
 - 3 or 4-Byte Addressing Mode
 - Software Die Select (C2h)
 - Software & Hardware Reset
- **High Performance Serial NOR Flash**
 - 104MHz Standard/Dual/Quad SPI clocks
 - 208/416MHz equivalent Dual/Quad SPI
 - 50MB/s continuous data transfer rate
 - Min. 100K Program-Erase cycles per sector
 - More than 20-year data retention
- **Efficient “Concurrent Operations”**
 - Independent single die access
 - Allows “Read while Program/Erase”
 - Allows “Multi Die Program/Erase”
 - Improves Program/Erase throughput
 - Reduces Suspend/Resume activities
- **Low Power, Wide Temperature Range**
 - Single 2.7 to 3.6V supply
 - 4mA active current, <20µA standby current
- **Flexible Architecture with 4KB sectors**
 - Uniform Sector/Block Erase (4K/32K/64K-Byte)
 - Program 1 to 256 byte per programmable page
 - Erase/Program Suspend & Resume
- **Advanced Security Features**
 - Power Supply Lock-Down and OTP protection
 - Top/Bottom, Complement array protection
 - Individual Block/Sector array protection
 - 64-Bit Unique ID for individual die
 - Discoverable Parameters (SFDP) Register
 - 3X256-Bytes Security Registers with OTP locks
 - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
 - 16-Pin SOIC 300-mil

Ordering Information

Part No	Density	Package	Grade
H7A5FM26B7CX	512M-bit/64M-byte	16-Pin SOIC 300-mil	Commercial

Pin Configuration



Pin Description (Simplified)

16-Pin SOIC, 300-mil			
Pin NO.	Pin Name	I/O	Function
1	IO3	Input / Output	Data Input Output 3
2	VCC		Power Supply
3	/RESET	Input	Reset Input
4-6,11-14	N/C		No Connect
7	/CS	Input	Chip Select Input
8	DO (IO1)	Input / Output	Data Output (Data Input Output 1)
9	IO2	Input / Output	Data Input Output 2
10	GND		Ground
15	DI (IO0)	Input / Output	Data Input (Data Input Output 0)
16	CLK	Input	Serial Clock Input

Note1: IO0 and IO1 are used for Standard and Dual SPI instructions and IO0 – IO3 are used for Quad SPI instructions .

Note2: The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system.

Absolute Maximum Rating

Item	Symbol	Conditions	Rating	Unit
Supply Voltage	V _{CC}		-0.6 to VCC+4.6	V
Voltage Applied to Any Pin	V _{IO}	Relative to Ground	-0.6 to VCC+0.4	V
Transient Voltage on any Pin	V _{IOT}	<20nS Transient Relative to Ground	- 2.0V to VCC+2.0V	V
Storage Temperature	T _{STG}		-65 ~ 150	°C
Lead Temperature	T _{LEAD}		Notes2	°C
Electrostatic Discharge Voltage	V _{ESD}	Human Body Model(3)	- 2000 to +2000	V

Note 1: This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

Note 2: Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.

Note 3: JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms)..

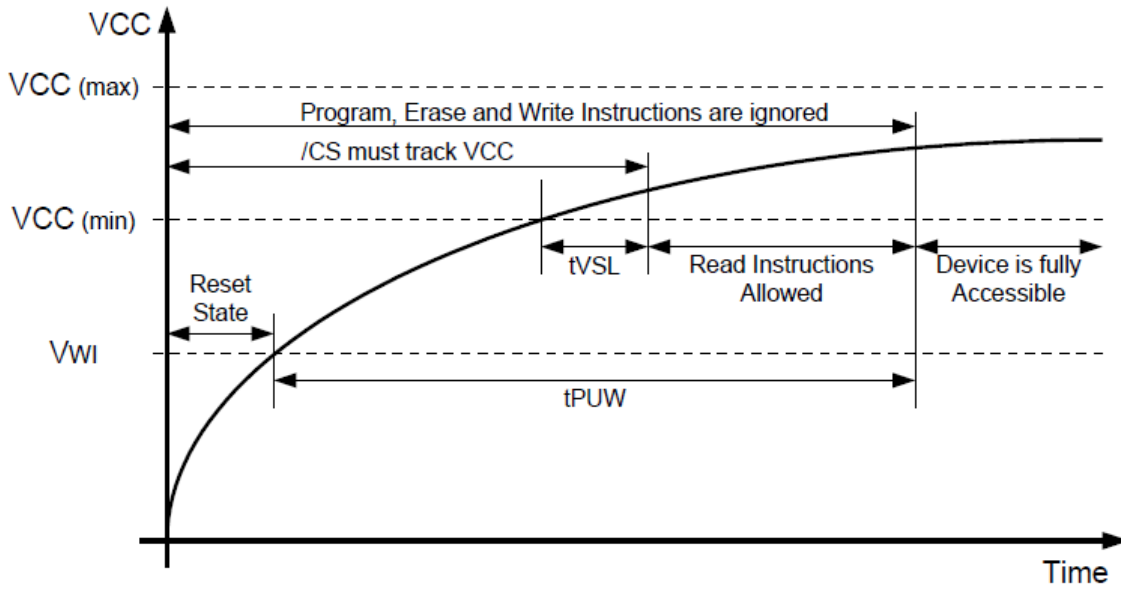
Operating Ranges

Parameter	Symbol	Conditions	Spec.		Unit
			Min.	Max.	
Supply Voltage	V _{CC}	FR=104MHz,fR=50MHz	2.7	3.6	V
Ambient Temperature, Operating	T _a	Commercial	0	70	°C

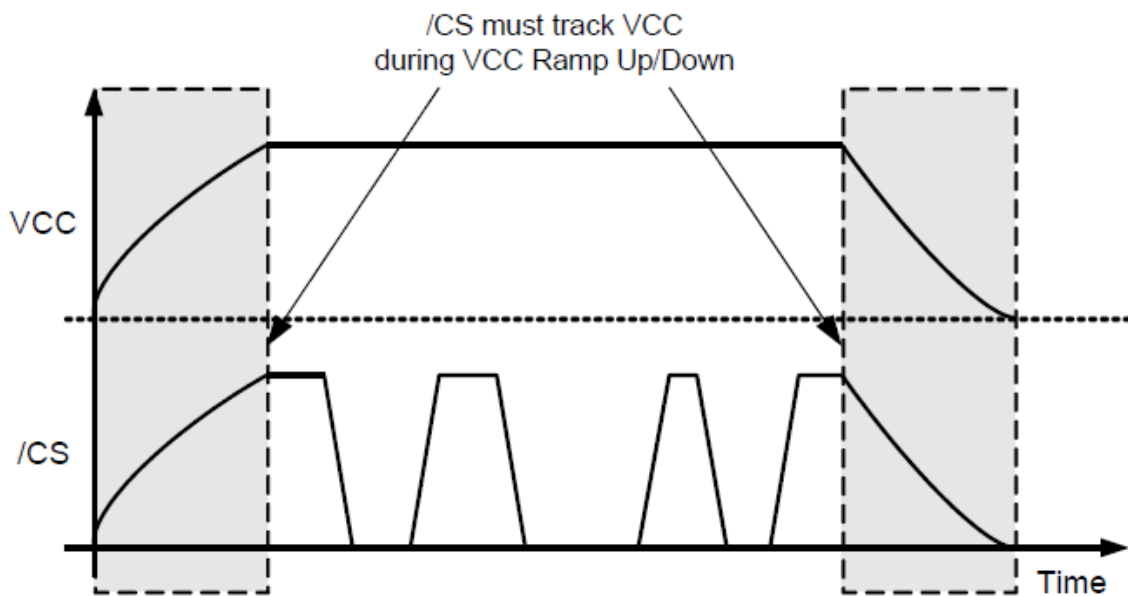
Note 1: VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

Device Power-up / Power-down Timing Requirement

Parameter	Symbol	Spec.		Unit
		Min.	Max.	
VCC (min) to /CS Low	tVSL	20		us
Time Delay Before Write Instruction	tPUW	5		ms
Write Inhibit Threshold Voltage	VWI	1.0	2.0	V



Power-up Timing and Voltage Levels



Power-up, Power-Down Requirement

DC Characteristics

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	
Input Capacitance	CIN(1)	VIN=0V(1)			6	pF
Output Capacitance	COUT(1)	VOUT=0V(1)			8	pF
Input Leakage	ILI				+/-4	uA
I/O Leakage	ILO				+/-4	uA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		20	120	uA
Current Read Data / Dual /Quad 50MHz	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open			20	mA
Current Read Data / Dual /Quad 80MHz	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open			25	mA
Current Read Data / Dual /Quad 104MHz	ICC3	C = 0.1 VCC / 0.9 VCC DO = Open			30	mA
Current Write Status Register	ICC4	/CS = VCC		20	25	mA
Current Page Program	ICC5	/CS = VCC		20	25	mA
Current Sector/Block Erase	ICC6	/CS = VCC		20	25	mA
Current Chip Erase	ICC7	/CS = VCC		20	25	mA
Input Low Voltage	VIL		-0.5		0.3 x Vcc	V
Input High Voltage	VIH		0.7 x Vcc		Vcc+0.4	V
Output Low Voltage	VOL	IOL=100uA			0.2	V
Output High Voltage	VOH	IOH = -100 μA	Vcc-0.2			V

Note 1: Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

AC Measurement Conditions

Parameter	Symbol	Spec.		Unit
		MIN	Max	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR,TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V

AC Electrical Characteristics

Description	Symbol	ALT	Spec.			Unit
			MIN	TYP	Max	
Clock frequency for all other instructions	FR	fC1	D.C.		104	Mhz
Clock frequency for Read Data instruction (03h)	fR		D.C.		50	Mhz
Clock High, Low Time for all instructions except for Read Data (03h)	tCLH,tCLL(1)		4			ns
Clock High, Low Time for Read Data (03h) instruction	tCRLH, tCRLL(1)		8			ns
Clock Rise Time peak to peak	tCLCH(2)		0.1			V/ns
Clock Fall Time peak to peak	tCHCL(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/CS Active Hold Time relative to CLK	tCHSH		3			ns
/CS Not Active Setup Time relative to CLK	tSHCH		3			ns
/CS Deselect Time (During Read)	tSHSL1	tCSH	10			ns
/CS Deselect Time (During Erase or Program or Write)	tSHSL2	tCSH	50			ns
Output Disable Time	tSHQZ(2)	tDIS			7	ns
Clock Low to Output Valid	tCLQV	tV			7	ns
Output Hold Time	tCLQX	tHO	1.5			ns
/CS High to Standby Mode without ID Read	tRES1(2)				3	us
/CS High to Standby Mode with ID Read	tRES2(2)				1.8	us
/CS High to next Instruction after Suspend	tSUS(2)				20	us
/CS High to next Instruction after Reset	tRST(2)				30	us
/RESET pin Low period to reset the device	tRESET(2)		1			us
Status Register Write Time	tw			10	15	ms
Page Program Time	tPP			0.7	3	ms
Sector Erase Time (4KB)	tSE			50	400	ms
Block Erase Time (32KB)	tBE1			120	1600	ms
Block Erase Time (64KB)	tBE2			150	2000	ms
Single Die Erase Time (256Mb) Concurrent Dual-Die Erase Time (2 x 256Mb)	tCE			80	400	s

Note: 1. Clock high + Clock low must be less than or equal to $1/f_C$.

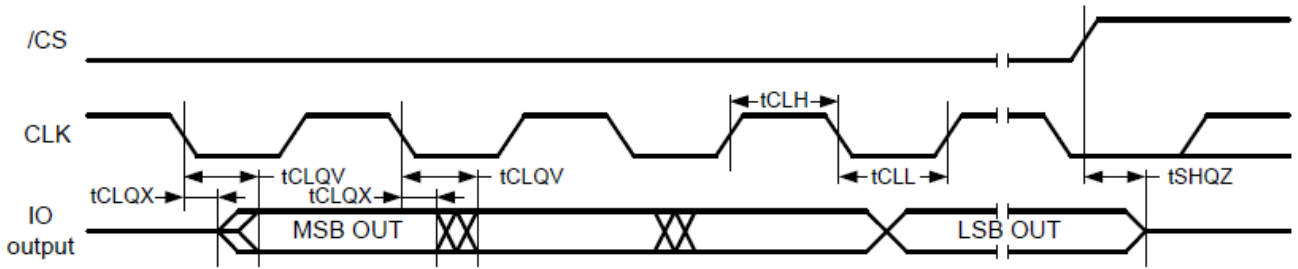
Note: 2. Value guaranteed by design and/or characterization, not 100% tested in production.

Note: 3. It is possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.

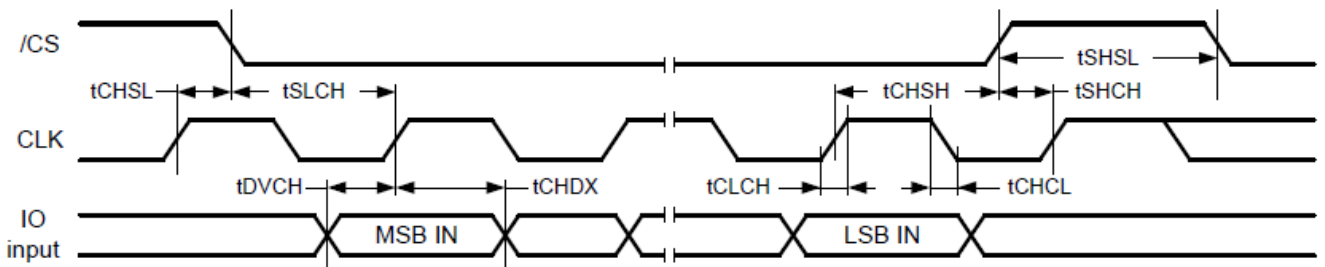
Note: 4. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

Note: 5. 4-bytes address alignment for Quad Read, start address from [A1,A0]=(0,0).

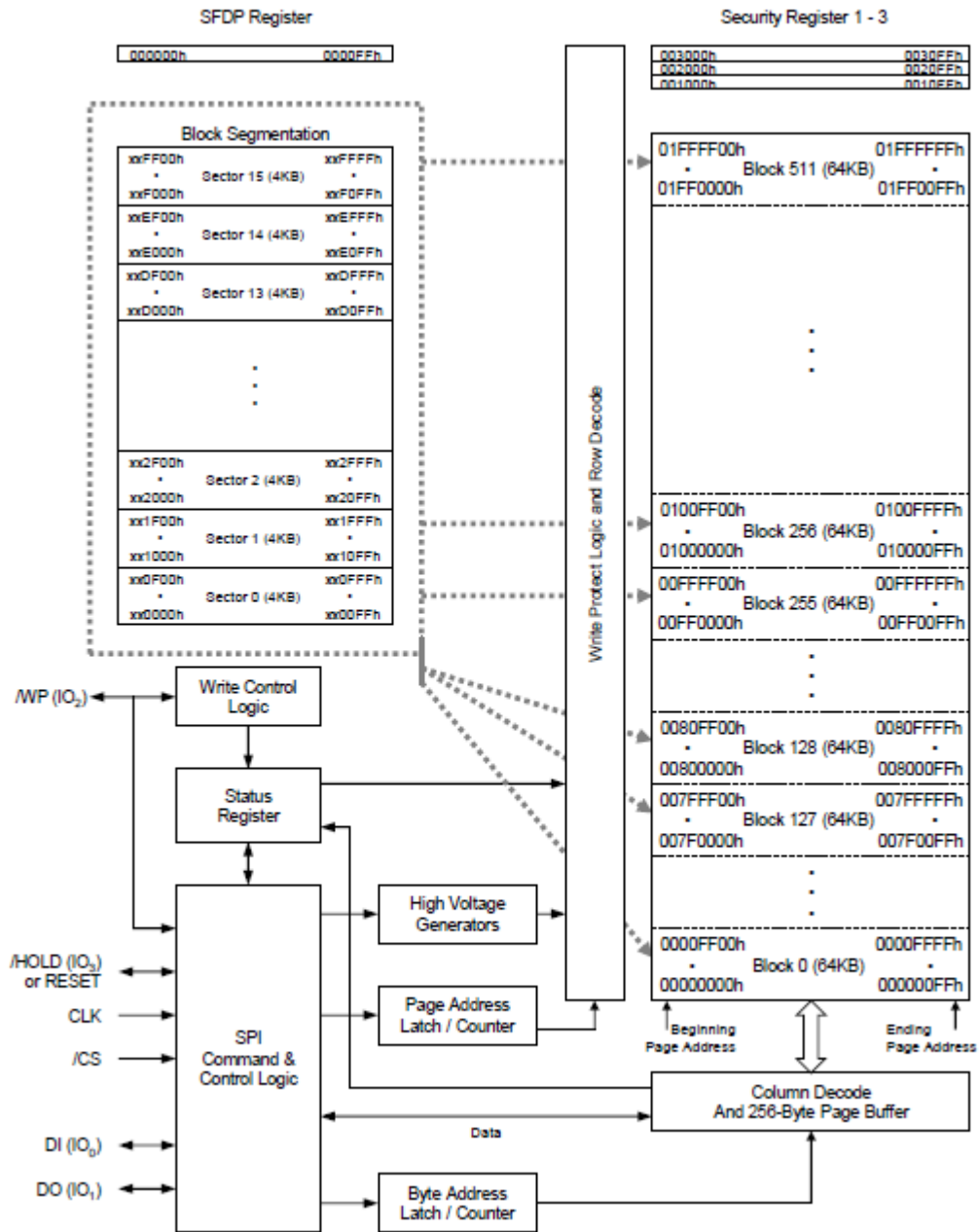
Serial Output Timing



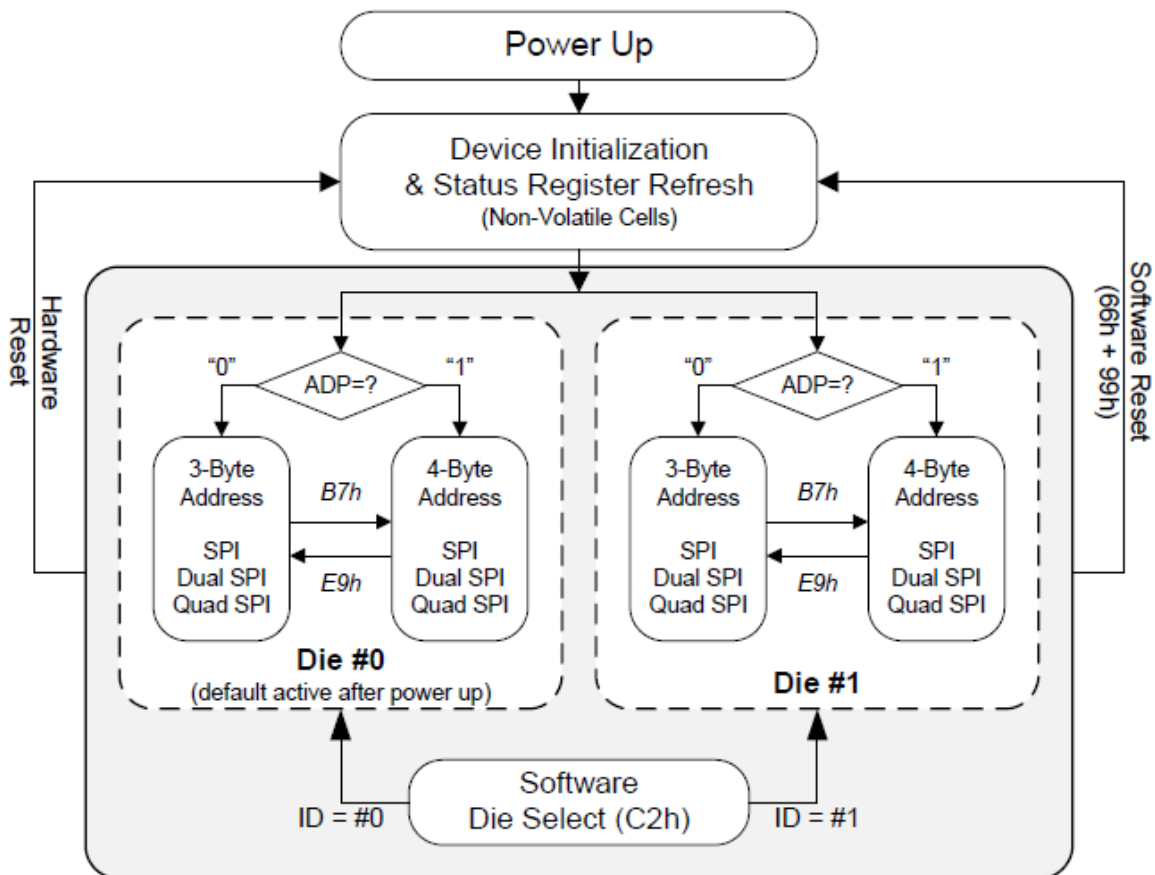
Serial Input Timing



Single Die Block Diagram



Device Operations



Stacked Die Operations

Once the device is power on, Die #0 will be active and have control of the SPI bus. “Software Die Select (C2h)” instruction followed by the 8-bit Die ID can be used to select the active die. The active die is available to accept any instruction issued by the controller and perform specific operations. The inactive/idle die does not accept any other instructions except the “Software Die Select (C2h)” and “Software Reset (66h + 99h)”. However, the inactive/idle die can still perform internal Program/Erase operation which was initiated when the die was active. Therefore, “Read (on Active die) while Program/Erase (on Idle die)” and “Multi-die Program/Erase (both Active & Idle dies)” concurrent operations are feasible. “Software Die Select (C2h)” instruction will only change the active/idle status of the stacked dies, and it will not interrupt any on-going Program/Erase operations

Standard SPI Instructions

The H7A5FM26B7CX is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

Dual & Quad SPI Instructions

The H7A5FM26B7CX supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1. The H7A5FM26B7CX also supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. When using Quad SPI instructions, the DI and DO pins become bidirectional IO0 and IO1, with the additional I/O pins: IO2, IO3.

3-Byte / 4-Byte Address Modes

The H7A5FM26B7CX provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The Extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the H7A5FM26B7CX can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0. ADP bit cannot be used to switch the address mode during normal operation.

To switch between 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

H7A5FM26B7CX also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set Tables for details.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, each stacked die within H7A5FM26B7CX provides several means to protect the data from inadvertent writes independently.

- ◆ Device resets when VCC is below threshold
- ◆ Time delay write disable after Power-up
- ◆ Write enable/disable instructions and automatic write disable after erase or program
- ◆ Software write protection using Status Registers
- ◆ Lock Down write protection for Status Register until the next power-up
- ◆ Additional Individual Block/Sector Locks for array protection
- ◆ One Time Program (OTP) write protection for Array and Security Registers using Status Register

Upon power-up or at power-down, each stacked die will maintain a reset condition while VCC is below the threshold value of VWI,. While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached, and it must also track the VCC supply level at powerdown to prevent

adverse instruction sequence. If needed, a pull-up resistor on /CS pin can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Lock (SRL) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. See Status Register section for further information.

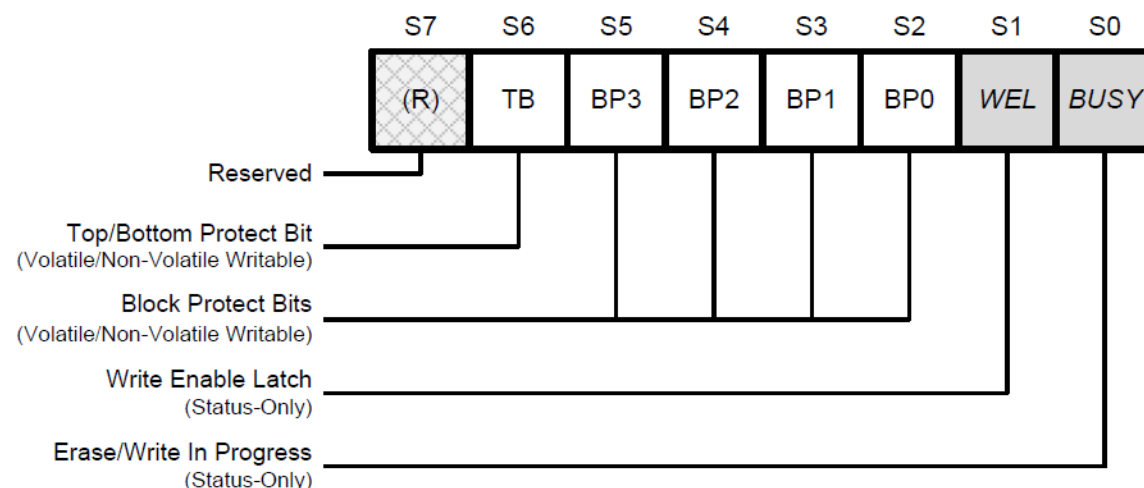
Each stacked die also provides another Write Protect method using the Individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 510 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program instructions issued to the corresponding sector or block will be ignored. When the device is powered on, all Individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An "Individual Block Unlock (39h)" instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, TB, BP[3:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write protection.

Status and Configuration Registers

Three Status and Configuration Registers are provided for H7A5FM26B7CX. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Security Register OTP locks, output driver strength and power-up Address Mode. Write access to the Status Registers is controlled by the state of the volatile/non-volatile Status Register Lock bit (SRL), and the Write Enable instruction.

Status Register-1



Erase/Write In Progress (BUSY) – Status Only

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions. Read Status Register instruction can always be used to poll the BUSY status during internal operations to determine if the operation has finished.

Write Enable Latch (WEL) – Status Only

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

Block Protect Bits (BP3, BP2, BP1, BP0) – Volatile/Non-Volatile Writable

The Block Protect Bits (BP3, BP2, BP1, BP0) are read/write bits in the status register (S5, S4, S3, and S2) that provide Write Protection control and status to the memory array. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

Top/Bottom Block Protect (TB) – Volatile/Non-Volatile Writable

The Top/Bottom bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRL and WEL bits.

Complement Protect (CMP) – Volatile/Non-Volatile Writable

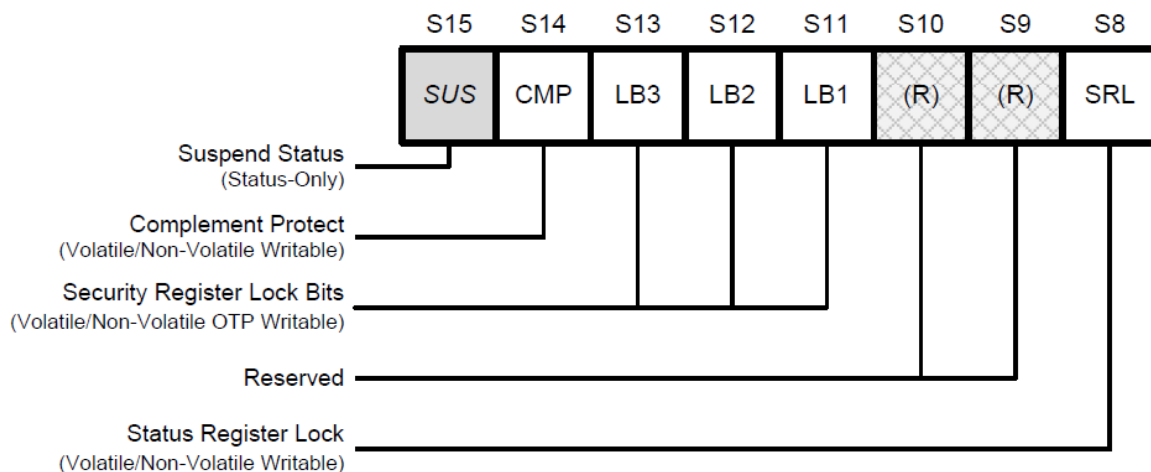
The Complement Protect bit (CMP) is a read/write bit in the status register (S14). It is used in conjunction with TB, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

Status Register Lock (SRL) – Volatile/Non-Volatile OTP Writable

The Status Register Lock bit (SRL) is a volatile/non-volatile read/write bit in the status register (S8). The SRL bit controls the method of write protection to the Status Registers: temporary Power Lock-Down or permanently One Time Program OTP.

SRL	Status Register Lock	Descriptions
0	Non-Lock	Status Registers are unlocked.
1	Power Lock-Down (Temporary/Volatile)	Status Registers are locked and cannot be written to until the next power-down, power-up cycle to reset SRL=0.
	One Time Program (Permanently/Non-Volatile)	A special instruction flow can be used to permanently OTP lock the Status Registers.

Status Register-2



Erase/Program Suspend Status (SUS) – Status Only

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

Security Register Lock Bits (LB[3:1]) – Volatile/Non-Volatile OTP Writable

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

Current Address Mode (ADS) – Status Only

The Current Address Mode bit is a read only bit in the Status Register-3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

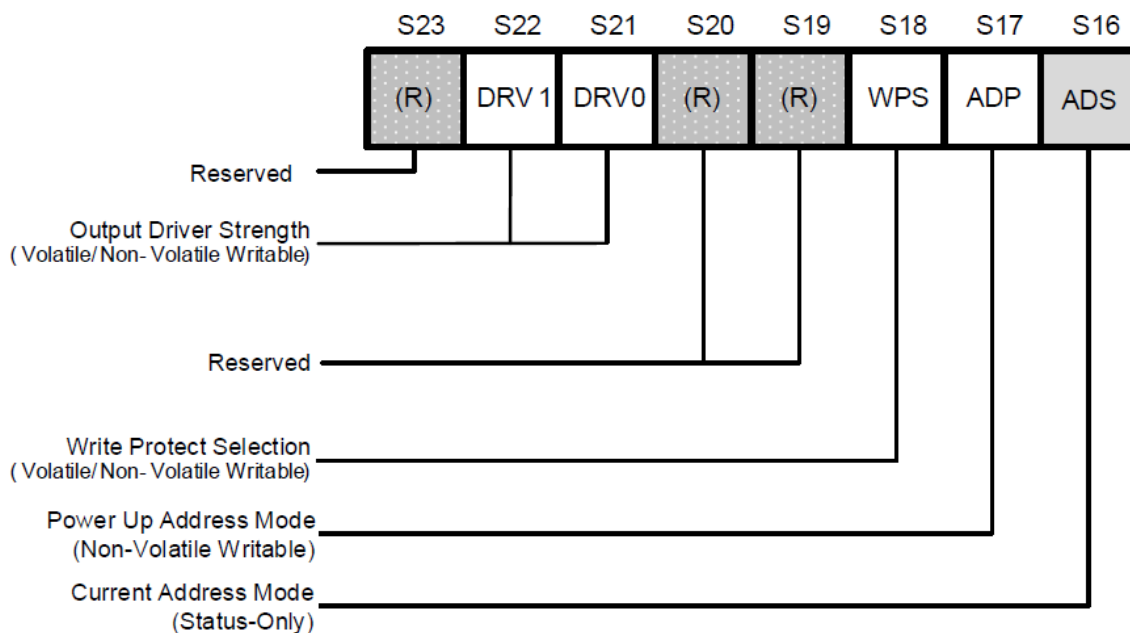
Power-Up Address Mode (ADP) – Non-Volatile Writable

The ADP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

Write Protect Selection (WPS) – Volatile/Non-Volatile Writable

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0 (factory default), the device will use the combination of CMP, TB, BP[3:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

Status Register-3



Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0,0	100%
0,1	75%
1,0	50%
1,1	25%(default)

Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0” or “1”, but there will not be any effects.

Single Die Status Register Memory Protection(WPS=0, CMP=0)

STATUS REGISTER					(256M-BIT / 32M-BYTE) MEMORY PROTECTION			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESS	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h - 01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 thru 511	01FE0000h - 01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 thru 511	01FC0000h - 01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 thru 511	01F80000h - 01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 thru 511	01F00000h - 01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 thru 511	01E00000h - 01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 thru 511	01C00000h - 01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 thru 511	01800000h - 01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 thru 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 thru 1	00000000h - 0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 thru 3	00000000h - 0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 thru 7	00000000h - 0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 thru 15	00000000h - 000FFFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 thru 31	00000000h - 001FFFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 thru 63	00000000h - 003FFFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 thru 127	00000000h - 007FFFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 thru 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	0 thru 511	00000000h - 01FFFFFFh	32MB	ALL
X	1	X	1	X	0 thru 511	00000000h - 01FFFFFFh	32MB	ALL

Note: 1. X = don't care.

Note: 2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

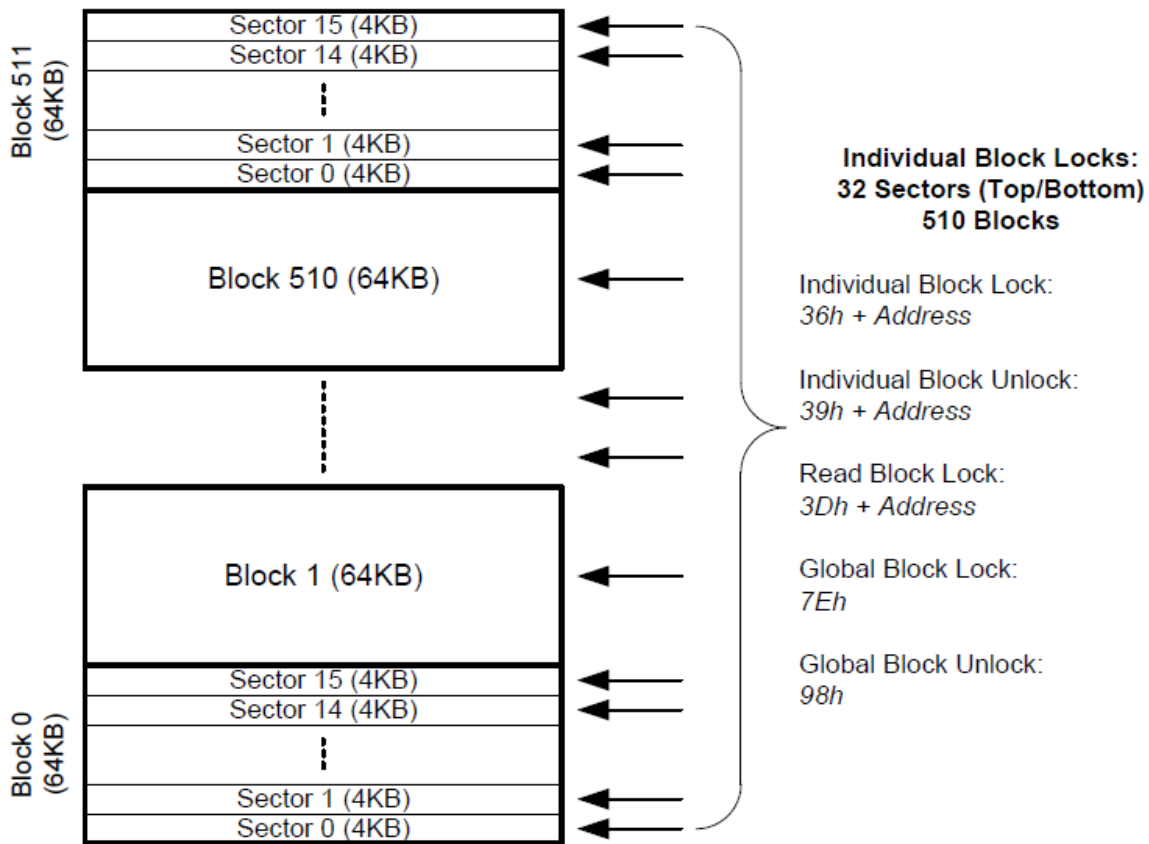
Single Die Status Register Memory Protection(WPS=0, CMP=1)

STATUS REGISTER					(256M-BIT / 32M-BYTE) MEMORY PROTECTION			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESS	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	ALL	00000000h - 01FFFFFFh	ALL	ALL
0	0	0	0	1	0 thru 510	00000000h - 01FEFFFFh	32,704KB	Lower 511/512
0	0	0	1	0	0 thru 509	00000000h - 01FDFFFFh	32,640KB	Lower 255/256
0	0	0	1	1	0 thru 507	00000000h - 01FBFFFFh	32,512KB	Lower 127/128
0	0	1	0	0	0 thru 503	00000000h - 01F7FFFFh	32,256KB	Lower 63/64
0	0	1	0	1	0 thru 495	00000000h - 01EFFFFFh	31MB	Lower 31/32
0	0	1	1	0	0 thru 479	00000000h - 01DFFFFFh	30MB	Lower 15/16
0	0	1	1	1	0 thru 447	00000000h - 01BFFFFFh	28MB	Lower 7/8
0	1	0	0	0	0 thru 383	00000000h - 017FFFFFh	24MB	Lower 3/4
0	1	0	0	1	0 thru 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
1	0	0	0	1	1 thru 511	00010000h - 01FFFFFFh	32,704KB	Upper 511/512
1	0	0	1	0	2 thru 511	00020000h - 01FFFFFFh	32,640KB	Upper 255/256
1	0	0	1	1	4 thru 511	00040000h - 01FFFFFFh	32,512KB	Upper 127/128
1	0	1	0	0	8 thru 511	00080000h - 01FFFFFFh	32,256KB	Upper 63/64
1	0	1	0	1	16 thru 511	00100000h - 01FFFFFFh	31MB	Upper 31/32
1	0	1	1	0	32 thru 511	00200000h - 01FFFFFFh	30MB	Upper 15/16
1	0	1	1	1	64 thru 511	00400000h - 01FFFFFFh	28MB	Upper 7/8
1	1	0	0	0	128 thru 511	00800000h - 01FFFFFFh	24MB	Upper 3/4
1	1	0	0	1	256 thru 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
X	1	1	0	X	NONE	NONE	NONE	NONE
X	1	X	1	X	NONE	NONE	NONE	NONE

Note: 1. X = don't care.

Note: 2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Single Die Individual Block Memory Protection (WPS=1)



Note: 1. Individual Block/Sector protection is only valid when WPS=1.

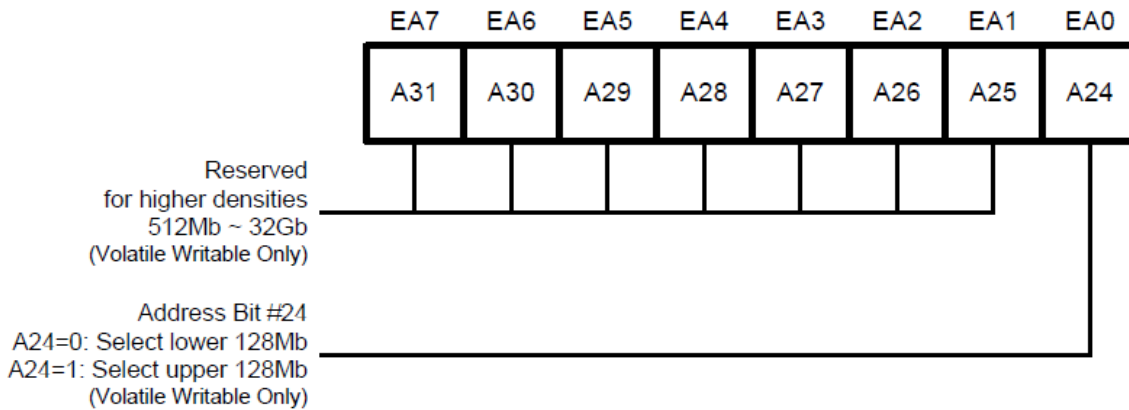
Note: 2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

Extended Address Register – Volatile Writable Only

In addition to the Status Registers, H7A5FM26B7CX provides a volatile Extended Address Register which consists of the 4th byte of memory address. The Extended Address Register is used only when the device is operating in the 3-Byte Address Mode (ADS=0). The lower 128Mb memory array (00000000h – 00FFFFFFh) is selected when A24=0, all instructions with 3-Byte addresses will be executed within that region. When A24=1, the upper 128Mb memory array (01000000h – 01FFFFFFh) will be selected.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7h)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignored. However, any command with 4-byte address input will replace the Extended Address Register Bits (A31-A24) with new settings.

Upon power up or after the execution of a Software/Hardware Reset, the Extended Address Register values will be cleared to 0.



Instruction Set Table 1 (Standard SPI, 3-Byte Address Mode ADS=0)(1)

Data Input Output	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
I/O Protocol(1-1-1)							
Software Die Select	C2h	Die ID#					
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Read Device ID	ABh	Dummy	Dummy	Dummy	ID7-ID0(2)		
Read Manufacturer/Device ID	90h	Dummy	Dummy	00h	MF7-MF0	ID7-ID0	
Read JEDEC ID	9Fh	MF7-MF0	ID15-ID8	ID7-ID0			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	UID63-0	
Read Data	03h	A23-A16	A15-A8	A7-A0	D7-D0		
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
4KB Sector Erase	20h	A23-A16	A15-A8	A7-A0			
4KB Sector Erase with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0		
32KB Block Erase	52h	A23-A16	A15-A8	A7-A0			
64KB Block Erase	D8h	A23-A16	A15-A8	A7-A0			
64KB Block Erase with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h/60h						
Read Status Register-1	05h	S7-S0(2)					
Write Status Register-1(4)	01h	S7-S0(4)					
Read Status Register-2	35h	S15-S8(2)					
Write Status Register-2	31h	S15-S8					
Read Status Register-3	15h	S23-S16(2)					
Write Status Register-3	11h	S23-S16					
Read Extended Address Register	C8h	EA7-EA0(2)					
Write Extended Address Register	C5h	EA7-EA0					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0			
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Global Block Lock	7Eh						
Global Block Unlock	98h						
Read Block Lock	3Dh	A23-A16	A15-A8	A7-A0	L7-L0		

Individual Block Lock	36h	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	39h	A23-A16	A15-A8	A7-A0			
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Enter 4-Byte Address Mode	B7h						
Exit 4-Byte Address Mode	E9h						
Enable Reset	66h						
Reset Device	99h						

Instruction Set Table 2(Dual/Quad SPI Instructions, 3-Byte Address Mode ADS=0)

Data Input Output	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
I/O Protocol (1 – 1 – 2)(7)									
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /2			
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /2		
I/O Protocol (1 – 2 – 2)(6,7)									
Mftr./Device ID Dual I/O	92h	A23-A16 /2	A15-A8 /2	00 /2	Dummy /2	MF7-MF0 /2	ID7-ID0 /2	MF7-MF0 /2	ID7-ID0 /2
Fast Read Dual I/O	BBh	A23-A16 /2	A15-A8 /2	A7-A0 /2	Dummy /2	D7-D0 /2			
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24 /2	A23-A16 /2	A15-A8 /2	A7-A0 /2	Dummy /2	D7-D0 /2		
I/O Protocol (1 – 1 – 4)(9)									
Quad Input Page Program(3)	32h	A23-A16	A15-A8	A7-A0	D7-D0 /4				
Quad Page Program with 4-Byte Address(3)	34h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0 /4			
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /4			
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /4		
I/O Protocol (1 – 4 – 4)(8,9)									
Mftr./Device ID Quad I/O	94h	A23-A16 /4	A15-A8 /4	00h /4	Dummy /4	Dummy /4	Dummy /4	MF7-MF0 /4	ID7-ID0 /4
Fast Read Quad I/O	EBh	A23-A16 /4	A15-A8 /4	A7-A0 /4	Dummy /4	Dummy /4	Dummy /4	D7-D0 /4	
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24 /4	A23-A16 /4	A15-A8 /4	A7-A0 /4	Dummy /4	Dummy /4	Dummy /4	D7-D0 /4
Set Burst with Wrap	77h	Dummy /4	Dummy /4	Dummy /4	W7-W0 /4				

Instruction Set Table 3(Standard SPI, 4-Byte Address Mode ADS=1)(1)

Data Input Output	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
I/O Protocol (1 – 1 – 1)							
Software Die Select	C2h	Die ID#					
Write Enable	C6h						
Volatile Status Register Write Enable	50h						
Write Disable	04h						
Read Device ID	ABh	Dummy	Dummy	Dummy	ID7-ID0(2)		
Read Manufacturer/Device ID	90h	Dummy	Dummy	00h	MF7-MF0	ID7-ID0	
Read JEDEC ID	9Fh	MF7-MF0	ID15-ID8	ID7-ID0			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	Dummy	UID63-0
Read Data	03h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	Dummy	D7-D0	
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
4KB Sector Erase	20h	A31-A24	A23-A16	A15-A8	A7-A0		
4KB Sector Erase with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0		
32KB Block Erase	52h	A31-A24	A23-A16	A15-A8	A7-A0		
64KB Block Erase	D8h	A31-A24	A23-A16	A15-A8	A7-A0		
64KB Block Erase with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h/60h						
Read Status Register-1	05h	S7-S0(2)					
Write Status Register-1(4)	01h	S7-S0(4)					
Read Status Register-2	35h	S15-S8(2)					
Write Status Register-2	31h	S15-S8					
Read Status Register-3	15h	S23-S16(2)					
Write Status Register-3	11h	S23-S16					
Read Extended Address Register	C8h	EA7-EA0(2)					
Write Extended Address Register	C5h	EA7-EA0					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Erase Security Register(5)	44h	A31-A24	A23-A16	A15-A8	A7-A0		
Program Security Register(5)	42h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Read Security Register(5)	48h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0
Global Block Lock	7Eh						
Global Block Unlock	98h						
Read Block Lock	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	L7-L0	
Individual Block Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0		

Erase / Program Suspend	75h								
Erase / Program Resume	7Ah								
Enter 4-Byte Address Mode	B7h								
Exit 4-Byte Address Mode	E9h								
Enable Reset	66h								
Reset Device	99h								

Instruction Set Table 4 (Dual/Quad SPI Instructions, 4-Byte Address Mode ADS=1)

Data Input Output	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
I/O Protocol (1 – 1 – 2)(7)									
Fast Read Dual Output	3Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /2		
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /2		
I/O Protocol (1 – 2 – 2)(6,7)									
Mftr./Device ID Dual I/O	92h	A31-A24 /2	A23-A16 /2	A15-A8 /2	00/2	Dummy /2	MF7-MF0 /2	ID7-ID0 /2	MF7-MF0 /2
Fast Read Dual I/O	BBh	A31-A24 /2	A23-A16 /2	A15-A8 /2	A7-A0 /2	Dummy /2	D7-D0 /2		
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24 /2	A23-A16 /2	A15-A8 /2	A7-A0 /2	Dummy /2	D7-D0 /2		
I/O Protocol (1 – 1 – 4)(9)									
Quad Input Page Program(3)	32h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0 /4			
Quad Page Program with 4-Byte Address(3)	34h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0 /4			
Fast Read Quad Output	6Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /4		
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0 /4		
I/O Protocol (1 – 4 – 4)(8,9)									
Mftr./Device ID Quad I/O	94h	A31-A24 /4	A23-A16 /4	A15-A8 /4	00h/4	Dummy /4	Dummy /4	Dummy /4	MF7-MF0 /4
Fast Read Quad I/O	EBh	A31-A24 /4	A23-A16 /4	A15-A8 /4	A7-A0 /4	Dummy /4	Dummy /4	Dummy /4	D7-D0 /4
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24 /4	A23-A16 /4	A15-A8 /4	A7-A0 /4	Dummy /4	Dummy /4	Dummy /4	D7-D0 /4
Set Burst with Wrap	77h	Dummy /4	Dummy /4	Dummy /4	W7-W0 /4				

Note 1: Data bytes are shifted with Most Significant Bit first. Byte fields with bold and italic style D7-D0 indicate data output from the device. "D7-D0" indicates single I/O pin; "D7-D0 /2" indicates 2 I/O pins; "D7-D0 /4" indicates 4 I/O pins.

Note 2: The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.

Note 3: At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

Note 4: Write Status Register-1 (01h) can also be used to program Status Register-1&2

Note 5: Security Register Address:

Status Register 1 : A23-16 = 00h; A15-8 = 10h; A7-0 = byte address

Status Register 2 : A23-16 = 00h; A15-8 = 20h; A7-0 = byte address

Status Register 3 : A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

Note 6: Dual SPI address input format:

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 , A6, A4, A2, A0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 , A7, A5, A3, A1

Note 7: Dual SPI data input/output format:

IO0 = D6, D4, D2, D0,

IO1 = D7, D5, D3, D1,

Note 8: Quad SPI address input format:

IO0 = A20, A16, A12, A8, A4, A0

IO1 = A21, A17, A13, A9, A5, A1

IO2 = A22, A18, A14, A10, A6, A2

IO3 = A23, A19, A15, A11, A7, A3

Set Burst with Wrap input format:

IO0 = x, x, x, x, x, x, W4, x

IO1 = x, x, x, x, x, x, W5, x

IO2 = x, x, x, x, x, x, W6, x

IO3 = x, x, x, x, x, x, x, x

Note 9: Quad SPI data input/output format:

IO0 = D4, D0,

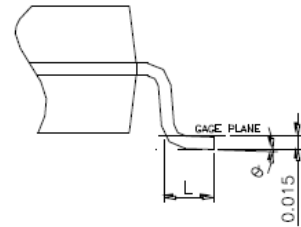
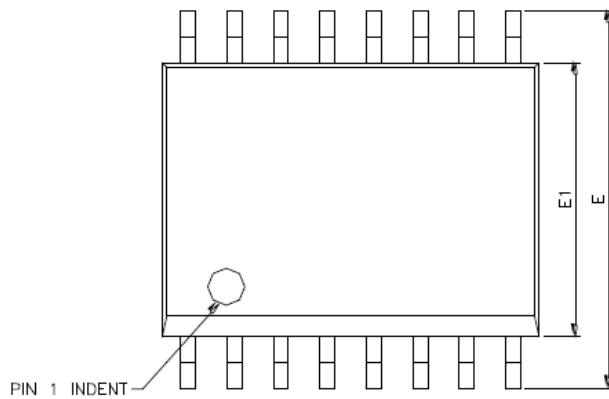
IO1 = D5, D1,

IO2 = D6, D2,

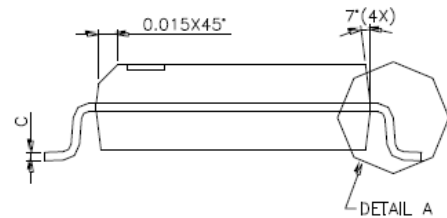
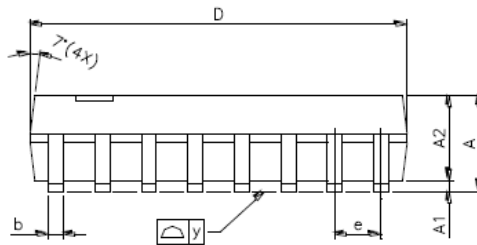
IO3 = D7, D3,

Package Description

16-Pin SOIC 300-mil



DETAIL A



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	---	0.30	0.004	---	0.012
A2	---	2.31	---	---	0.091	---
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
L	0.38	0.81	1.27	0.015	0.032	0.050
y	---	---	0.076	---	---	0.003
θ	0°	---	8°	0°	---	8°

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Nov. 2017	Maven Hsu	N/A
1.0	First SPEC. Release.	Nov. 2017	Maven Hsu	N/A