1G-BIT 3.3V SPI-NAND FLASH MEMORY

Descriptions

The H7A41G26B7CG (1G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The H7A41G26B7CG incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 25mA active and 10µA for standby.

H7A41G26B7CG was offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory. The H7A41G26B7CG 1G-bit memory array is organized into 65,536 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase).

The H7A41G26B7CG has 1,024 erasable blocks and supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.The H7A41G26B7CG supports JEDEC standard manufacturer and device ID, one 2,048-Byte Unique ID page, one 2,048-Byte parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, bad block management are also available in H7A41G26B7CG.

Features

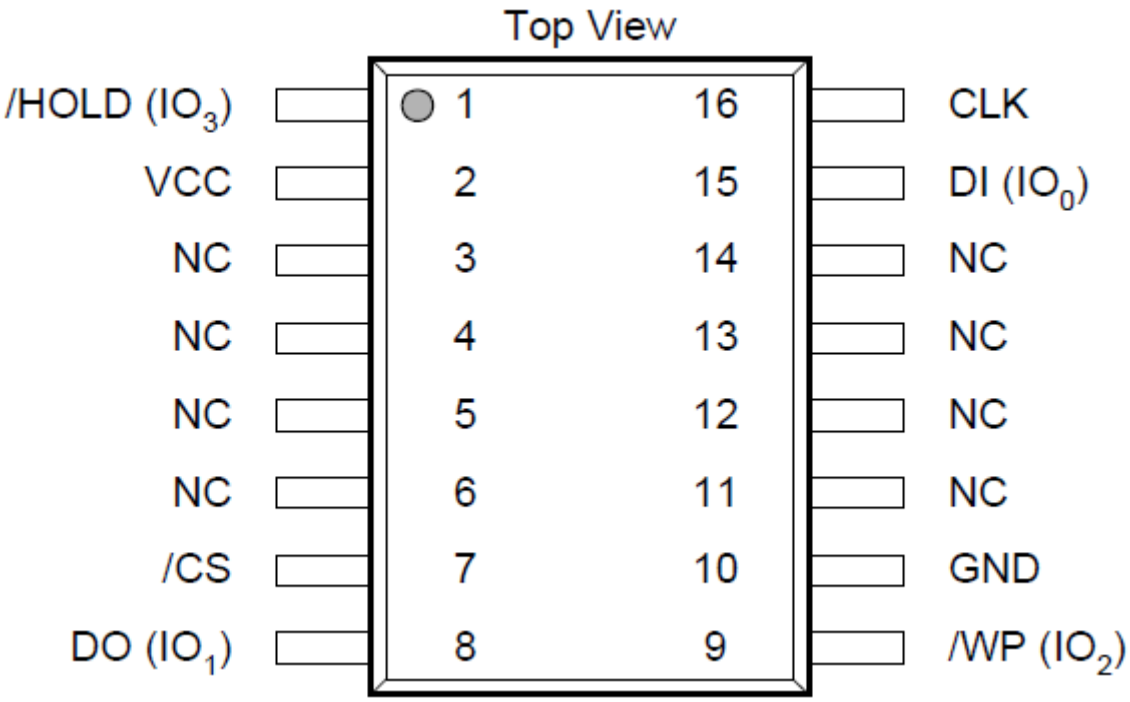
- **Basic Features**
  - Density : 1Gbit / 128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP,/Hold
  - Dual SPI: CLK, /CS, IO0, IO1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Fast Program/Erase performance
  - More than 100,000 erase/program cycles
  - More than 10-year data retention
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 25mA active, 10µA standby current
  - 0°C to 70°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - bad block management and LUT access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - 2KB Unique ID and 2KB parameter pages
  - Ten 2KB OTP pages
- **Space Efficient Packaging**
  - 16-pin SOIC 300-mil

Notes:
1. H7A41G26B7CG: Default BUF=1 after power up.
2. LUT stands for Look-Up Table.
3. OTP pages can only be programmed.

Ordering Information

Part No	Density	Read Command Mode	Package	Grade
H7A41G26B7CG	1G-bit/128M-byte	Buffer Read Mode (BUF=1)	16-Pin SOIC 300-mil	Commercial

Pad Configuration



16-pin SOIC 300-mil

Pin Description (Simplified)

16-pin SOIC, 300-mil			
Pad NO.	**PAD Name**	**I/O**	**Function**
1	/HOLD (IO3)	Input / Output	Hold Input (Data Input Output 3)
2	VCC		Power Supply
3~6,11~14	N/C		No Connect
7	/CS	Input	Chip Select Input
8	DO (IO1)	Input / Output	Data Output (Data Input Output 1)
9	/WP (IO2)	Input / Output	Write Protect Input (Data Input Output 2)
10	GND		Ground
15	DI (IO0)	Input / Output	Data Input (Data Input Output 0)
16	CLK	Input	Serial Clock Input

Note1: IO0 and IO1 are used for Standard and Dual SPI instructions and IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI

Absolute Maximum Rating

Item	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{cc}		-0.6 ~ 4.6	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	-0.6 ~ 4.6	V
Transient Voltage on any Pin	V_{IOT}	<20nS Transient Relative to Ground	－2.0V to VCC+2.0V	V
Short circuit output current	I_{OS}		5	mA
Storage Temperature	T_{STG}		-65 ~ 150	˚C
Lead Temperature	T_{LEAD}		Notes2	˚C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model(3)	－2000 to +2000	V

Note 1: This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

Note 2: Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.

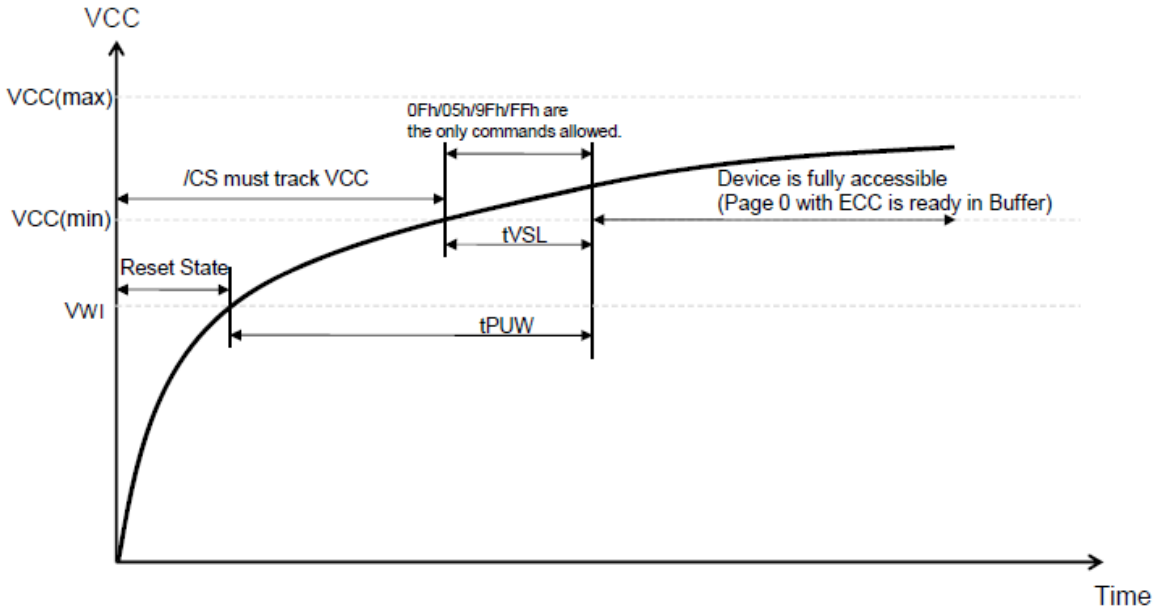
Note 3: JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms)..

Operating Ranges

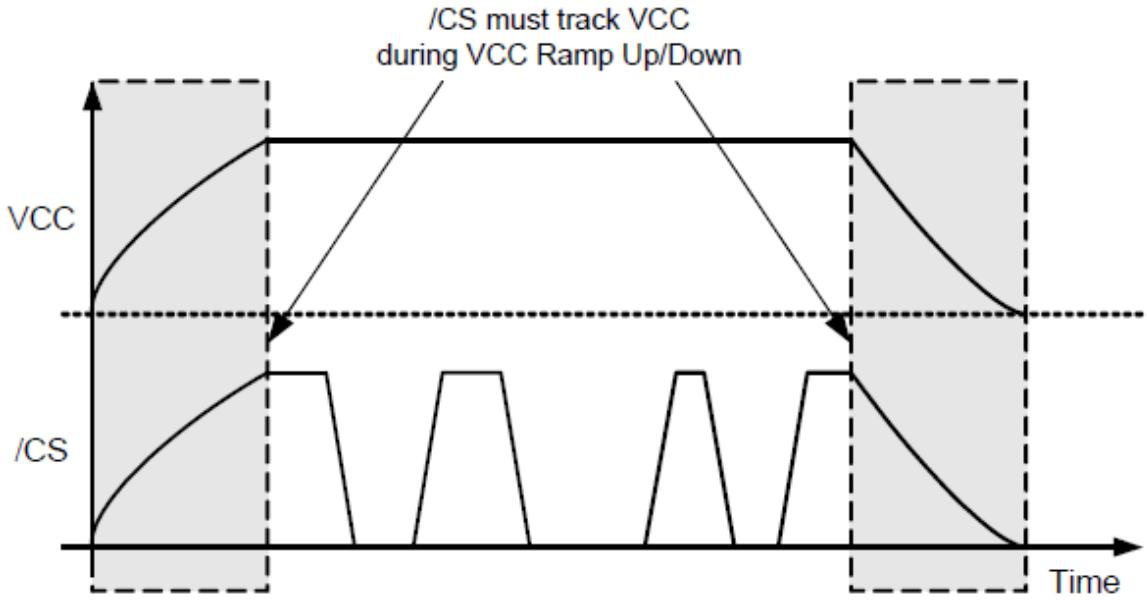
Parameter	Symbol	Conditions	Spec.		Unit
			Min.	Max.	
Supply Voltage	Vcc		2.7	3.6	V
Ambient Temperature, Operating	Ta	Commercial	0	70	˚C

Device Power-up / Power-down Timing Requirement

Parameter	Symbol	Spec.		Unit
		Min.	Max.	
VCC (min) to /CS Low	tVSL	50	500	us
Time Delay Before Write Instruction	tPUW	5		ms
Write Inhibit Threshold Voltage	V_{WI}	1.0	2.0	V



Power-up Timing and Voltage Levels



Power-up, Power-Down Requirement

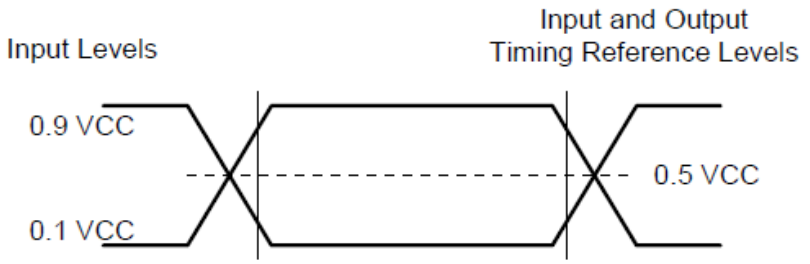
DC Characteristics

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	
Input Capacitance	CIN(1)	VIN=0V(1)			6	pF
Output Capacitance	COUT(1)	VOUT=0V(1)			8	pF
Input Leakage	ILI				+/-2	uA
I/O Leakage	ILO				+/-2	uA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		10	50	uA
Read Current	ICC2	C = 0.1 VCC / 0.9 VCC DO = Open		25	35	mA
Current Page Program	ICC3	/CS = VCC		25	35	mA
Current Block Erase	ICC4	/CS = VCC		25	35	mA
Input Low Voltage	VIL				0.3 x Vcc	V
Input High Voltage	VIH		0.7 x Vcc			V
Output Low Voltage	VOL	IOL=2.1mA			0.4	V
Output High Voltage	VOH	IOH = –400 µA	2.4			V

Note 1: Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

AC Measurement Conditions

Parameter	Symbol	Spec.		Unit
		MIN	Max	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR,TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V



AC Measurement I/O Waveform

AC Electrical Characteristics

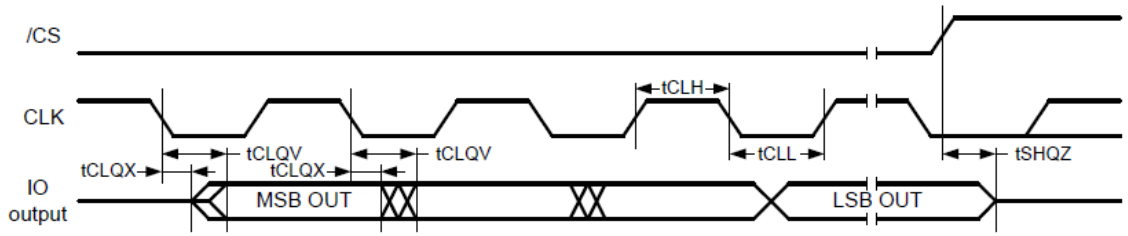
Description	Symbol	ALT	Spec.			Unit
			MIN	TYP	Max	
Clock frequency for all instructions	FR	fC1	D.C.		104	Mhz
Clock High, Low Time for all instructions	tCLH,tCLL(1)		4			ns
Clock Rise Time peak to peak	tCLCH(2)		0.1			V/ns
Clock Fall Time peak to peak	tCHCL(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/CS Active Hold Time relative to CLK	tCHSH		3			ns
/CS Not Active Setup Time relative to CLK	tSHCH		3			ns
/CS Deselect Time (for Array Read → Array Read)	tSHSL1	tCSH	10			ns
/CS Deselect Time (for Erase, Program or Read Status Registers → Read Status Registers)	tSHSL2	tCSH	50			ns
Output Disable Time	tSHQZ(2)	tDIS			7	ns
Clock Low to Output Valid	tCLQV	tV			7	ns
Output Hold Time	tCLQX	tHO	2			ns
/HOLD Active Setup Time relative to CLK	tHLCH		5			ns
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns
/HOLD to Output Low-Z	tHHQX(2)	tLZ			7	ns
/HOLD to Output High-Z	tHLQZ(2)	tHZ			12	ns
Write Protect Setup Time Before /CS Low	tWHSL		20			ns
Write Protect Hold Time After /CS High	tSHWL		100			ns
Status Register Write Time	tw				50	ns
/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase	tRST(2)				5/10/100	us
Read Page Data Time (ECC disabled)	tRD1				25	us
Read Page Data Time (ECC enabled)	tRD2				60	us
Page Program, OTP Lock, BBM Management Time	tPP			250	700	us
Block Erase Time	tBE			2	10	ms
Number of partial page programs	NoP				4	times

Note: 1. Clock high + Clock low must be less than or equal to 1/fC.

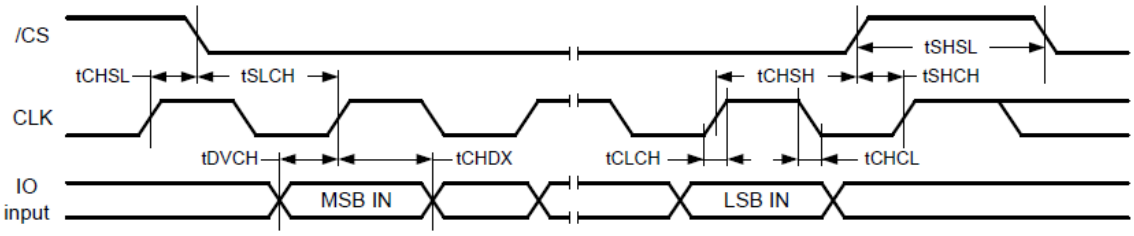
Note: 2. Value guaranteed by design and/or characterization, not 100% tested in production.

Note: 3. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

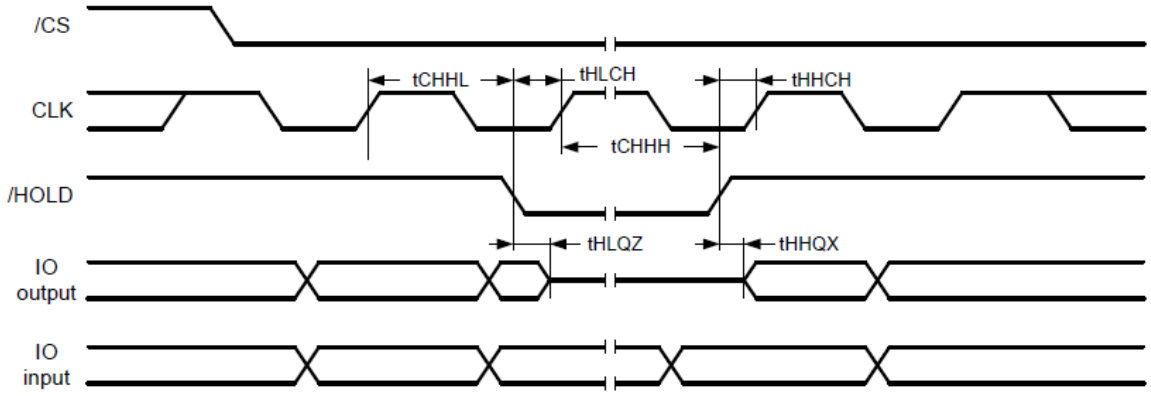
Serial Output Timing



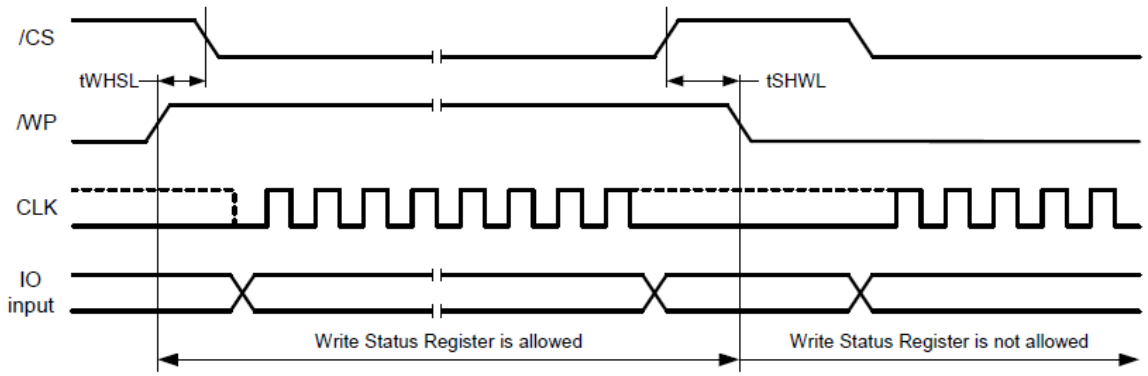
Serial Input Timing



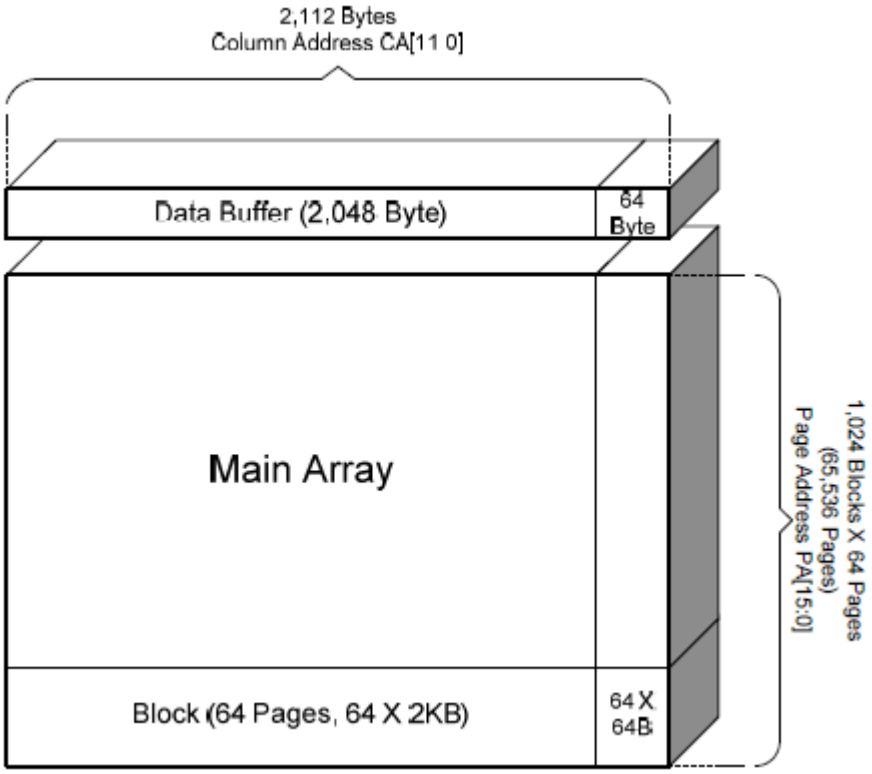
/Hold Timing



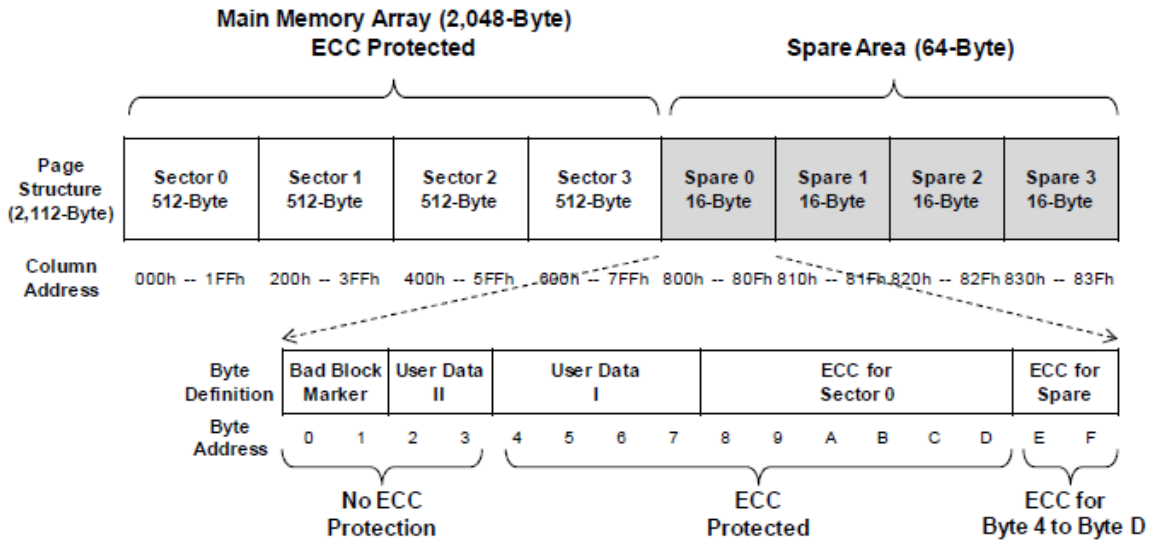
/WP Timing



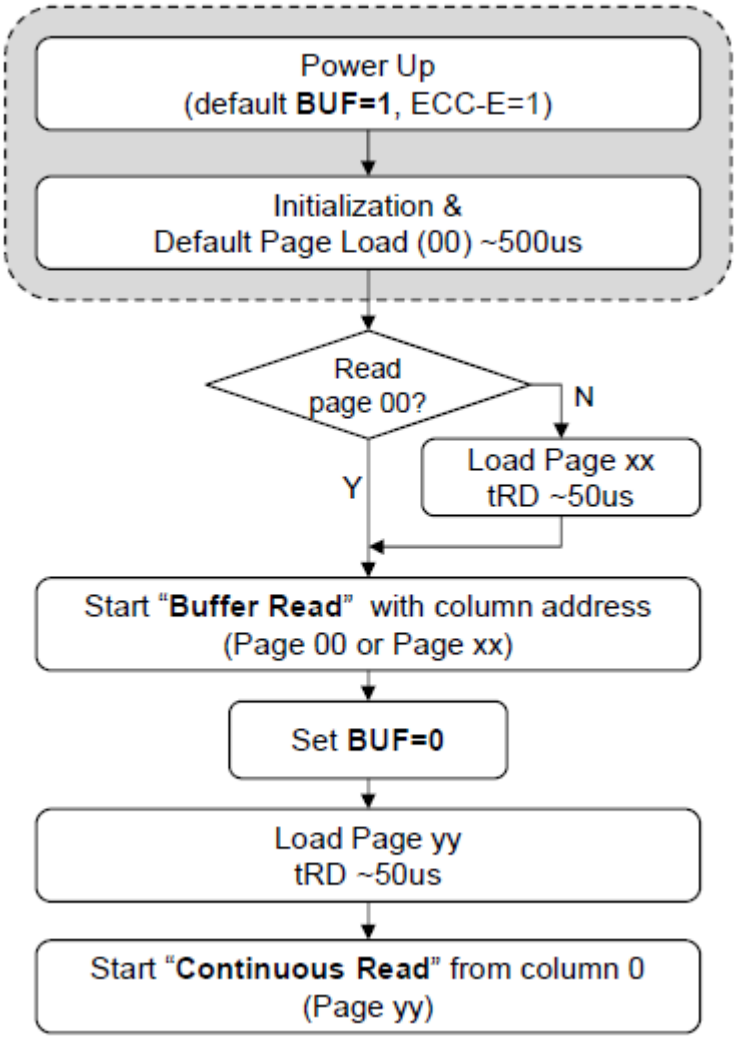
Block Diagram and Memory Architecture



Address Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SpiFlash (up to 128M-Bit)	X	X	X	X	X	X	X	X	64KB Block Addr (256 Blocks)								Page Address (256 Pages)								Byte Address (0-255 Byte)							
SpiFlash (up to 32G-Bit)	64KB Block Address																Page Address (256 Pages)								Byte Address (0-255 Byte)							
Serial NAND (1G-Bit)	X	X	X	X	**Page Address (PA) [15:0]**												**Column Address (CA) [11:0]**															
	X	X	X	X	128KB Block Addr (1024 Blocks)												Page Addr (64 Pages)				Ext	Byte Address (0-2047 Byte)										



Device Operation Flow



Standard SPI Instructions

The H7A41G26B7CG is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

Dual SPI Instructions

The H7A41G26B7CG supports Dual SPI operation when using instructions such as "Fast Read Dual Output (3Bh)" and "Fast Read Dual I/O (BBh)". These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI Instructions

The H7A41G26B7CG supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the H7A41G26B7CG operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, /HOLD pin will act as a dedicated IO pin (IO3).

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the H7A41G26B7CG provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, the H7A41G26B7CG will maintain a reset condition while VCC is below the threshold value of VWI. While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute or Block Erase instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

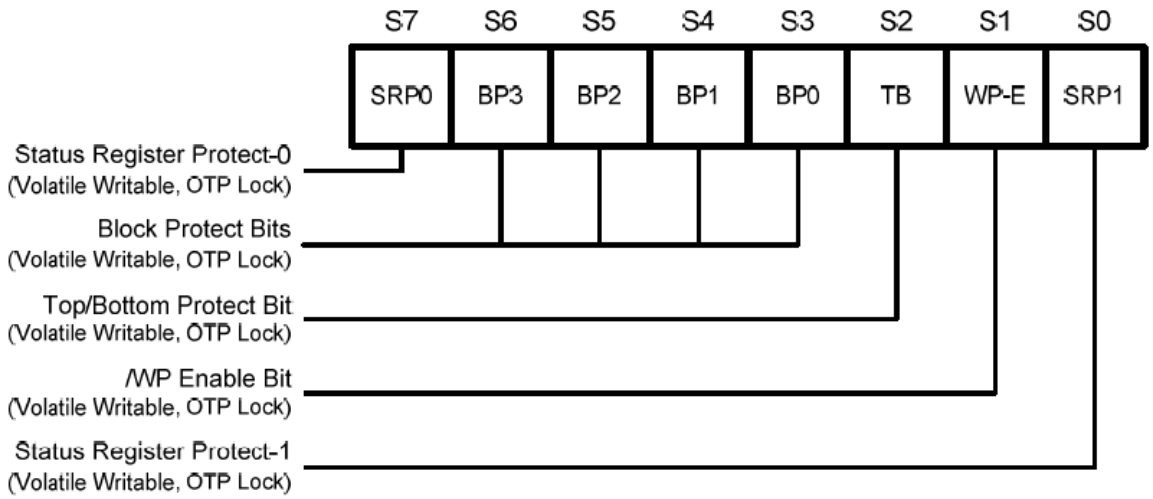
The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the H7A41G26B7CG,the device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

Protection, Configuration and Status Registers

Three Status Registers are provided for H7A41G26B7CG: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

Protection Register / Status Register-1 (Volatile Writable, OTP lockable)



Block Protect Bits – Volatile Writable, OTP lockable

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions. The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

Write Protection Enable Bit – Volatile Writable, OTP lockable

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

Status Register Protect Bits – Volatile Writable, OTP lockable

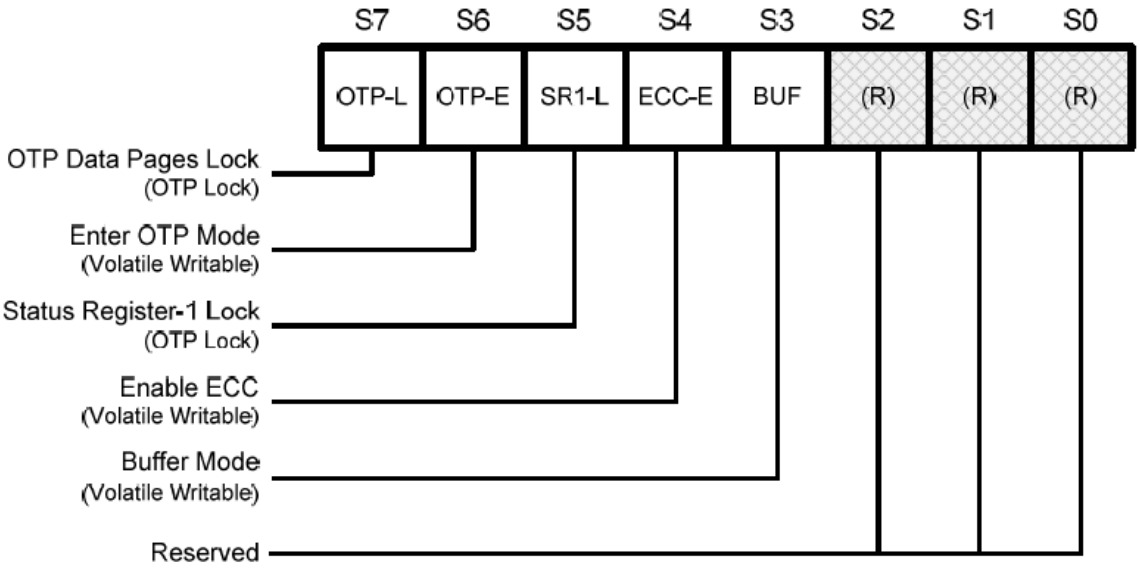
The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SRP1	**SRP0**	**WP-E**	**/WP /IO2**	**Descriptions**
0	0	0	X	No /WP functionality /WP pin will always function as IO2
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) /WP pin will function as IO2 for Quad operations
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) /WP pin will function as IO2 for Quad operations
1	0	0	X	Power Lock Down(1) SR-1 /WP pin will always function as IO2
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) /WP pin will always function as IO2

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All "Write/Program/Erase" commands are blocked Entire device (SRs, Array, OTP area) is read-only

Note: 1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

Configuration Register / Status Register-2 (Volatile Writable)



One Time Program Lock Bit (OTP-L) – OTP lockable

In addition to the main memory array, H7A41G26B7CG also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

Enter OTP Access Mode Bit (OTP-E) – Volatile Writable

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

Status Register-1 Lock Bit (SR1-L) – OTP lockable

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1,1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming.

ECC Enable Bit (ECC-E) – Volatile Writable

H7A41G26B7CG has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

Buffer Read / Continuous Read Mode Bit (BUF) – Volatile Writable

H7A41G26B7C provides two different modes for read operations, Buffer Read Mode (BUF=1) and Continuous Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

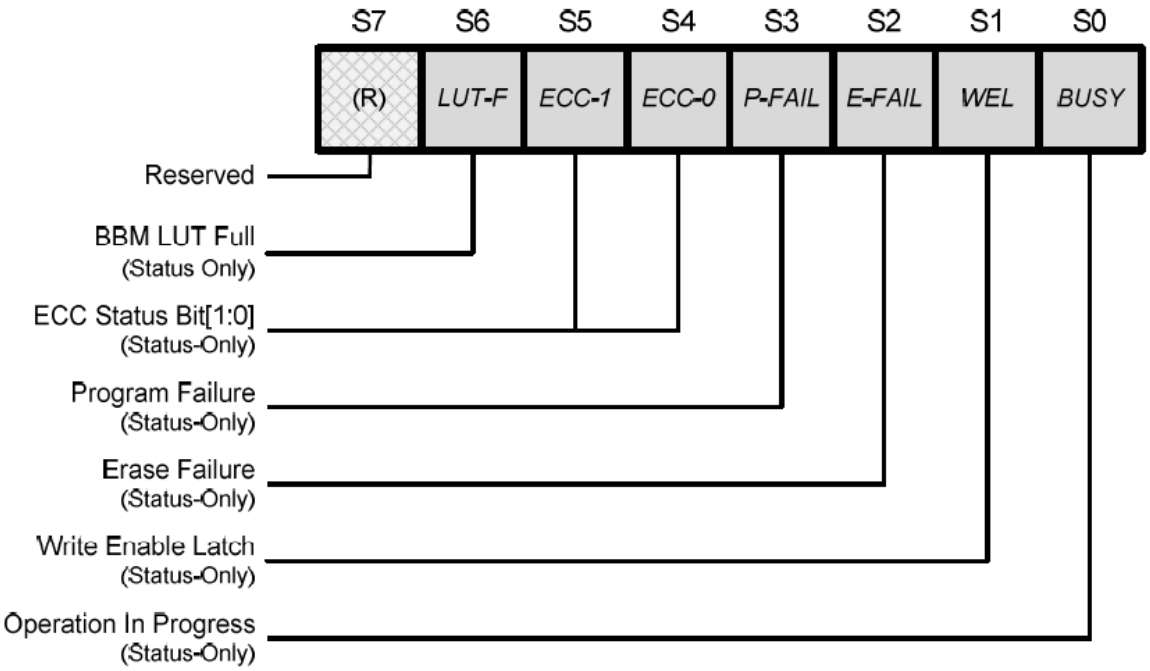
The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 2,111), DO (IO1) pin will become high-Z state.

The Continuous Read Mode (BUF=0) doesn't require the starting Column Address.The device will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (Byte 2,048) is reached, the data output will continue through the next memory page. With Continuous Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

For H7A41G26B7CG part number, the default value of BUF bit after power up is 1. BUF bit can be written to 0 in the Status Register-2 to perform the Continuous Read operation.

BUF	ECC-E	Read Mode (Starting from Buffer)	ECC Status	Data Output Structure
1	0	Buffer Read	N/A	2048 + 64
1	1	Buffer Read	Page base	2048 +64
0	0	Continuous Read	N/A	2048
0	1	Continuous Read	Operation base	2048

Status Register-3 (Status Only)



Look-Up Table Full (LUT-F) – Status Only

To facilitate the NAND flash memory bad block management, the H7A41G26B7CG is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

Cumulative ECC Status (ECC-1, ECC-0) – Status Only

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command.

ECC-1	ECC-0	Descriptions
0	0	Entire data output is successful, without any ECC correction.
0	1	Entire data output is successful, with 1~4 bit/page ECC corrections in either a single page or multiple pages.
1	0	Entire data output contains more than 4 bits errors only in a single page which cannot be repaired by ECC. In the Continuous Read Mode, an additional command can be used to read out the Page Address (PA) which had the errors.
1	1	Entire data output contains more than 4 bits errors/page in multiple pages. In the Continuous Read Mode, the additional command can only provide the last Page Address (PA) that had failures, the user cannot obtain the PAs for other failure pages. Data is not suitable to use.

Note: 1. ECC-1,ECC-0 = (1,1) is only applicable during Continuous Read operation (BUF=0).

Program/Erase Failure (P-FAIL, E-FAIL) – Status Only

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.

Erase/Program In Progress (BUSY) – Status Only

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, BBM Management, Program Execute, Block Erase, Program Execute for OTP area, OTP Locking or after a Continuous Read instruction. During this time the device will ignore further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

Write Enable Latch (WEL) – Status Only

WEL is a read only bit in status register (S1) that is set to 1 after executing a Write Enable Instruction. WEL status bit is cleared to 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages.

Status Register Memory Protection

STATUS REGISTER					(1G-BIT / 128M-BYTE) MEMORY PROTECTION			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[15:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	None	None	None	None
0	0	0	0	1	1022 &1023	FF80h - FFFFh	256KB	Upper 1/512
0	0	0	1	0	1020 ~ 1023	FF00h - FFFFh	512KB	Upper 1/256
0	0	0	1	1	1016 ~ 1023	FE00h - FFFFh	1MB	Upper 1/128
0	0	1	0	0	1008 ~ 1023	FC00h - FFFFh	2MB	Upper 1/64
0	0	1	0	1	992 ~ 1023	F800h - FFFFh	4MB	Upper 1/32
0	0	1	1	0	960 ~ 1023	F000h - FFFFh	8MB	Upper 1/16
0	0	1	1	1	896 ~ 1023	E000h - FFFFh	16MB	Upper 1/8
0	1	0	0	0	768 ~ 1023	C000h - FFFFh	32MB	Upper 1/4
0	1	0	0	1	512 ~ 1023	8000h - FFFFh	64MB	Upper 1/2
1	0	0	0	1	0 & 1	0000h – 007Fh	256KB	Lower 1/512
1	0	0	1	0	0 ~ 3	0000h - 00FFh	512KB	Lower 1/256
1	0	0	1	1	0 ~ 7	0000h - 01FFh	1MB	Lower 1/128
1	0	1	0	0	0 ~ 15	0000h - 03FFh	2MB	Lower 1/64
1	0	1	0	1	0 ~ 31	0000h - 07FFh	4MB	Lower 1/32
1	0	1	1	0	0 ~ 63	0000h - 0FFFh	8MB	Lower 1/16
1	0	1	1	1	0 ~ 127	0000h - 1FFFh	16MB	Lower 1/8
1	1	0	0	0	0 ~ 255	0000h - 3FFFh	32MB	Lower 1/4
1	1	0	0	1	0 ~ 511	0000h - 7FFFh	64MB	Lower 1/2
X	1	0	1	X	0 ~ 1023	0000h - FFFFh	128MB	ALL
X	1	1	X	X	0 ~ 1023	0000h - FFFFh	128MB	ALL

Note: 1. X = don't care.

Note: 2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

Command Set Table(Buffer Read, BUF = 1, xxCG Default Power Up Mode)

Commands	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	FFh								
JEDEC ID	9Fh	Dummy	EFh	AAh	21h				
Read Status Register	0Fh / 05h	SR Addr	S7-0	S7-0	S7-0	S7-0	S7-0	S7-0	S7-0
Write Status Register	1Fh / 01h	SR Addr	S7-0						
Write Enable	06h								
Write Disable	04h								
BB Management (Swap Blocks)	A1h	LBA	LBA	PBA	PBA				
Read BBM LUT	A5h	Dummy	LBA0	LBA0	PBA0	PBA0	LBA1	LBA1	PBA1
Last ECC failure Page Address	A9h	Dummy	PA15-8	PA7-0					
Block Erase	D8h	Dummy	PA15-8	PA7-0					
Program Data Load (Reset Buffer)	02h	CA15-8	CA7-0	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	84h	CA15-8	CA7-0	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	32h	CA15-8	CA7-0	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	34h	CA15-8	CA7-0	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	10h	Dummy	PA15-8	PA7-0					
Page Data Read	13h	Dummy	PA15-8	PA7-0					
Read	03h	CA15-8	CA7-0	Dummy	D7-0	D7-0	D7-0	D7-0	D7-0
Fast Read	0Bh	CA15-8	CA7-0	Dummy	D7-0	D7-0	D7-0	D7-0	D7-0
Fast Read with 4-Byte Address	0Ch	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0	D7-0	D7-0
Fast Read Dual Output	3Bh	CA15-8	CA7-0	Dummy	D7-0/2	D7-0/2	D7-0/2	D7-0/2	D7-0/2
Fast Read Dual Output with 4-Byte Address	3Ch	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0/2	D7-0/2	D7-0/2
Fast Read Quad Output	6Bh	CA15-8	CA7-0	Dummy	D7-0/4	D7-0/4	D7-0/4	D7-0/4	D7-0/4
Fast Read Quad Output with 4-Byte Address	6Ch	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0/4	D7-0/4	D7-0/4
Fast Read Dual I/O	BBh	CA15-8/ 2	CA7-0/ 2	Dummy /2	D7-0/2	D7-0/2	D7-0/2	D7-0/2	D7-0/2
Fast Read Dual I/O with 4-Byte Address	BCh	CA15-8/ 2	CA7-0/ 2	Dummy /2	Dummy /2	Dummy /2	D7-0/2	D7-0/2	D7-0/2
Fast Read Quad I/O	EBh	CA15-8/ 4	CA7-0/ 4	Dummy /4	Dummy /4	D7-0/4	D7-0/4	D7-0/4	D7-0/4
Fast Read Quad I/O with 4-Byte Address	ECh	CA15-8/ 4	CA7-0/ 4	Dummy /4	Dummy /4	Dummy /4	Dummy /4	Dummy /4	D7-0/4

Note 1: Output designates data output from the device.

Note 2: Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.

Note 3: Page Address (PA) requires 16 bits. PA[15:6] is the address for 128KB blocks (total 1,024 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).

Note 4: Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[9:0] & PBA[9:0] are effective Block Addresses. LBA[15:14] is used for additional information.

Note 5: Status Register Addresses:

Status Register 1 / Protection Register: Addr = Axh
Status Register 2 / Configuration Register: Addr = Bxh
Status Register 3 / Status Register: Addr = Cxh

Note 6: Dual SPI Address Input (CA15-8 / 2 and CA7-0 / 2) format:

IO0 = x, x, CA10, CA8, CA6, CA4, CA2, CA0
IO1 = x, x, CA11, CA9, CA7, CA5, CA3, CA1

Note 7: Dual SPI Data Output (D7-0 / 2) format:

IO0 = D6, D4, D2, D0, ……
IO1 = D7, D5, D3, D1, ……

Note 8: Quad SPI Address Input (CA15-8 / 4 and CA7-0 / 4) format:

IO0 = x, CA8, CA4, CA0
IO1 = x, CA9, CA5, CA1
IO2 = x, CA10, CA6, CA2
IO3 = x, CA11, CA7, CA3

Note 9: Quad SPI Data Input/Output (D7-0 / 4) format:

IO0 = D4, D0, ……
IO1 = D5, D1, ……
IO2 = D6, D2, ……
IO3 = D7, D3, ……

Note 10: All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

Note 11: For all Read operations in the Buffer Read Mode, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the H7A41G26B7CG is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	2,112-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	2,112-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to “1” first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A “Page Data Read” command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the “Buffer Read Mode” command structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit setting. ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (2K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from “1” to “0”) until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to “1” to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any “Program Data Load” commands. The “Program Execute” command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during “Program Execute”, and the ECC information will be stored into the 64-Byte spare area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the “OTP Access Mode” (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to “1”, and issue a “Program Execute” command without any Page Address. After the device finishes the OTP lock setting (BUSY=0), the user can set OTPE to “0” to return to the main memory array operation.

SR1-L OTP Lock Operation

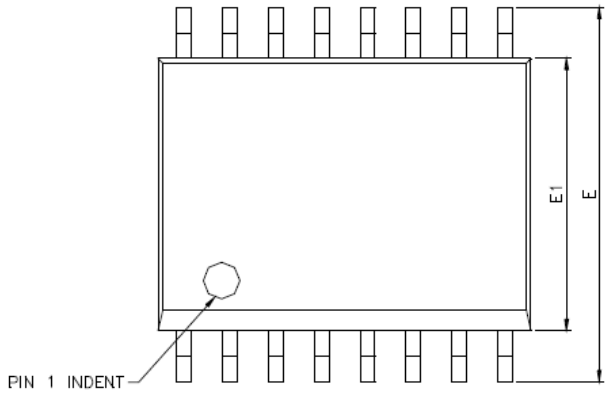
The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0) or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to “1”s as well to allow SR1-L bit being set to “1” to permanently lock the protection settings in the Status Register-1 (SR1). Similar to the OTP-L setting procedure above, in order to set SR1-L lock bit, the device must enter the “OTP Access Mode” (OTP-E=1) first, and SR1-L bit should be set to “1” prior to the “Program Execute” command without any Page Address. Once SR1-L is set to “1” (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

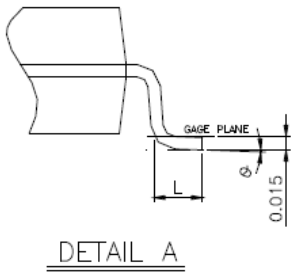
Parameter Page Data Definitions

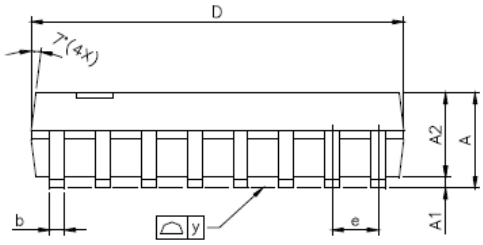
Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	02h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer	57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44~63	Device model	57h, 32h, 35h, 4Eh, 30h, 31h, 47h, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	EFh
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	40h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 04h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	14h, 00h
105~106	Block endurance	01h, 06h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	BCh, 02h
135~136	Maximum block erase time (us)	10h, 27h
137~138	Maximum page read time (us)	32h, 00h
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	Set at test
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768+	Reserved	

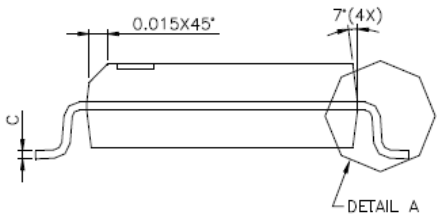
Package Description

16-Pin SOIC 300-mil









Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	---	0.30	0.004	---	0.012
A2	---	2.31	---	---	0.091	---
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
L	0.38	0.81	1.27	0.015	0.032	0.050
y	---	---	0.076	---	---	0.003
θ	0°	---	8°	0°	---	8°

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Sep. 2017	Maven Hsu	N/A
1.0	First SPEC. Release.	Sep. 2017	Maven Hsu	N/A