128Mb (2M×4Bank×16) Synchronous DRAM

Descriptions

H2A11281636B is a high-speed synchronous dynamic random access memory (SDRAM), organized as 2M words x 4 banks x 16 bits. H2A11281636B delivers a data bandwidth of up to 166M words per second

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command..

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. H2A11281636B is ideal for main memory in high performance applications.

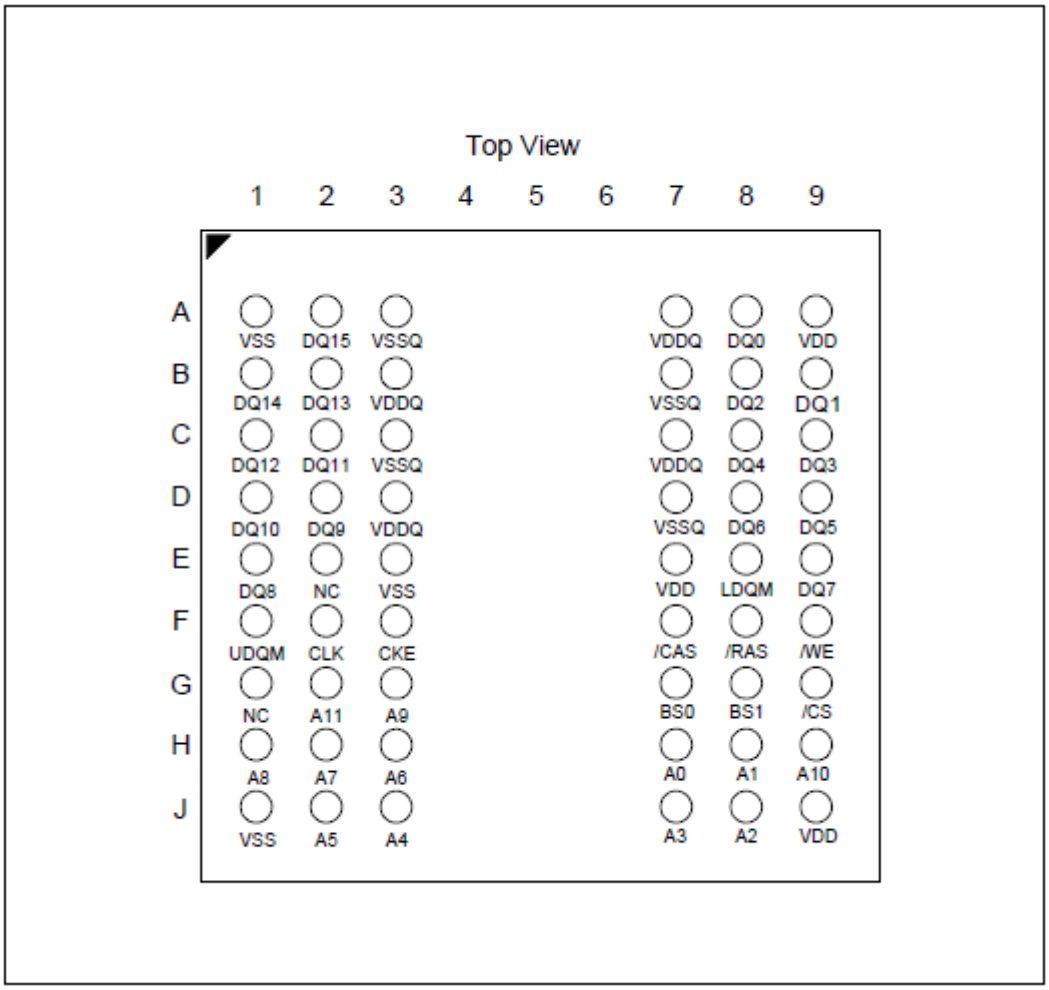
Features

- 3.3V +/- 0.3V Power Supply
- Up to 166 MHz Clock Frequency
- 2,097,152 Words x 4 banks x 16 bits organization
- Self Refresh Mode
- CAS Latency: 2 and 3
- Burst Length: 1,2,4,8 and full page
- Burst Read,Single Writes Mode
- Byte Data Controlled by LDQM, UDQM
- Auto-precharge and Controlled Precharge
- 4K Refresh cycles / 64 mS
- Interface: LVTTL
- Packaged in TFBGA 54 Ball (8x8 mm^2)

Ordering Information

Part No	Organization	Max. Frequency	Package	Grade
H2A11281636B8VC	8M X 16	133MHz @ CL3	54Ball BGA, 8x8mm	Commercial
H2A11281633BMVC	8M X 16	166MHz @ CL3	54Ball BGA, 8x8mm	Commercial

Ball Configuration



TFBGA 54 Ball (8x8 mm^2)

Ball Description (Simplified)

Ball Location	Name	Function Description
H7, H8, J8, J7, J3,J2, H3, H2, H1,G3, H9, G2	A0~A11	**(Address)** Multiplexed pins for row and column address. Row address: A0-A11. Column address: A0-A8. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
G7, G8	BS0, BS1	**(Bank Selet)** Select bank to activate during row address latch time, or bank to read/write during address latch time.
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0~DQ 15	**(Data Input/Output)** Multiplexed pins for data output and input.
G9	CS	**(Chip Select)** Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
F8	RAS	**(Row Address Strobe)** Command input. When sampled at the rising edge of the clock RAS, CAS and WE define the operation to be executed.
F7	CAS	**(Column Address Strobe)** Referred to RAS
F9	WE	**(Write Enable)** Referred to RAS
F1, E8	UDQM, LDQM	**(Input/Output Mask)** The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
F2	CLK	**(Clock Inputs)** System clock used to sample inputs on the rising edge of clock.
F3	CKE	**(Clock Enable)** CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
A9, E7, J9	VDD	**(Power)** Power for input buffers and logic circuit inside DRAM.
A1, E3, J1	VSS	**(Ground)** Ground for input buffers and logic circuit inside DRAM.
A7, B3, C7, D3	VDDQ	**(Power for I/O buffer)** Separated power from VDD, to improve DQ noise immunity.
A3, B7, C3, D7	VSSQ	**(Ground for I/O)** Separated ground from VSS, to improve DQ noise immunity.
E2, G1	NC	**(No Connection)** No connection

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ V_{DD}+0.5 (≦ 4.6V max.)		V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.5 ~ +4.6		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +70	°C
T_{STG}	Storage Temperature Range	-55 ~ +150		°C
TSOLDER	Soldering Temperature (10s)	260		˚C
P_D	Power Dissipation	1		W
I_{OS}	Short Circuit Current	50		mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Capacitance (V_{CC}=3.3V, f=1MHz, T_A=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{CLK}	Clock Capacitance	-	-	3.5	pF
C_I	Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	-	-	3.8	pF
C_O	Input / Output Capacitance	-	-	6.5	pF

Recommended DC Operating Conditions (T_A=-0°C ~+70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V_{IH}	Input Logic High Voltage	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Logic Low Voltage	-0.3	-	0.8	V

Note: * All voltages referred to VSS.

* VIH (max.) = VDD / VDDQ +1.5V for pulse width ≦ 5ns

* VIL (min.) = VDD / VSSQ -1.5V for pulse width ≦ 5ns

Recommended DC Operating Conditions

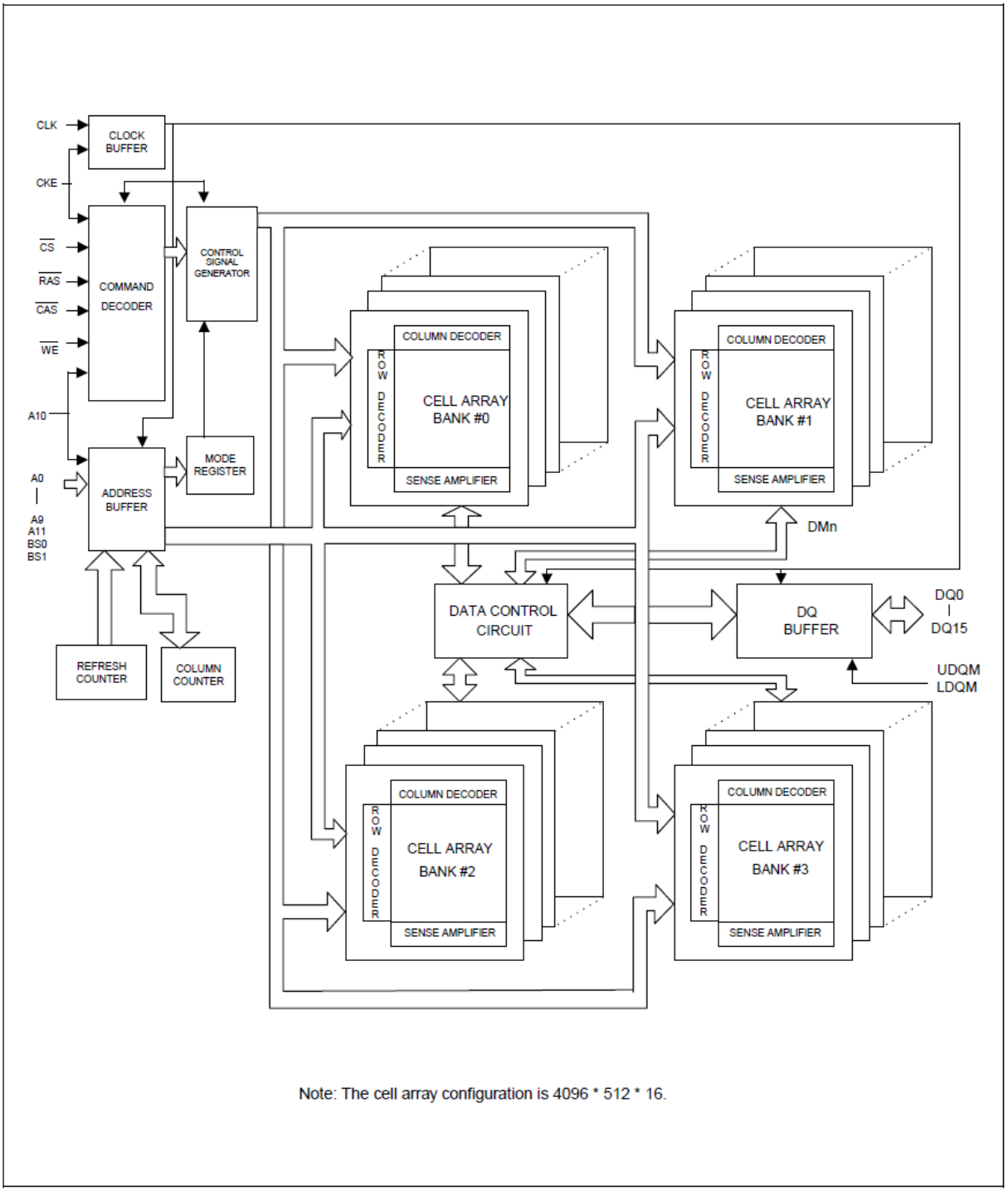
(V_{DD}=3.3V±0.3V, T_A=0°C ~ 70°C)

Parameter		Symbol	Max.		Units
			166MHz	133MHz	
Operating Current t_{CK} = min., t_{RC} = min. Active precharge command cycling without burst operation	1 Bank operation	IDD1	50	45	mA
Standby Current t_{CK} = min., CS = V_{IH} $V_{IH/L}$ = V_{IH} (min.) /V_{IL} (max.) Bank: inactive state	CKE = V_{IH}	IDD2	20		mA
	CKE = V_{IL} (Power Down mode)	IDD2P	2		mA
Standby Current CLK = V_{IL}, CS = V_{IH} $V_{IH/L}$ = V_{IH} (min.) /V_{IL} (max.) Bank: inactive state	CKE = V_{IH}	IDD2S	12		mA
	CKE = V_{IL} (Power Down mode)	IDD2PS	2		mA
No Operating Current t_{CK} = min., CS = V_{IH} (min.) Bank: active state (4 Banks)	CKE = V_{IH}	IDD3	35	30	mA
	CKE = V_{IL} (Power Down mode)	IDD3P	12		mA
Burst Operating Current (t_{CK} = min.) Read/ Write command cycling		IDD4	75	70	mA
Auto Refresh Current (t_{CK} = min.) Auto refresh command cycling		IDD5	65	60	mA
Self Refresh Current Self refresh mode (CKE = 0.2V)		IDD6	2	2	mA

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{IL}	Input Leakage Current	0≤V_I≤V_{DDQ}, V_{DDQ}=V_{DD} All other pins not under test=0V	-5	5	uA
I_{OL}	Output Leakage Current	0≤V_O≤V_{DDQ}, D_{OUT} is disabled	-5	5	uA
V_{OH}	High Level Output Voltage	I_O=-4mA	2.4	-	V
V_{OL}	Low Level Output Voltage	I_O=+4mA	-	0.4	V

Block Diagram



Note: The cell array configuration is 4096 * 512 * 16.

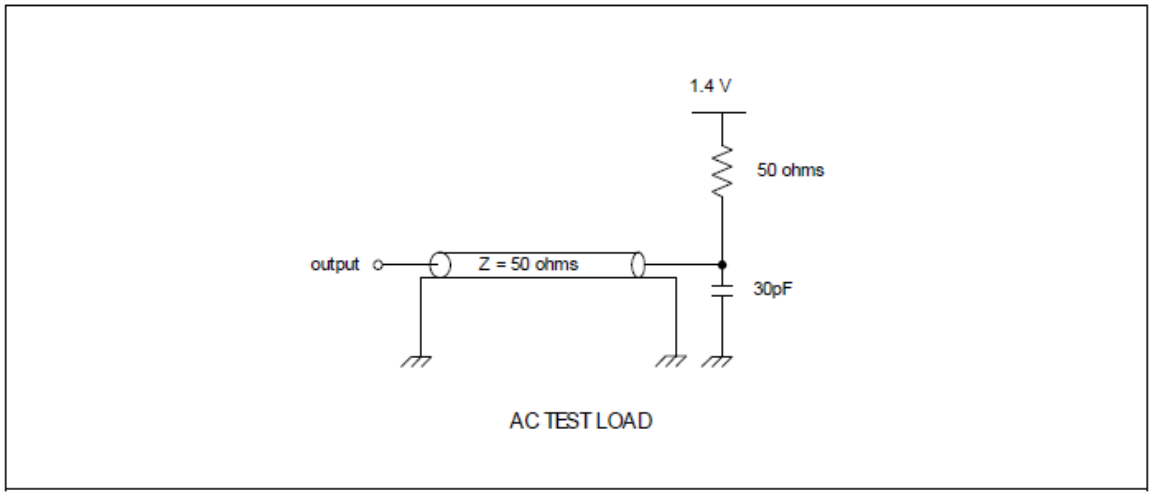
AC Test Characteristics and Operating Conditions

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

PARAMETER		SYM.	166MHz		133MHz		Unit	Notes
			Min.	Max.	Min.	Max.		
Ref/Active to Ref/Active Command Period		tRC	60		65		nS	
Active to Precharge Command Period		tRAS	42	100000	45	100000		
Active to Read/Write Command Delay Time		tRCD	15		20			
Read/Write(a) to Read/Write(b)Command Period		tCCD	1		1		tCK	
Precharge to Active(b) Command Period		tRP	15		20		nS	
Active(a) to Active(b) Command Period		tRRD	12		15			
Write Recovery Time	CL* = 2	tWR	2		2		tCK	
	CL* = 3		2		2			
CLK Cycle Time	CL* = 2	tCK	7.5	1000	10	1000	nS	
	CL* = 3		6	1000	7.5	1000		
CLK High Level Width		tCH	2		2.5			8
CLK Low Level Width		tCL	2		2.5			8
Access Time from CLK	CL* = 2	tAC		6		6		9
	CL* = 3			5		5.4		9
Output Data Hold Time		tOH	3		3			9
Output Data High Impedance Time	CL* = 2	tHZ		6		6		7
	CL* = 3			5		5.4		
Output Data Low Impedance Time		tLZ	0		0			9
Power Down Mode Entry Time		tSB	0	6	0	7.5		
Transition Time of CLK (Rise and Fall)		tT		1		1		
Data-in-Set-up Time		tDS	1.5		1.5			8
Data-in Hold Time		tDH	0.8		0.8			8
Address Set-up Time		tAS	1.5		1.5			8
Address Hold Time		tAH	0.8		0.8			8
CKE Set-up Time		tCKS	1.5		1.5			8
CKE Hold Time		tCKH	0.8		0.8			8
Command Set-up Time		tCMS	1.5		1.5			8
Command Hold Time		tCMH	0.8		0.8			8
Refresh Time		tREF		64		64	mS	
Mode Register Set Cycle Time		tRSC	2		2		tCK	
Exit self refresh to ACTIVE command		tXSR	72		75		nS	

Notes:

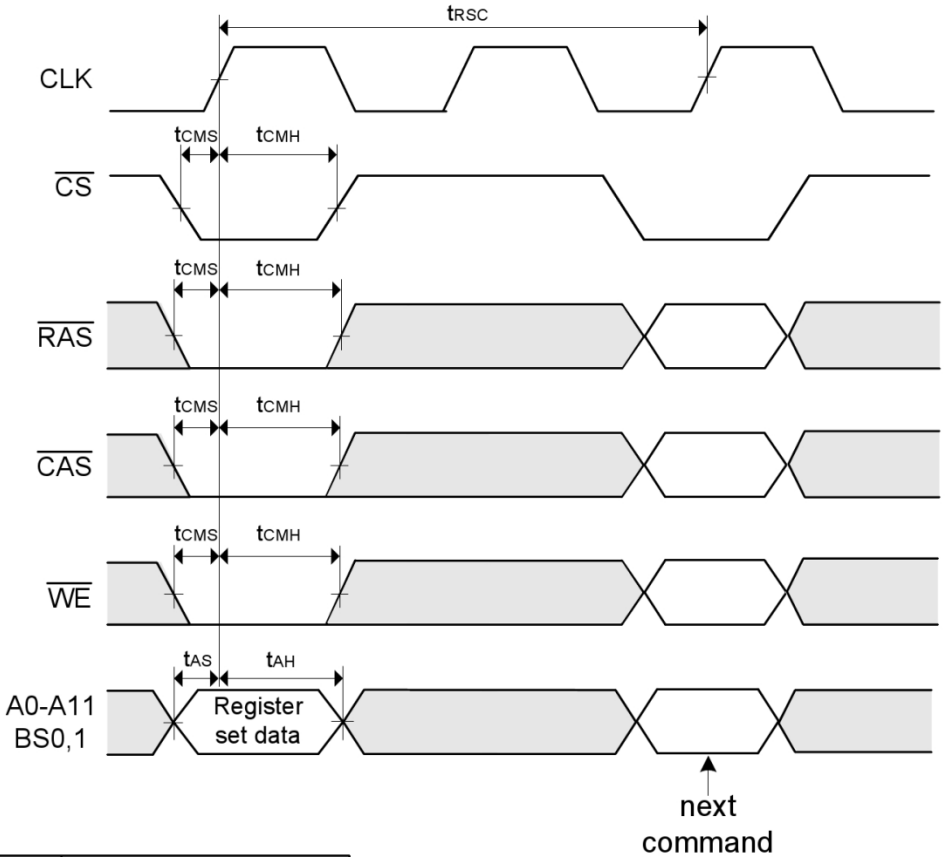
1. Operation exceeds “Absolute Maximum Ratings” may cause permanent damage to the devices.
2. All voltages are referenced to VSS.
3. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of tCK and tRC.
4. These parameters depend on the output loading conditions. Specified values are obtained with output open.
5. Power up sequence is further described in the “Functional Description” section.
6. AC test load diagram.



AC TEST LOAD

7. tHZ defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
8. Assumed input rise and fall time (tT) = 1nS.
   If tr & tf is longer than 1nS, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]nS should be added to the parameter.
9. If clock rising time (tT) is longer than 1nS, (tT/2-0.5)nS should be added to the parameter.

Address Input for Mode Register Set



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	Reserved
A11	"0"	
BS0	"0"	
BS1	"0"	

		Burst Length	
A2	A1 A0	Sequential	Interleave
0	0 0	1	1
0	0 1	2	2
0	1 0	4	4
0	1 1	8	8
1	0 0	Reserved	Reserved
1	0 1		
1	1 0		
1	1 1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

A6 A5 A4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

* "Reserved" should stay "0" during MRS cycle.

Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	0	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page*	n	n	n	Cn Cn+1 Cn+2……	-

* Page length is a function of I/O organization and column addressing ×16 (CA0 ~ CA7):Full page = 256bits

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A11, A9~A10
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	L	H	H	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. DQM Truth Table

Command	Symbol	CKE		/CS
		n-1	n	
Data Write/Output Enable	ENB	H	X	H
Data Mask/Output Disable	MASK	H	X	L
Upper Byte Write Enable/Output Enable	BSTH	H	X	L
Read	READ	H	X	L
Read with Auto Pre-charge	READA	H	X	L
Write	WRIT	H	X	L
Write with Auto Pre-charge	WRITA	H	X	L
Bank Activate	ACT	H	X	L
Pre-charge Select Bank	PRE	H	X	L
Pre-charge All Banks	PALL	H	X	L
Mode Register Set	MRS	H	X	L

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

3. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-	n					
Activating	Clock Suspend Mode Entry		H	L	X	X	X	X	X
Any	Clock Suspend Mode		L	L	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit		L	H	X	X	X	X	X
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	X	X	X	X	X
Power Down	Power Down Exit		L	H	X	X	X	X	X

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	Nop or power down (Note 8)
	L	H	H	X	X	NOP or BST	Nop or power down (Note 8)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Refresh or self refresh (Note 10)
	L	L	L	L	Op-Code	MRS	Mode register accessing
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	X	X	NOP or BST	Nop
	L	H	L	H	BA/CA/A10	READ/READA	Begin read: Determine AP (Note 11)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write: Determine AP (Note 11)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Pre-charge (Note 12)
	L	L	L	H	X	REF/SELF	ILLEGAL (Note 10)
	L	L	L	L	Op-Code	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end → Row active
	L	H	H	H	X	NOP	Continue burst to end → Row active
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read: Determine AP (Note 13)
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start write: Determine AP (Note 13, 14)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging (Note 10)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering
	L	H	H	H	X	NOP	Continue burst to end → Write recovering
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read: Determine AP 7, 8 (Note 13, 14)
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new write: Determine AP 7 (Note 13)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging (Note 15)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	Continue burst to end → Pre-charging
	L	H	H	H	X	NOP	Continue burst to end → Pre-charging
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	Burst to end → Write recovering with auto pre-charge
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto pre-charge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9)
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	Nop → Enter idle after t_{RCD}
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RCD}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL (Note 9)
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL (Note 9)
	L	L	H	H	BA/RA	ACT	ILLEGAL (Note 9, 16)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (Note 9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

4. Operative Command Table (Continued) (Note 7)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP *(Note 14)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 9)*
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL *(Note 9)*
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write Recovering with AP	H	X	X	X	X	DESL	Nop → Enter pre-charge after t_{DPL}
	L	H	H	H	X	NOP	Nop → Enter pre-charge after t_{DPL}
	L	H	H	L	X	BST	Nop → Enter pre-charge after t_{DPL}
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL *(Note 9, 14)*
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL *(Note 9)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 9)*
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	Nop → Enter idle after t_{RC}
	L	H	H	X	X	NOP/BST	Nop → Enter idle after t_{RC}
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL
Mode Register Accessing	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 7: All entries assume that CKE was active (High level) during the preceding clock cycle.

Note 8: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode. All input buffers except CKE will be disabled.

Note 9: Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 10: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode. All input buffers except CKE will be disabled.

Note 11: Illegal if tRCD is not satisfied.

Note 12: Illegal if tRAS is not satisfied.

Note 13: Must satisfy burst interrupt condition.

Note 14: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 15: Must mask preceding data which don't satisfy tDPL.

Note 16: Illegal if tRRD is not satisfied.

5. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit self refresh
	L	H	H	X	X	X	X	Self refresh recovery
	L	H	L	H	H	X	X	Self refresh recovery
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	Maintain self refresh
Self Refresh Recovery	H	H	H	X	X	X	X	Idle after t_{RC}
	H	H	L	H	H	X	X	Idle after t_{RC}
	H	H	L	H	L	X	X	ILLEGAL
	H	H	L	L	X	X	X	ILLEGAL
	H	L	H	X	X	X	X	ILLEGAL
	H	L	L	H	H	X	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
Power Down	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit power down
	L	H	X	X	X	X	X	Exit power down → Idle
	L	L	X	X	X	X	X	Maintain power down mode
Both Banks Idle	H	H	H	X	X	X		Refer to operations in Operative Command Table
	H	H	L	H	X	X		
	H	H	L	L	H	X		
	H	H	L	L	L	H	X	Refresh
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	H	L	H	X	X	X		
	H	L	L	H	X	X		
	H	L	L	L	H	X		
	H	L	L	L	L	H	X	Self refresh *(Note 17)*
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down *(Note 17)*
Row Active	H	X	X	X	X	X	X	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down *(Note 17)*
Any State Other than Listed above	H	H	X	X	X	X		Refer to operations in Operative Command Table
	H	L	X	X	X	X	X	Begin clock suspend next cycle *(Note 18)*
	L	H	X	X	X	X	X	Exit clock suspend next cycle
	L	L	X	X	X	X	X	Maintain clock suspend

Remark: H = High level, L = Low level, X = High or Low level (Don't care)

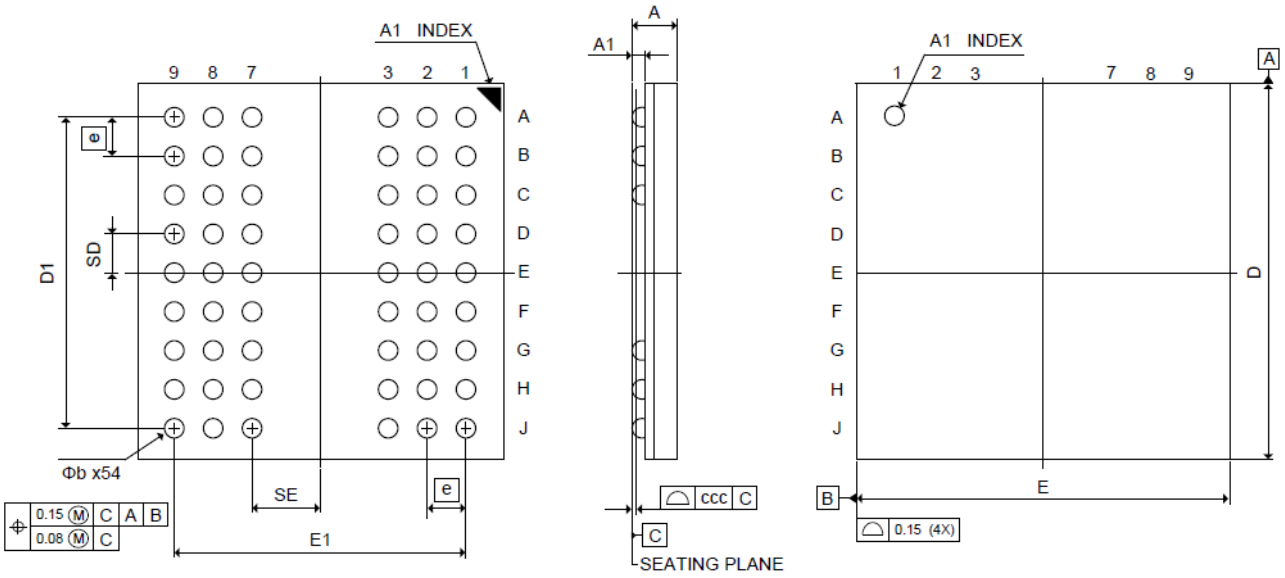
Notes 17: Self refresh can be entered only from the both banks idle state.

Power down can be entered only from both banks idle or row active state.

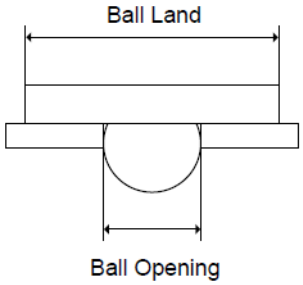
Notes 18: Must be legal command as defined in Operative Command Table

Package Description

Package Outline TFBGA 54 Ball (8x8 mm2, ball pitch:0.8mm, Ø =0.45mm)



SYMBOL	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.28	---	0.40	0.010	---	0.016
b	0.40	0.45	0.50	0.016	0.018	0.020
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		6.40 BSC.			0.252 BSC.	
E	7.90	8.00	8.10	0.311	0.315	0.319
E1		6.40 BSC.			0.252 BSC.	
SE		1.60 TYP.			0.063 TYP.	
SD		0.80 TYP.			0.031 TYP.	
e		0.80 BSC.			0.031 BSC.	
ccc	---	---	0.10	---	---	0.004



Note: 1. Ball land : 0.5mm
2. Ball opening : 0.4mm
3. PCB Ball land suggested ≤ 0.4mm

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2016	Maven Hsu	N/A
1.0	First SPEC. release.	Aug. 2016	Maven Hsu	N/A