# *64Mb (1M×4Banks×16bits) DDR SDRAM*

## *Descriptions*

The H2A264M1643B is CMOS Double Data Rate synchronous dynamic random access memory (DDR SDRAM); organized as 1Meg words x 4 banks by 16 bits. The 64Mb DDR SDRAM uses double data rate architecture to accomplish high-speed operation. The data path internally prefetches multiple bits and it transfers the data for both rising and falling edges of the system clock. It means the doubled data bandwidth can be achieved at the I/O pins.

Available packages: TSOPII 66P 400mil.

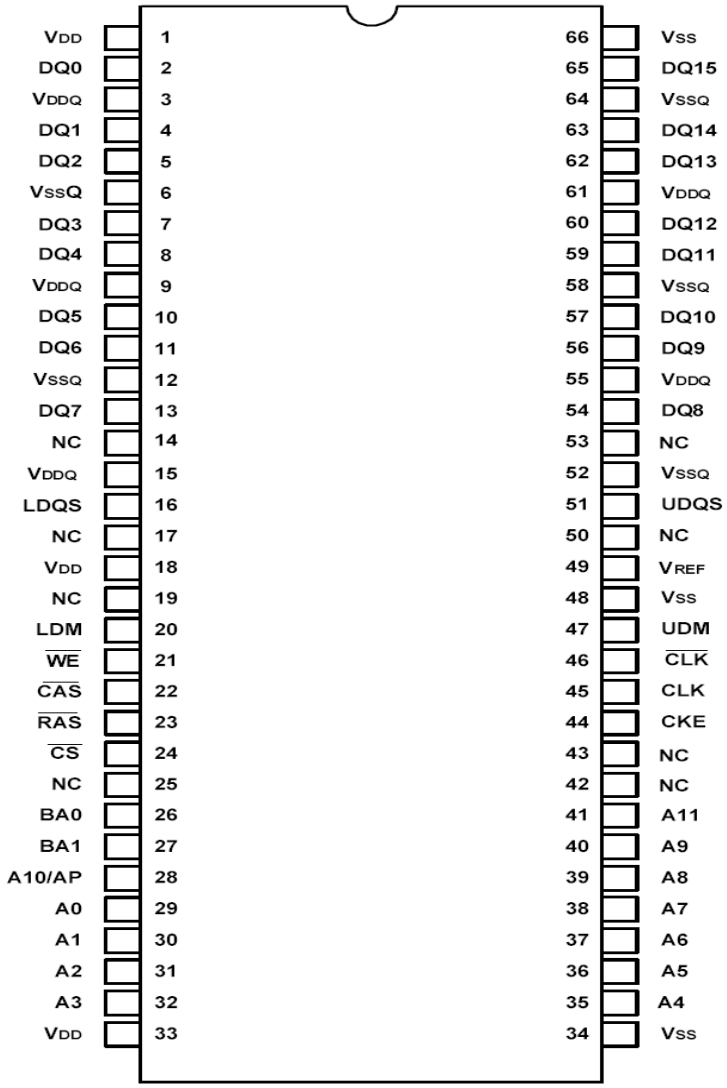
## *Features*

- 2.5V ± 0.2V Power Supply for DDR400/ 333
- Double Data Rate architecture; two data transfers per clock cycle
- Differential clock inputs (CLK and /CLK )
- DQS is edge-aligned with data for Read; center-aligned with data for Write
- CAS Latency: 2, 2.5, 3 and 4
- Burst Length: 2, 4 and 8
- Auto Refresh and Self Refresh
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = 1
- Maximum burst refresh cycle: 8
- Interface: SSTL_2
- Packaged in TSOP II 66-pin, using Lead free materials with RoHS compliant

## Ordering Information

| Part No | Organization | Max. Freq | Package | Grade |
|---|---|---|---|---|
| H2A264M1643BN1C | 4M X 16 | DDR-333 (2.5-2.5-2.5) | 66pin TSOP(II) | Commercial |
| H2A264M1643B91C | 4M X 16 | DDR-400 (3-3-3) | 66pin TSOP(II) | Commercial |

## Pin Assignment




**66pin TSOP II / (400mil x 875mil) / (0.65mm Pin pitch)**

## *Pin Description*

| Pin | Name | Function |
|---|---|---|
| 28–32, 35–41 | A0−A11 | **(Address)** Multiplexed pins for row and column address. Row address: A0 - A11. Column address: A0 – A7. (A10 is used for Auto-precharge) |
| 26, 27 | BA0, BA1 | **(Bank Select)** Select bank to activate during row address latch time, or bank to read/write during column address latch time. |
| 2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65 | DQ0−DQ15 | **(Data Input/ Output)** The DQ0 – DQ15 input and output data are synchronized with both edges of DQS. |
| 16,51 | LDQS, UDQS | **(Data Strobe)** DQS is Bi-directional signal. DQS is input signal during write operation and output signal during read operation. It is Edge-aligned with read data, Center-aligned with write data. |
| 24 | /CS | **(Chip Select)** Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues. |
| 21,22,23 | /CAS,/RAS, /WE | **(Command Inputs)** Command inputs (along with /CS) define the command being entered. |
| 20,47 | LDM,UDM | **(Write Mask)** When DM is asserted “high” in burst write, the input data is masked. DM is synchronized with both edges of DQS. |
| 45, 46 | CLK, /CLK | **(Differential Clock Inputs)** All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. |
| 49 | $V_{REF}$ | **(Reference Voltage)** $V_{REF}$ is reference voltage for inputs. |
| 44 | CKE | **(Clock Enable)** CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered. |
| 1, 18, 33 | $V_{DD}$ | **(Power)** Power for logic circuit inside DDR SDRAM. |
| 34, 48, 66 | $V_{SS}$ | **(Ground)** Ground for logic circuit inside DDR SDRAM. |
| 3, 9, 15, 55, 61 | $V_{DDQ}$ | **(Power for I/O Buffer)** Separated power from VDD, used for output buffer, to improve noise. |
| 6, 12, 52, 58, 64 | $V_{SSQ}$ | **(Ground for I/O Buffer)** Separated ground from VSS, used for output buffer, to improve noise. |
| 14, 17, 19, 25, 42, 43, 50, 53 | NC | **(No Connection)** No connection. |

## Absolute Maximum Rating

| Symbol | Item | Rating | | Units |
|---|---|---|---|---|
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to VSS | -0.5 ~ $V_{DDQ}$ + 0.5 | | V |
| $V_{DD}$, $V_{DDQ}$ | Voltage on VDD/VDDQ supply relative to VSS | -1 ~ 3.6 | | V |
| $T_{OPR}$ | Operating Temperature Range | Commercial | 0 ~ +70 | °C |
| $T_{STG}$ | Storage Temperature Range | -55 ~ +150 | | °C |
| $T_{SOLDER}$ | Soldering Temperature (10s) | 260 | | °C |
| $P_D$ | Power Dissipation | 1 | | W |
| $I_{OUT}$ | Short Circuit Current | 50 | | mA |

***Note 1:*** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

***Note 2:*** This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

***Note 3:*** Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Capacitance ($V_{CC}$=2.5V, f=1MHz, $T_A$=25°C)

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $C_{CLK}$ | Input Capacitance (CLK) | 2.0 | 3.0 | pF |
| $C_{IN}$ | Input Capacitance (A0 to A11, BS0,BS1, /CS, /RAS, /CAS , /WE, UDQM, LDQM, CKE) | 2.0 | 3.0 | pF |
| $C_{I/O}$ | Input/ Output Capacitance (DQ0 to DQ15) | 4.0 | 5.0 | pF |
| $C_{NC}$ | NC Pin Capacitance | - | 1.5 | pF |

***Note:*** These parameters are periodically sampled and not 100% tested.
The NC pins have additional for adjustment for the adjacent pin capacitance.

## Recommended DC Operating Conditions ($T_A$=-0°C ~+70°C)

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 2.3 | 2.5 | 2.7 | V |
| $V_{DDQ}$ | Power Supply Voltage (for I/O Buffer) | 2.3 | 2.5 | 2.7 | V |
| $V_{IH}$ | Input High Voltage | $V_{REF}$+0.15 | - | $V_{DDQ}$+0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3 | - | $V_{REF}$-0.15 | V |
| $V_{REF}$ | Output Logic High Voltage | 0.49x$V_{DDQ}$ | 0.5x$V_{DDQ}$ | 0.51x$V_{DDQ}$ | V |
| $V_{TT}$ | Output Logic Low Voltage | $V_{REF}$-0.04 | $V_{REF}$ | $V_{REF}$+0.04 | V |

## DC Characteristics

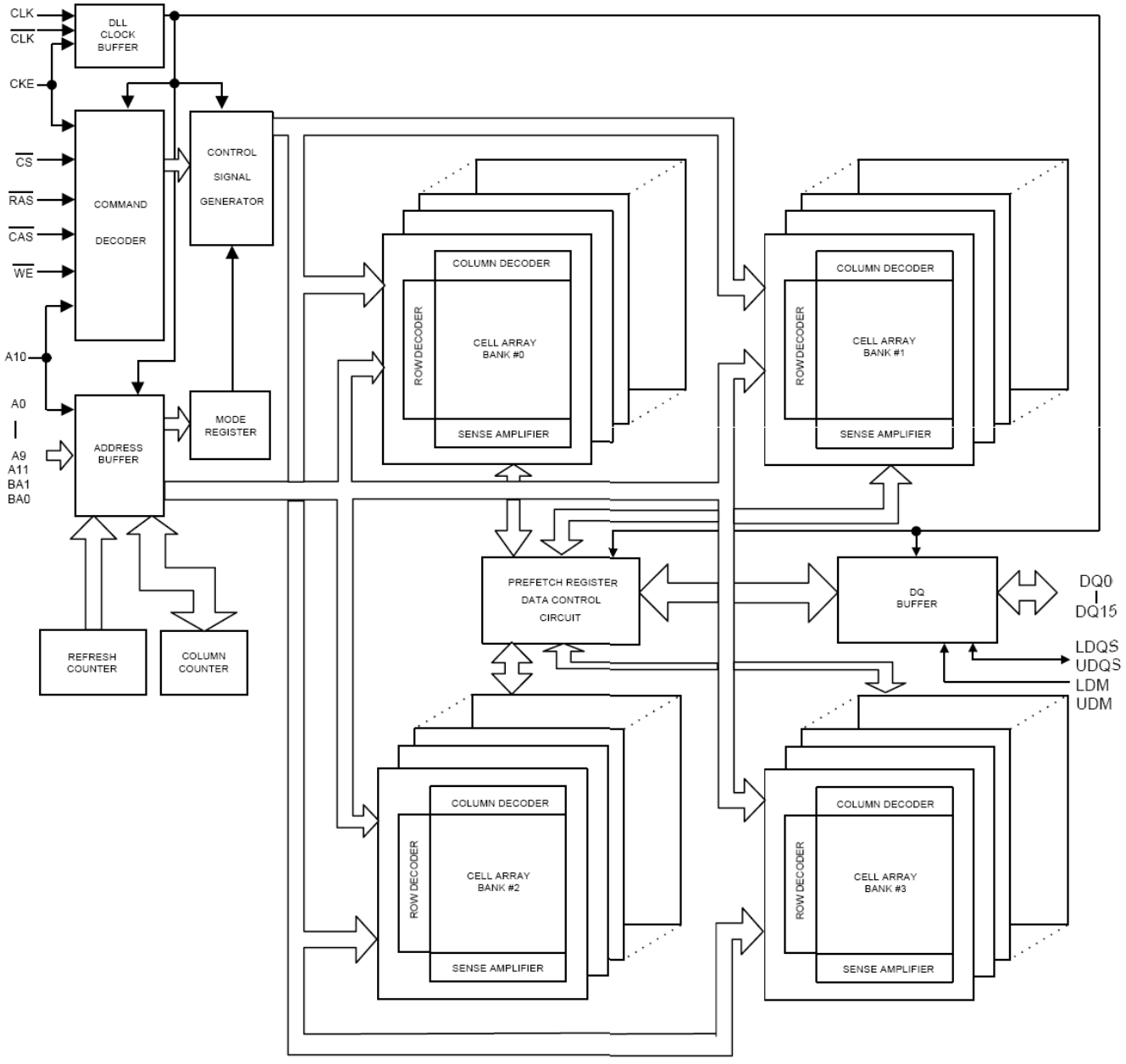
($V_{DD}$=2.5V±0.2V, $T_A$=0°C ~ 70°C)

| Symbol | Parameter | Max. | | Units |
|---|---|---|---|---|
| | | DDR-400 | DDR-333 | |
| $I_{DD0}$ | **(Operating current): One bank Active-Precharge**<br>$t_{RC}$ = $t_{RC}$ min; $t_{CK}$ = $t_{CK}$ min;<br>DQ, DM and DQS inputs changing once per clock cycle;<br>Address and control inputs changing once every two clock cycles. | 45 | 40 | mA |
| $I_{DD1}$ | **(Operating current) One Bank Active-Read-Precharge;**<br>Burst = 4; $t_{RC}$ = $t_{RC}$ min;<br>CL = 3; $t_{CK}$ = $t_{CK\ min}$; $I_{OUT}$ = 0 mA; Address and control inputs changing once per clock cycle. | 55 | 50 | |
| $I_{DD2P}$ | **(Precharge Power Down standby current)**<br>All Banks Idle; Power down mode; CKE ≤ $V_{IL\ max}$;<br>$t_{CK}$ = $t_{CK\ min}$; $V_{in}$ = $V_{REF}$ for DQ, DQS and DM. | 5 | 5 | |
| $I_{DD2N}$ | **(Idle standby current)**<br>/CS ≥ VIH min; All Banks Idle; CKE ≥ $V_{IH\ min}$; $t_{CK}$ = $t_{CK\ min}$;<br>Address and other control inputs changing once per clock cycle; $V_{in}$ ≥ $V_{IH\ min}$ or $V_{in}$ ≤ $V_{IL\ max}$ for DQ, DQS and DM. | 25 | 25 | |
| $I_{DD3P}$ | **(Active Power Down standby current)**<br>One Bank Active; Power down mode; CKE ≤ $V_{IL\ max}$;<br>$t_{CK}$ = $t_{CK\ min}$; $V_{in}$ = $V_{REF}$ for DQ, DQS and DM. | 15 | 15 | |
| $I_{DD3N}$ | **(Active standby current)**<br>/CS ≥ $V_{IH\ min}$; CKE ≥ $V_{IH\ min}$; One Bank Active-Precharge;<br>$t_{RC}$ = $t_{RAS\ max}$; $t_{CK}$ = $t_C$K min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle. | 30 | 30 | |
| $I_{DD4R}$ | **(Operating current)**<br>Burst = 2; Reads; Continuous burst; One Bank Active;<br>Address and control inputs changing once per clock cycle;<br>CL=2; $t_{CK}$ = $t_{CK\ min}$; $I_{OUT}$ = 0mA. | 100 | 90 | |
| $I_{DD4W}$ | **(Operating current)**<br>Burst = 2; Write; Continuous burst; One Bank Active;<br>Address and control inputs changing once per clock cycle;<br>CL = 2; $t_{CK}$ = $t_{CK}$ min;<br>DQ, DM and DQS inputs changing twice per clock cycle. | 95 | 85 | |
| $I_{DD5}$ | **(Auto Refresh current)**<br>$t_{RC}$ = $t_{RFC}$ min. | 60 | 60 | |
| $I_{DD6}$ | **(Self Refresh current)**<br>CKE ≤ 0.2V; external clock on; $t_{CK}$ = $t_{CK\ min}$. | 2 | 2 | |
| $I_{DD7}$ | **(Random Read current)**<br>4 Banks Active Read with activate every 20nS; Auto-Precharge Rea<br>every 20 nS; Burst = 4; $t_{RCD}$ = 3; $I_{OUT}$ = 0mA;<br>DQ, DM and DQS inputs changing twice per clock cycle;<br>Address changing once per clock cycle. | 110 | 100 | |

***Note 1:*** These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of tCK and tRC.

***Note 2:*** These parameters depend on the output loading. Specified values are obtained with the output open.

## *Block Diagram*

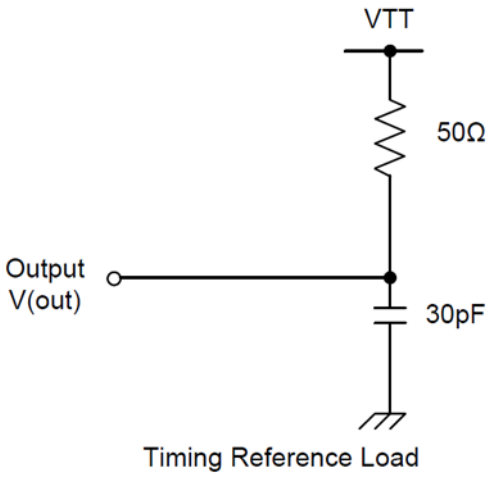



NOTE : The cell array configuration is 4096 * 256 * 16

## *AC Operating Test Conditions*

($V_{DD}$=2.5V±0.2V, $T_A$=0°C ~70°C)

| Item | Conditions |
|---|---|
| $V_{IH\ (AC)}$, Input High Voltage (AC) | VREF + 0.31 |
| $V_{IL\ (AC)}$, Input Low Voltage (AC) | VREF - 0.31 |
| Input Reference Voltage | 0.5 x VDDQ |
| Termination Voltage | 0.5 x VDDQ |
| $V_{X\ (AC)}$, Differential Clock Input Reference Voltage | Vx (AC) |
| $V_{ID\ (AC)}$, Input Difference Voltage. CLK and CLK Inputs (AC) | 1.5 |
| Output Timing Measurement Reference Voltage | 0.5 x VDDQ |



## AC Characteristics

($V_{DD}$=2.5V±0.2V, $T_A$=0°C ~70°C)

| Symbol | Parameter | 400 MHz | | 333 MHz | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WPRE}$ | DQS Write Preamble Time ***(Note1)*** | 0.25 | | 0.25 | | $t_{CK}$ |
| $t_{WPST}$ | DQS Write Postamble Time ***(Note1)*** | 0.4 | 0.6 | 0.4 | 0.6 | |
| $t_{DQSS}$ | Write Command to First DQS Latching Transition ***(Note1)*** | 0.72 | 1.25 | 0.72 | 1.25 | |
| $t_{IS}$ | Input Setup Time (fast slew rate) ***(Note5,Note7-9)*** | 0.6 | | 0.6 | | ns |
| $t_{IH}$ | Input Hold Time (fast slew rate) ***(Note5,Note7-9)*** | 0.6 | | 0.6 | | |
| $t_{IS}$ | Input Setup Time (slow slew rate) ***(Note6-9)*** | 0.7 | | 0.7 | | |
| $t_{IH}$ | Input Hold Time (slow slew rate) ***(Note6-9)*** | 0.7 | | 0.7 | | |
| $t_{IPW}$ | Control & Address Input Pulse Width (for each input) | 2.2 | | 2.2 | | |
| $t_{HZ}$ | Data-out High-impedance Time from CLK, /CLK | | 0.7 | | 0.7 | |
| $t_{LZ}$ | Data-out Low-impedance Time from CLK, /CLK | -0.7 | 0.7 | -0.7 | 0.7 | |
| $t_{T(SS)}$ | SSTL Input Transition | 0.5 | 1.5 | 0.5 | 1.5 | |
| $t_{WTR}$ | Internal Write to Read Command Delay | 2 | | 1 | | $t_{CK}$ |
| $t_{XSNR}$ | Exit Self Refresh to non-Read Command | 75 | | 75 | | ns |
| $t_{XSRD}$ | Exit Self Refresh to Read Command | 200 | | 200 | | $t_{CK}$ |
| $t_{REFi}$ | Refresh Interval Time (4K/64mS) ***(Note3)*** | | 15.6 | | 15.6 | µS |
| $t_{REFiA}$ | Refresh Interval Time (4K/16mS) ***(Note3)*** | | 3.9 | | | |
| $t_{MRD}$ | Mode Register Set Cycle Time | 10 | | 12 | | ns |
| $t_{RC}$ | Active to Ref/Active Command Period | 55 | | 50 | | ns |
| $t_{RFC}$ | Ref to Ref/Active Command Period | 70 | | 70 | | |
| $t_{RAS}$ | Active to Precharge Command Period | 40 | 70K | 42 | 100K | |
| $t_{RCD}$ | Active to Read/Write Command Delay Time | 15 | | 18 | | |
| $t_{RAP}$ | Active to Read with Auto-precharge Enable | 15 | | 18 | | |
| $t_{CCD}$ | Read/Write(a) to Read/Write(b) Command Period | 1 | | 1 | | $t_{CK}$ |
| $t_{RP}$ | Precharge to Active Command Period | 15 | | 18 | | ns |
| $t_{RRD}$ | Active(a) to Active(b) Command Period | 10 | | 10 | | |
| $t_{WR}$ | Write Recovery Time | 15 | | 15 | | |
| $t_{DAL}$ | Auto-precharge Write Recovery + Precharge Time ***(Note4)*** | (tWR/tCK) + (tRP/tCK) | | (tWR/tCK) + (tRP/tCK) | | |

## AC Characteristics (Continued)

($V_{DD}$=2.5V±0.2V, $T_A$=0°C ~70°C)

| Symbol | Parameter | | 400 MHz | | 333 MHz | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{CK}$ | CLK Cycle Time | CL=2.5 | - | - | 6 | 10 | ns |
| | | CL=3 | 4 | 10 | 5 | 10 | |
| $t_{AC}$ | Data Access Time from CLK, /CLK ***(Note2)*** | | -0.7 | 0.7 | -0.7 | 0.7 | |
| $t_{DQSCK}$ | DQS Output Access Time from CLK, /CLK ***(Note2)*** | | -0.6 | 0.6 | -0.6 | 0.6 | |
| $t_{DQSQ}$ | Data Strobe Edge to Output Data Edge Skew | | | 0.4 | | 0.4 | |
| $t_{CH}$ | CLk High Level Width | | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ |
| $t_{CL}$ | CLK Low Level Width | | 0.45 | 0.55 | 0.45 | 0.55 | |
| $t_{HP}$ | CLK Half Period (minimum of actual tCH, tCL) | | min, (tCL, tCH) | | min, (tCL, tCH) | | ns |
| $t_{QH}$ | DQ Output Data Hold Time from DQS | | HP-05 | | HP-05 | | |
| $t_{RPRE}$ | DQS Read Preamble Time | | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ |
| $t_{RPST}$ | DQS Read Postamble Time | | 0.4 | 0.6 | 0.4 | 0.6 | |
| $t_{DS}$ | DQ and DM Setup Time | | 0.4 | | 0.4 | | ns |
| $t_{DH}$ | DQ and DM Hold Time | | 0.4 | | 0.4 | | |
| $t_{DIPW}$ | DQ and DM Input Pulse Width (for each input) | | 1.75 | | 1.75 | | |
| $t_{DQSH}$ | DQS Input High Pulse Width | | 0.35 | | 0.35 | | $t_{CK}$ |
| $t_{DQSL}$ | DQS Input Low Pulse Width | | 0.35 | | 0.35 | | $t_{CK}$ |
| $t_{DSS}$ | DQS Falling Edge to CLK Setup Time | | 0.2 | | 0.2 | | $t_{CK}$ |
| $t_{DSH}$ | DQS Falling Edge Hold Time from CLK | | 0.2 | | 0.2 | | $t_{CK}$ |
| $t_{WPRES}$ | Clock to DQS Write Preamble Set-up Time | | 0 | | 0 | | ns |

***Note 1:*** IF the result of nominal calculation with regard to Tck contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., $t_{DQSS}$ = 1.25 x $t_{CK}$, $t_{CK}$ = 5 nS, 1.25 x 5 nS = 6.25 nS is rounded up to 6.2 nS.)

***Note 2:*** $t_{AC}$ and $t_{DQSCK}$ depend on the clock jitter. These timing are measured at stable clock.

***Note 3:*** A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

***Note 4:*** $t_{DAL}$ = ($t_{WR}$/$t_{CK}$) + ($t_{RP}$/$t_{CK}$)
For each of the terms above, if not already an integer, round to the next highest integer.
Example: For -5 speed grade at CL=2.5 and $t_{CK}$=6 nS
$t_{DAL}$ = ((15 nS / 6 nS) + (15 nS / 6 nS)) clocks = ((3) + (3)) clocks = 6 clocks

***Note 5:*** For command/address input slew rate ≥1.0 V/nS.

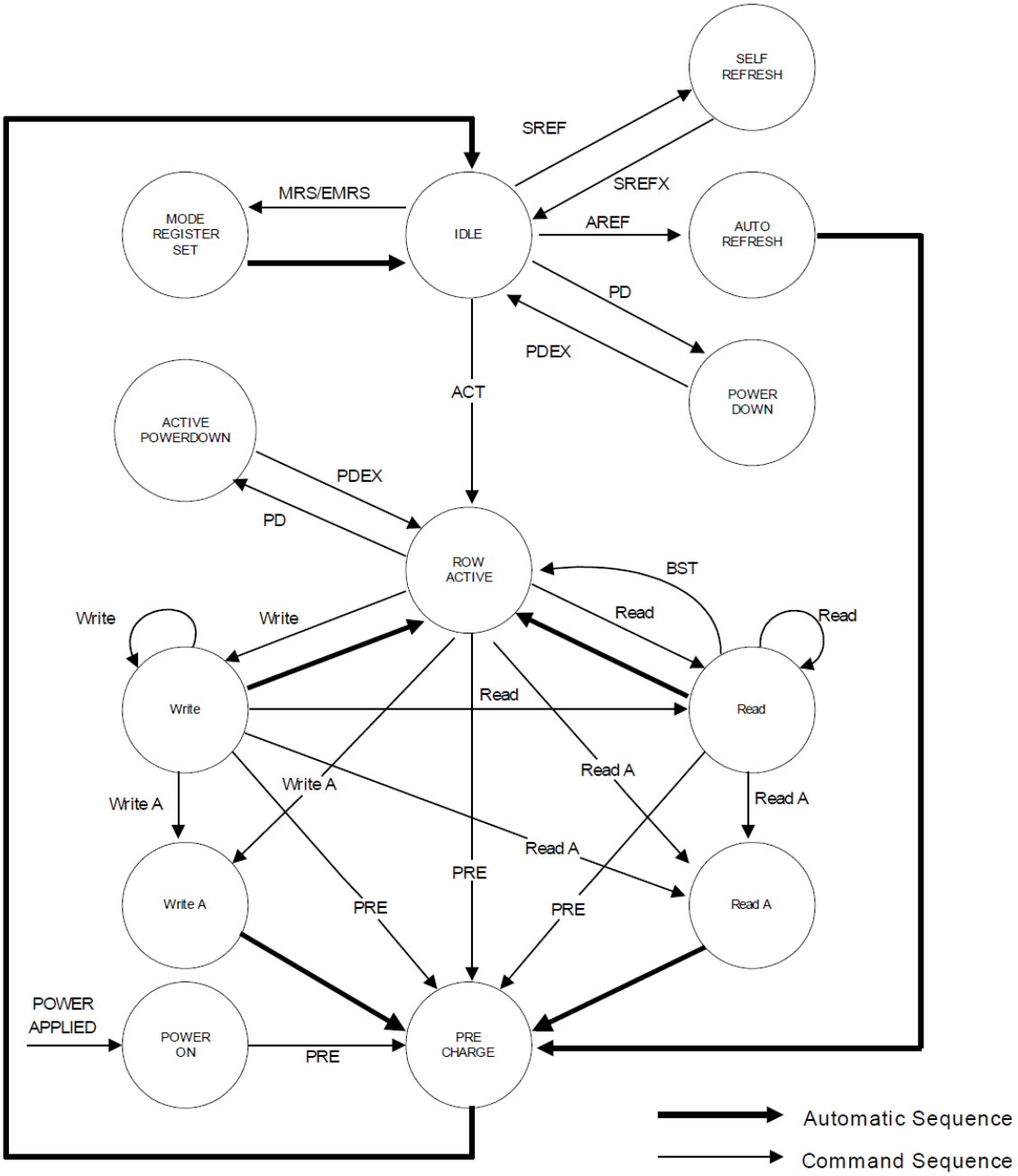
***Note 6:*** For command/address input slew rate ≥0.5 V/nS and <1.0 V/nS.

***Note 7:*** For CLK & /CLK slew rate ≥1.0 V/nS (single--ended).

***Note 8:*** These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

***Note 9:*** Slew Rate is measured between $V_{OH}$(ac) and $V_{OL}$(ac).

## *Simplified State Diagram*



## Command Truth Table

| Command | Symbol | CKE | | /CS | /RAS | /CAS | /WE | BA0, BA1 | A10 | A11~A0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | n-1 | n | | | | | | | |
| Ignore Command | DESL | H | X | H | X | X | X | X | X | X |
| No Operation | NOP | H | X | L | H | H | H | X | X | X |
| Burst Stop | BSTH | H | X | L | H | H | L | X | X | X |
| Read | READ | H | X | L | H | L | H | V | L | V |
| Read with Auto Pre-charge | READA | H | X | L | H | L | H | V | H | V |
| Write | WRIT | H | X | L | H | L | L | V | L | V |
| Write with Auto Pre-charge | WRITA | H | X | L | L | H | H | V | H | V |
| Bank Activate | ACT | H | X | L | L | H | H | V | V | V |
| Pre-charge Select Bank | PRE | H | X | L | L | H | L | V | L | X |
| Pre-charge All Banks | PALL | H | X | L | L | H | L | X | H | X |
| Mode Register Set | MRS | H | X | L | L | L | L | L | L | V |

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

## CKE Truth Table

| Item | Command | CKE | | /CS | /RAS | /CAS | /WE | Addr. |
|---|---|---|---|---|---|---|---|---|
| | | n-1 | n | | | | | |
| Idle | CBR Refresh Command | H | H | L | L | L | H | X |
| Idle | Self Refresh Entry | H | L | L | L | L | H | X |
| Self Refresh | Self Refresh Exit | L | H | L | H | H | H | X |
| | | L | H | H | X | X | X | X |
| Idle | Power Down Entry | H | L | X | X | X | X | X |
| Power Down | Power Down Exit | L | H | X | X | X | X | X |

H = High level, L = Low level, X = High or Low level (Don't care)

## 3. Operative Command Table

| Current State | /CS | /R | /C | /W | Addr. | Command | Action |
|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X | DSL | Nop |
| | L | H | H | X | X | NOP/BST | Nop |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL ***(Note 2)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL ***(Note 2)*** |
| | L | L | H | H | BA,RA | ACT | Row activating |
| | L | L | H | L | BA, A10 | PRE/PALL | Nop |
| | L | L | L | H | X | REF/SELF | Refresh or self refresh ***(Note 1)*** |
| | L | L | L | L | Op-Code | MRS/EMRS | Mode register accessing ***(Note 1)*** |
| Row Active | H | X | X | X | X | DSL | Nop |
| | L | H | H | X | X | NOP/BST | Nop |
| | L | H | L | H | BA,CA,A10 | READ/READA | Begin read: Determine AP ***(Note 3)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Begin write: Determine AP ***(Note 3)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | Pre-charge ***(Note 4)*** |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Read | H | X | X | X | X | DSL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | Burst stop |
| | L | H | L | H | BA,CA,A10 | READ/READA | Terminate burst, new read: Determine AP ***(Note 5)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | Terminate burst, pre-charging |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Write | H | X | X | X | X | DSL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | Term burst, start read: Determine AP ***(Note 5,6)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Term burst, start read: Determine AP ***(Note 5)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | Term burst, Precharging ***(Note 7)*** |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |

H = High level, L = Low level, X = High or Low level (Don't care)

## 3. Operative Command Table (Continued)

| Current State | /CS | /R | /C | /W | Addr. | Command | Action |
|---|---|---|---|---|---|---|---|
| Read with AP | H | X | X | X | X | DSL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL ***(Note 2)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Write with AP | H | X | X | X | X | DSL | Continue burst to end |
| | L | H | H | H | X | NOP | Continue burst to end |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL ***(Note 2)*** |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Pre-charging | H | X | X | X | X | DSL | NOP-> Idle after tRP |
| | L | H | H | H | X | NOP | NOP-> Idle after tRP |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL ***(Note 2)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL ***(Note 2)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | Idle after tRP |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Row Activating | H | X | X | X | X | DSL | NOP-> Row active after tRCD |
| | L | H | H | H | X | NOP | NOP-> Row active after tRCD |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL ***(Note 2)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL ***(Note 2)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL ***(Note 2)*** |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

## 3. Operative Command Table (Continued)

| Current State | /CS | /R | /C | /W | Addr. | Command | Action |
|---|---|---|---|---|---|---|---|
| Write Recovering | H | X | X | X | X | DSL | NOP->Row active after tWR |
| | L | H | H | H | X | NOP | NOP->Row active after tWR |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL ***(Note 2)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL ***(Note 2)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL ***(Note 2)*** |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Write Recovering with AP | H | X | X | X | X | DSL | NOP->Enter precharge after tWR |
| | L | H | H | H | X | NOP | NOP->Enter precharge after tWR |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL ***(Note 2)*** |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL ***(Note 2)*** |
| | L | L | H | H | BA,RA | ACT | ILLEGAL ***(Note 2)*** |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL ***(Note 2)*** |
| | L | L | L | H | X | AREF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL |
| Refreshing | H | X | X | X | X | DSL | NOP->Idle after tRC |
| | L | H | H | H | X | NOP | NOP->Idle after tRC |
| | L | H | L | L | X | BST | ILLEGAL |
| | L | H | H | H | X | READ/WRIT | ILLEGAL |
| | L | L | L | X | X | ACT/PRE/PREA | ILLEGAL |
| | L | L | L | X | X | AREF/SELF/MRS/EMRS | ILLEGAL |
| Mode Register Accessing | H | X | X | X | X | DSL | NOP->Row after tMRD |
| | L | H | H | H | X | NOP | NOP->Row after tMRD |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | X | X | READ/WRIT | ILLEGAL |
| | L | L | X | X | X | ACT/PRE/PALL/REF/SELF/MRS | ILLEGAL |

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

***Note 1:*** Illegal if any bank is not idle.
***Note 2:*** Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
***Note 3:*** Illegal if tRCD is not satisfied.
***Note 4:*** Illegal if tRAS is not satisfied.
***Note 5:*** Must satisfy burst interrupt condition.
***Note 6:*** Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
***Note 7:*** Must mask preceding data which don't satisfy tWR

## 4. Command Truth Table for CKE

| Current State | CKE | | /CS | /RAS | /CAS | /WE | Addr. | Action |
|---|---|---|---|---|---|---|---|---|
| | n-1 | n | | | | | | |
| Self Refresh | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Self Refresh->Idle after tXSNR |
| | L | H | L | H | H | X | X | Exit Self Refresh->Idle after tXSNR |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | Maintain self refresh |
| Power Down | H | X | X | X | X | X | X | INVALID |
| | L | H | X | X | X | X | X | Exit Power down->Idle after tIS |
| | L | L | X | X | X | X | X | Maintain power down mode |
| All banks Idle | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | H | X | X | X | X | Enter Power down ***(Notes 2)*** |
| | H | L | L | H | H | X | X | Enter Power down ***(Notes 2)*** |
| | H | L | L | L | L | H | X | Self Refresh ***(Notes 1)*** |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | X | X | X | ILLEGAL |
| | L | X | X | X | X | X | X | Power down |
| Row Active | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | H | X | X | X | X | Enter Power down ***(Notes 3)*** |
| | H | L | L | H | H | X | X | Enter Power down ***(Notes 3)*** |
| | H | L | L | L | L | H | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | X | X | X | ILLEGAL |
| | L | X | X | X | X | X | X | Power down |
| Any State Other than Listed above | H | H | X | X | X | X | X | Refer to Function Truth Table |

H = High level, L = Low level, X = High or Low level (Don't care)

***Notes 1:*** Self refresh can enter only from the all banks idle state.

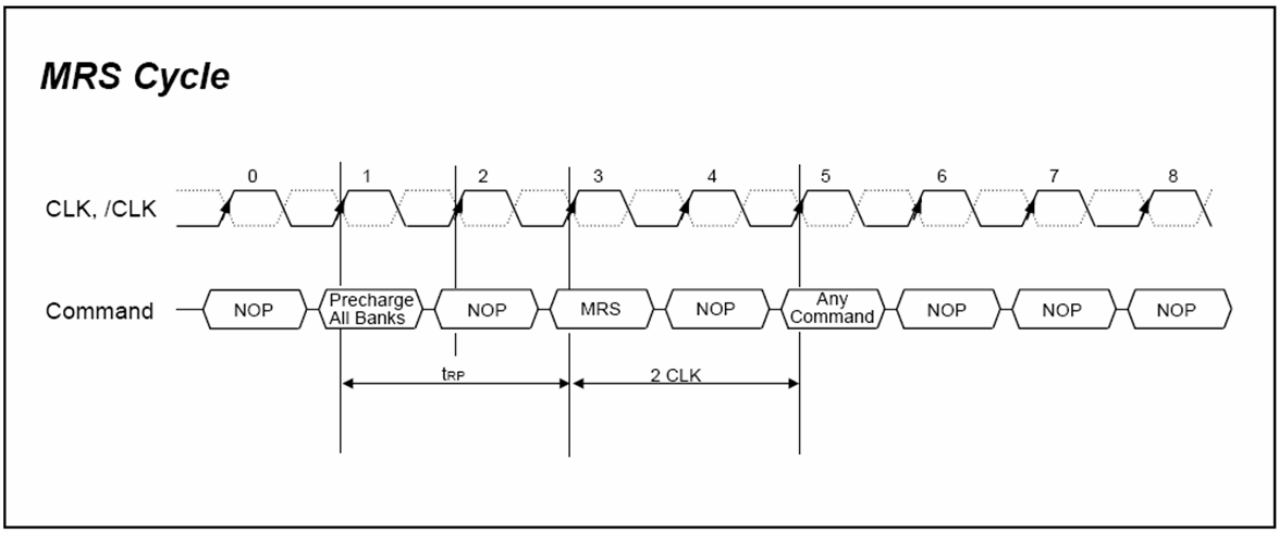
***Notes 2:*** Power Down occurs when all banks are idle; this mode is referred to as precharge power down.

***Notes 3:*** Power Down occurs when there is a row active in any bank; this mode is referred to as active power down.

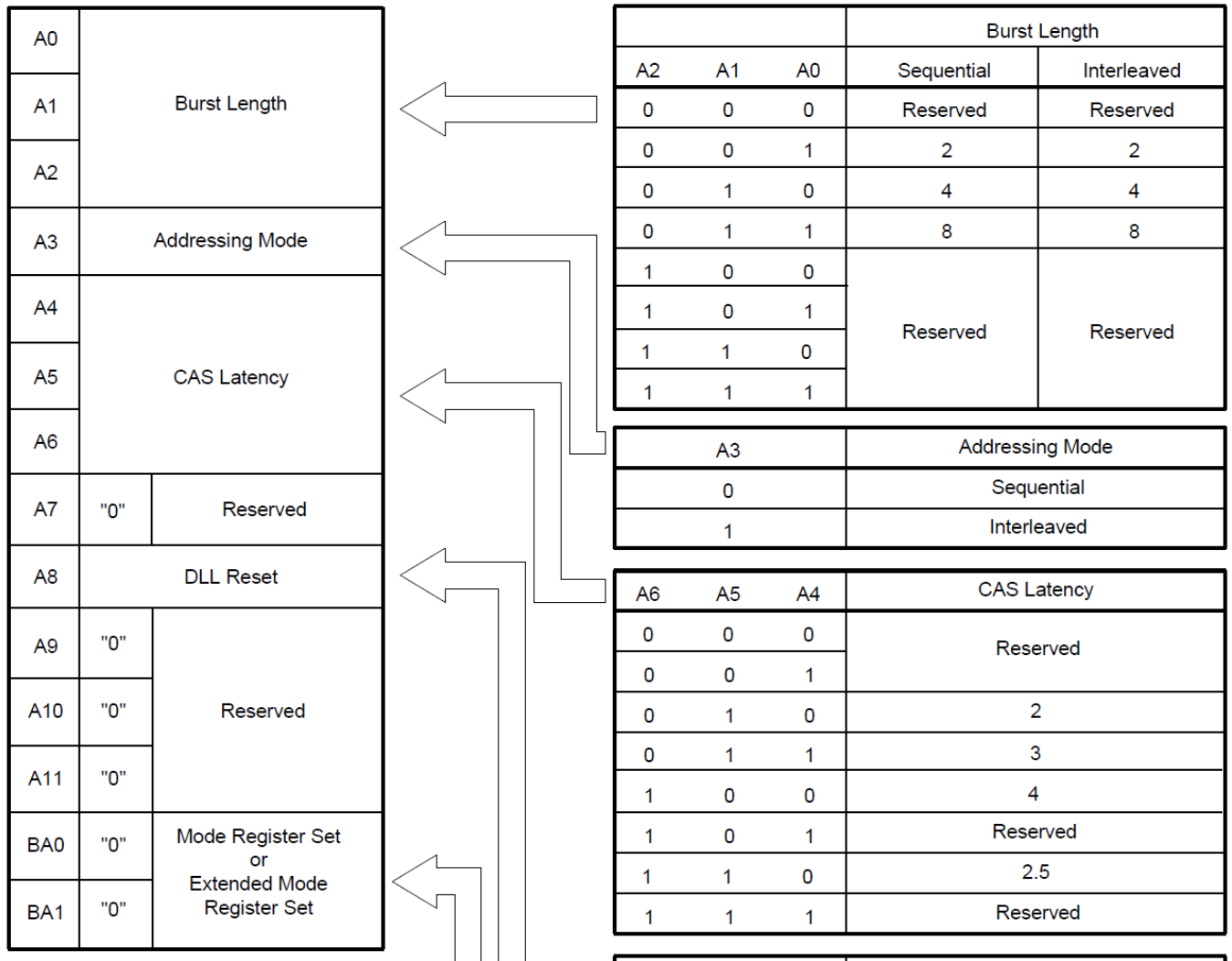
## Mode Register Definition

### Mode Register Set

The mode register stores the data for controlling the various operating modes of DDR SDRAM which contains addressing mode, burst length, /CAS latency, test mode, DLL reset and various vendor’ s specific opinions. The defaults values of the register is not defined, so the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0 ( The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. ) The state of the address pins A0-A11 in the same cycle as /CS, /RAS, /CAS, /WE and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operating as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, addressing mode uses A3, /CAS latency ( read latency from column address ) uses A4-A6. A7 is used for test mode. A8 is used for DDR reset. A7 must be set to low for normal MRS operation.



## *Address input for Mode Register Set*



| | | |
|---|---|---|
| A0 | Burst Length | |
| A1 | | |
| A2 | | |
| A3 | Addressing Mode | |
| A4 | CAS Latency | |
| A5 | | |
| A6 | | |
| A7 | "0" | Reserved |
| A8 | DLL Reset | |
| A9 | "0" | Reserved |
| A10 | "0" | |
| A11 | "0" | |
| BA0 | "0" | Mode Register Set or Extended Mode Register Set |
| BA1 | "0" | |

* "Reserved" should stay "0" during MRS cycle.

| | | | Burst Length | |
|---|---|---|---|---|
| A2 | A1 | A0 | Sequential | Interleaved |
| 0 | 0 | 0 | Reserved | Reserved |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

| A3 | Addressing Mode |
|---|---|
| 0 | Sequential |
| 1 | Interleaved |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | 2.5 |
| 1 | 1 | 1 | Reserved |

| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| BA1 | BA0 | MRS or EMRS |
|---|---|---|
| 0 | 0 | Regular MRS cycle |
| 0 | 1 | Extended MRS cycle |
| 1 | 0 | Reserved |
| 1 | 1 | |

## Burst Type (A3)

| Burst Length | A2 | A1 | A0 | Sequential Addressing | Interleave Addressing |
|---|---|---|---|---|---|
| 2 | X | X | 0 | 0 1 | 0 1 |
| | X | X | 0 | 1 0 | 1 0 |
| 4 | X | 0 | 0 | 0 1 2 3 | 0 1 2 3 |
| | X | 0 | 1 | 1 2 3 0 | 1 0 3 2 |
| | X | 1 | 0 | 2 3 0 1 | 2 3 0 1 |
| | X | 1 | 1 | 3 0 1 2 | 3 2 1 0 |
| 8 | 0 | 0 | 0 | 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 |
| | 0 | 0 | 1 | 1 2 3 4 5 6 7 0 | 1 0 3 2 5 4 7 6 |
| | 0 | 1 | 0 | 2 3 4 5 6 7 0 1 | 2 3 0 1 6 7 4 5 |
| | 0 | 1 | 1 | 3 4 5 6 7 0 1 2 | 3 2 1 0 7 6 5 4 |
| | 1 | 0 | 0 | 4 5 6 7 0 1 2 3 | 4 5 6 7 0 1 2 3 |
| | 1 | 0 | 1 | 5 6 7 0 1 2 3 4 | 5 4 7 6 1 0 3 2 |
| | 1 | 1 | 0 | 6 7 0 1 2 3 4 5 | 6 7 4 5 2 3 0 1 |
| | 1 | 1 | 1 | 7 0 1 2 3 4 5 6 | 7 6 5 4 3 2 1 0 |

*Page length is a function of I/O organization and column addressing

## DLL Enable / Disable

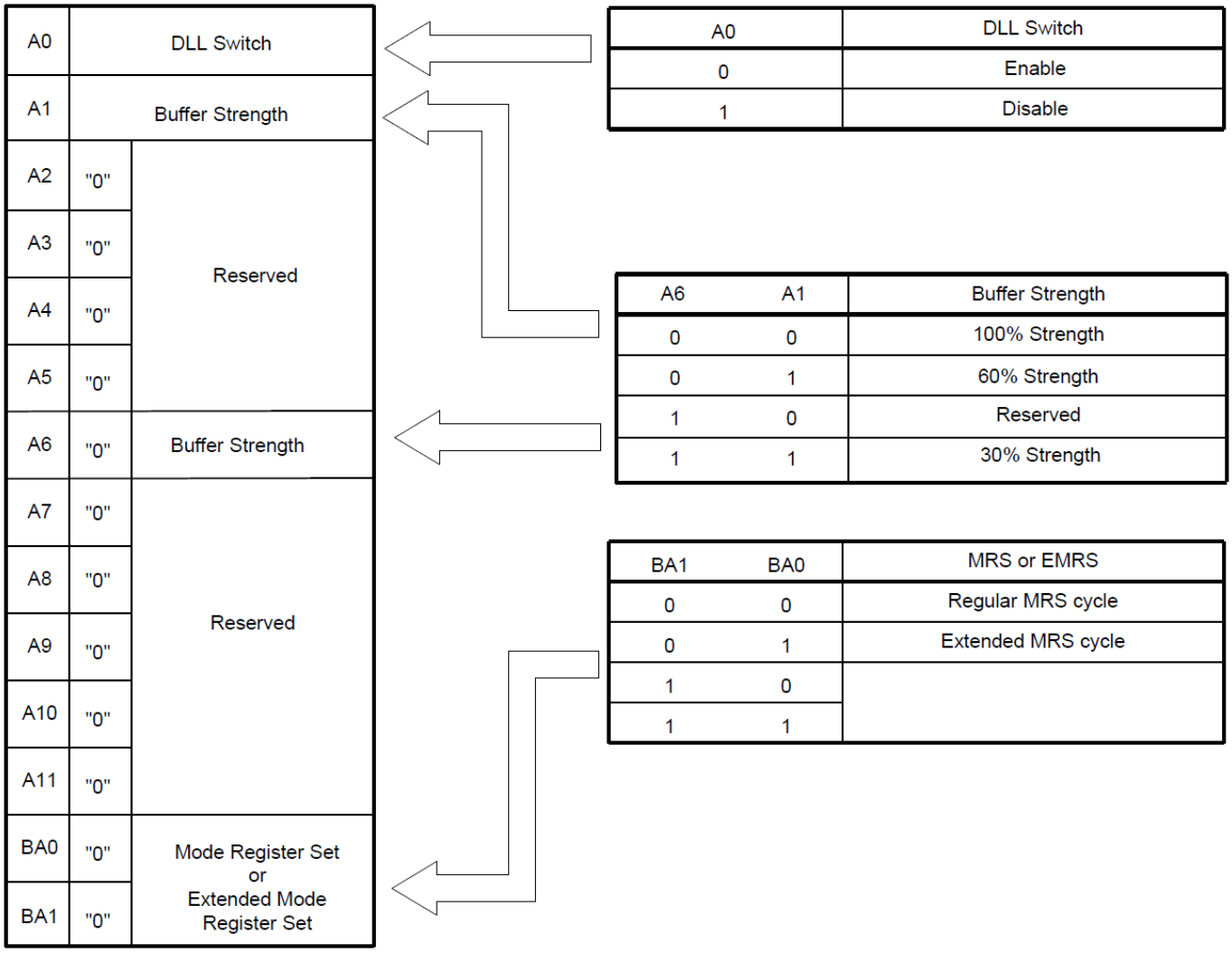
The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disable the DLL for the purpose of debug or evaluation ( upon existing Self Refresh Mode, the DLL is enable automatically. ) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

## Output Drive Strength

The normal drive strength got all outputs is specified to be SSTL-2, Class II. Some vendors might also support a weak drive strength option, intended for lighter load and/or point to point environments.

## *Extended Mode Register Set ( EMRS )*

The Extended mode register stores the data enabling or disabling DLL. The value of the extended mode register is not defined, so the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA0 ( The DDR SDRAM should be in all bank precharge with CKE already prior to writing into the extended mode register. ) The state of address pins A0-A10 and BA1 in the same cycle as /CS, /RAS, /CAS, and /WE going low is written in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. High on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation.

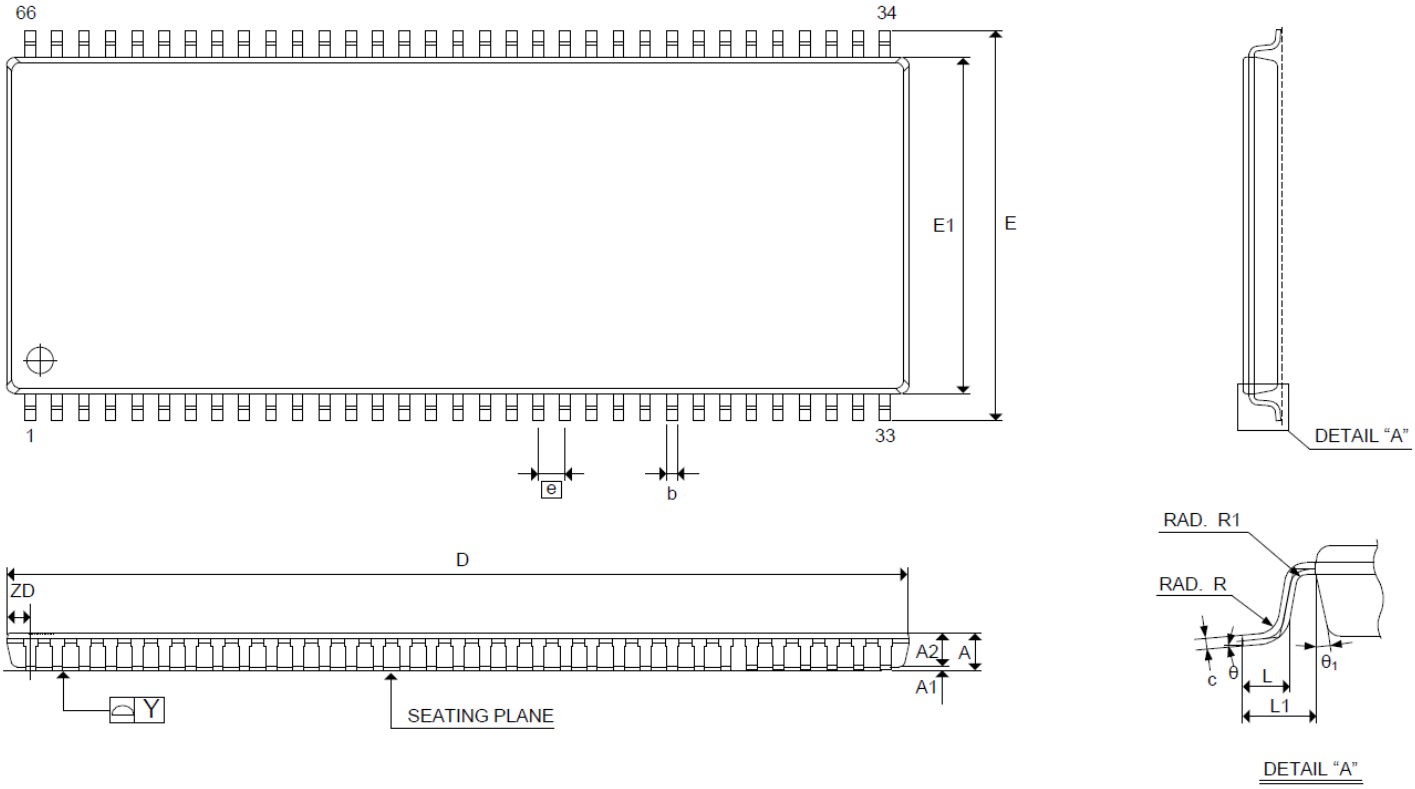



| A0 | DLL Switch |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A6 | A1 | Buffer Strength |
|---|---|---|
| 0 | 0 | 100% Strength |
| 0 | 1 | 60% Strength |
| 1 | 0 | Reserved |
| 1 | 1 | 30% Strength |

| BA1 | BA0 | MRS or EMRS |
|---|---|---|
| 0 | 0 | Regular MRS cycle |
| 0 | 1 | Extended MRS cycle |
| 1 | 0 | |
| 1 | 1 | |

## *Package Description*




Controlling Dimension : Millimeters

| SYMBOL | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | --- | --- | 1.20 | --- | --- | 0.047 |
| A1 | 0.05 | --- | 0.15 | 0.002 | --- | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.22 | --- | 0.38 | 0.009 | --- | 0.015 |
| c | 0.12 | --- | 0.21 | 0.005 | --- | 0.008 |
| D | 22.09 | 22.22 | 22.35 | 0.870 | 0.875 | 0.880 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 0.65 BASIC | | | 0.026 BASIC | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.80 BASIC | | | 0.031 BASIC | | |
| R | 0.12 | --- | 0.25 | 0.005 | --- | 0.010 |
| R1 | 0.12 | --- | --- | 0.005 | --- | --- |
| ZD | 0.71 REF | | | 0.028 REF | | |
| θ | 0° | --- | 8° | 0° | --- | 8° |
| $\theta_1$ | 10° | --- | 20° | 10° | --- | 20° |
| Y | --- | --- | 0.10 | --- | --- | 0.004 |

## *Revision History*

| Revision No. | History | Draft Date | Editor | Remark |
|---|---|---|---|---|
| 0.1 | Initial Release. | Dec. 2014 | Jon Hsu | N/A |
| 1.0 | First SPEC. release. | Dec. 2014 | Jon Hsu | N/A |