*64Mb (512K*x*4Banks×32) Synchronous SDRAM*

Descriptions

The H2A164M3233N is Synchronous Dynamic Random Access Memory (SDRAM) organized as 512K words x 4 banks by 32 bits. All inputs and outputs are synchronized with the positive edge of the clock.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

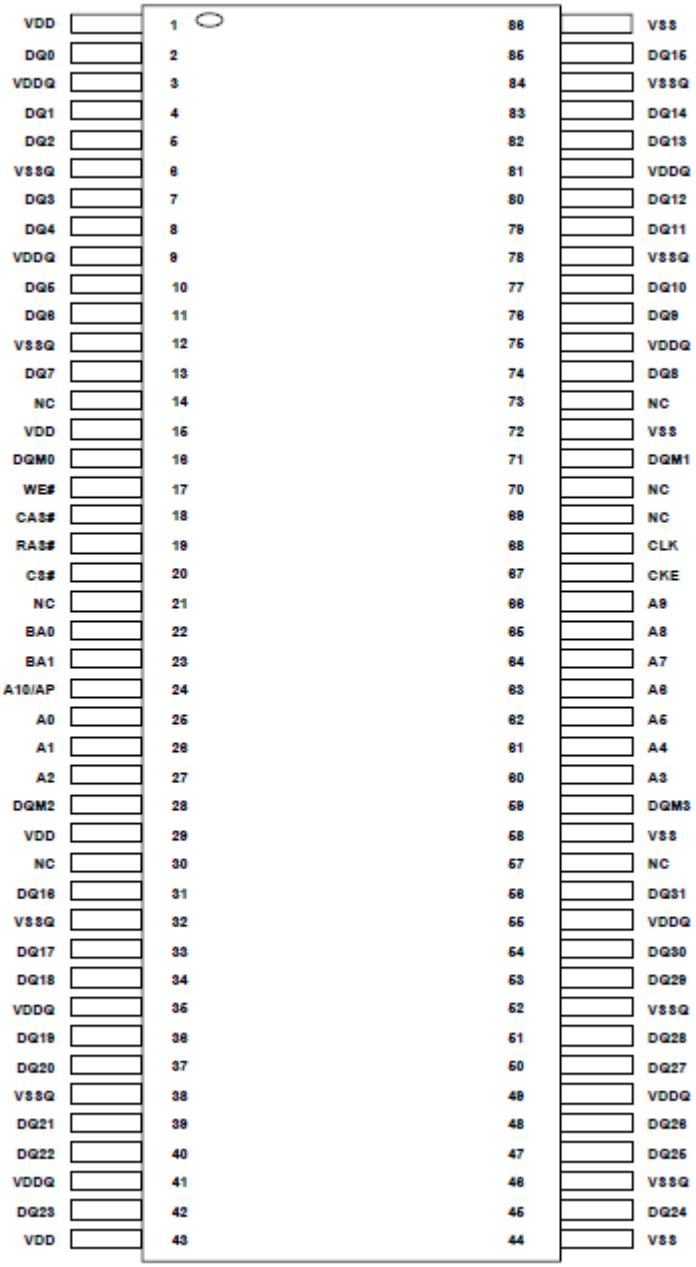
Features

- 512K Words × 4 banks × 32 bits organization
- Single 3.3V±0.3V Power Supply
- Self Refresh Mode
- CAS Latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and full page
- Burst Read, Single Writes Mode
- Byte Data Controlled by DQM
- Auto-precharge and Controlled Precharge
- 4K Refresh cycles / 64 mS
- Interface: LVTTL
- Packaged in TSOP II 86 pin, 400x875 mil
- Pb and Halogen Free

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A164M3233NM1C	2M X 32	PC-166MHz (3-3-3)	86pin TSOP(II)	Commercial

Pin Assignment



Pin Description (Simplified)

Pin	Name	Function
25-27, 60-66, 24,	A0−A10	**(Address)** Multiplexed pins for row and column address. Row address: A0−A10. Column address: A0−A7. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
22, 23	BA0, BA1	**(Bank Select)** Select bank to activate during row address latch time, or bank to read/write during address latch time.
2,4,5,7,8,10,11, 13,74,76,77,79, 80,82,83,85,31, 33,34,36,37,39, 40,42,45,47,48, 50,51,53,54,56	DQ0−DQ31	**(Data Input/ Output)** Multiplexed pins for data input and output.
20	/CS	**(Chip Select)** Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
19	/RAS	**(Row Address Strobe)** Command input. When sampled at the rising edge of the clock, /RAS, /CAS and /WE define the operation to be executed.
18	/CAS	**(Column Address Strobe)** Referred to /RAS
17	/WE	**(Write Enable)** Referred to /RAS

Pin Description (Simplified)

Pin	Name	Function
16,71,28,59	DQM0~3	**(Input/Output Mask)** The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
68	CLK	**(Clock Inputs)** System clock used to sample inputs on the rising edge of clock.
67	CKE	**(Clock Enable)** CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
1,15,29,43	V_{DD}	**(Power)** Power for input buffers and logic circuit inside DRAM.
44,58,72,86	V_{SS}	**(Ground)** Ground for input buffers and logic circuit inside DRAM.
3,9,35,41,49, 55,75,81	V_{DDQ}	**(Power for I/O buffer)** Separated power from VDD, to improve DQ noise immunity.
6,12,32,38, 46,52,78, 84	V_{SSQ}	**(Ground for I/O Buffer)** Separated ground from VSS, to improve DQ noise immunity.
14,30,57, 69,70,73	NC	**(No Connection)** No connection.

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-1.0 ~ + 4.6		V
V_{DD}, V_{DDQ}	Power Supply Voltage	-1.0 ~ + 4.6		V
T_{OPR}	Operating Temperature Range	Commercial	0 ~ +70	°C
T_{STG}	Storage Temperature	-55~+150		˚C
P_D	Power Dissipation	1		W
I_{OUT}	Short Circuit Current	50		mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Capacitance (V_{CC}=3.3V, f=1MHz, T_A=25°C)

Symbol	Parameter	Min.	Max.	Units
C_I	Input Capacitance (A0 to A11, BS0,BS1, /CS, /RAS, /CAS , /WE, DQM, CKE)	2	4	pF
C_{IO}	Input/Output Capacitance	4	6	pF

Note: These parameters are periodically sampled and not 100% tested

Recommended DC Operating Conditions (T_A=-0°C ~+70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V_{IH}	Input High Voltage ***(Note 1)***	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage ***(Note 2)***	-0.3	-	0.8	V

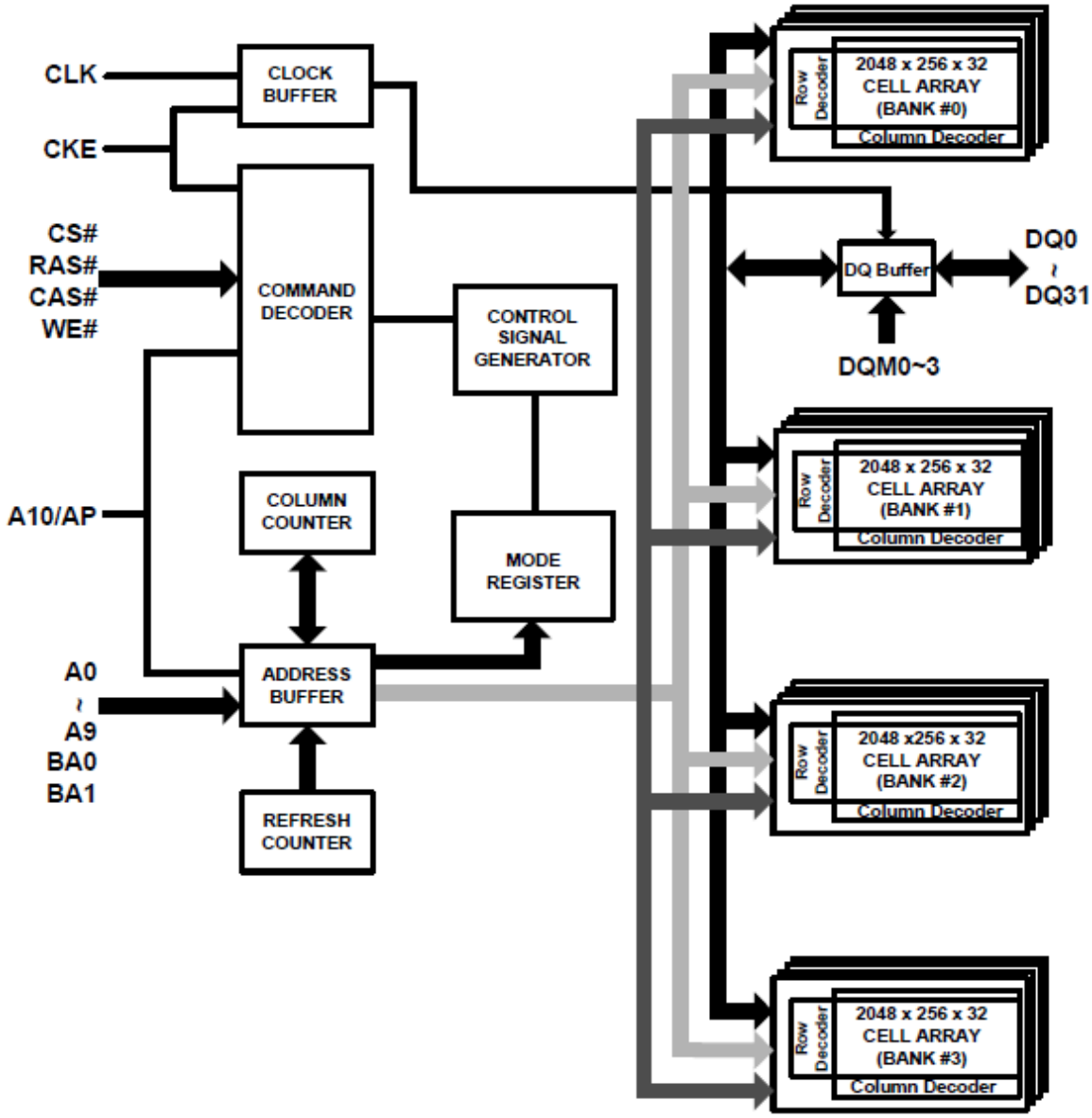
Note 1 : VIH (max.) = VDD/VDDQ+1.5V for pulse width ≤ 5 nS.
Note 2 : VIL (min.) = VSS/VSSQ-1.5V for pulse width ≤ 5 nS.

DC Characteristics

(V_{DD}=3.3V±0.3V, T_A=0°C ~ 70°C)

Symbol	Parameter	Test Conditions	PC-166MHz Max.	Units
I_{DD1}	Operating Current (One bank active) tRC ≥ tRC(min), Outputs Open, Input signal one transition per one cycle		95	mA
I_{DD2N}	Precharge Standby Current in non-power down mode tCK = 15ns, CS# ≥ VIH(min), CKE ≥ VIH Input signals are changed every 2clks		25	
I_{DD2NS}	Precharge Standby Current in non-power down mode tCK = ∞, CLK ≤ VIL(max), CKE ≥ VIH		15	
I_{DD2P}	Precharge Standby Current in power down mode tCK = 15ns, CKE ≤ VIL(max)		2	
I_{DD2PS}	Precharge Standby Current in power down mode tCK = ∞, CKE ≤ VIL(max)		2	
I_{DD3N}	Active Standby Current in non-power down mode tCK = 15ns, CKE ≥ VIH(min), CS# ≥ VIH(min) Input signals are changed every 2clks		35	
I_{DD3NS}	Active Standby Current in non-power down mode CKE≥ VIH(min), CLK ≤ VIL(max), tCK = ∞		30	
I_{DD4}	Operating Current (Burst mode) tCK =tCK(min), Outputs Open, Multi-bank interleave		100	
I_{DD5}	Refresh Current tRC ≥ tRC(min)		130	
I_{DD6}	Self Refresh Current CKE ≤ 0.2V ; for other inputs VIH≧VDD - 0.2V, VIL ≤ 0.2V		2	

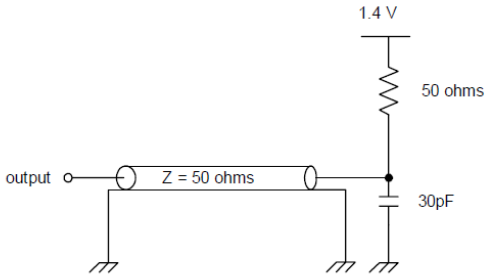
Block Diagram



AC Operating Test Conditions

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

Item	Conditions
Output Reference Level	1.4V/1.4V
Output Load	See diagram as below
Input Signal Level	2.4V/0.4V
Transition Time of Input Signals	1ns
Input Reference Level	1.4V



AC TEST LOAD

AC Characteristics

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

Symbol	Parameter		166 MHz		Units
			Min.	Max.	
T_{RC}	Row cycle time (same bank)		60	-	ns
T_{RCD}	RAS# to CAS# delay (same bank)		18	-	ns
T_{RP}	Precharge to refresh/row activate command (same bank)		18	-	ns
T_{RRD}	Row activate to row activate delay (different banks)		12	-	ns
T_{RAS}	Row activate to precharge time (same bank)		42	100K	ns
T_{WR}	Write recovery time		2	-	tck
T_{CCD}	CAS# to CAS# Delay time		1.0	-	tck
t_{CK}	Clock cycle time	CL*=2	-	6	ns
		CL*=3	-	5.4	ns
t_{CH}	Clock high time		2.5	-	ns
t_{CL}	Clock low time		2.5	-	ns
T_{AC}	Access time from CLK (positive edge)	CL*=2	-	6	ns
		CL*=3	-	5.4	ns
T_{OH}	Data output hold time		2.5	-	ns
T_{LZ}	Data output low impedance		1	-	ns
T_{HZ}	Data output high impedance	CL*=3	-	5.4	ns
T_{IS}	Data/Address/Control Input set-up time		1.5	-	ns
T_{IH}	Data/Address/Control Input hold time		1	-	ns
T_{PDE}	Power Down Exit set-up time		Tis+tck	-	ns
T_{REFI}	Average Refresh Interval Time		-	15.6	us

AC Characteristics (Continued)

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

Symbol	Parameter	166 MHz		Units
		Min.	Max.	
T_{XSR}	Exit Self-Refresh to Any Command	tRC+tIS	-	ns
T_{MRD}	Mode Register Set cycle time	2	-	tCK
t_{RFC}	Refresh cycle time	60	-	ns

* CL is CAS Latency.

Note 8: tHZ defines the time in which the outputs achieve the open circuit condition and are not at reference levels.
Note 9: If clock rising time is longer than 1 ns, (tR / 2 -0.5) ns should be added to the parameter.
Note 10: Assumed input rise and fall time tT (tR & tF) = 1 ns
If tR or tF is longer than 1 ns, transient time compensation should be considered, i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.

Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. (Like a conventional DRAM) During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed V_{DD}+0.3V on any of the input pins or V_{DD} supplies. (CLK signal started at same time) After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command.
To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

Address Input for Mode Register Set

BA0,1	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU*		WBL	Test Mode		CAS Latency			BT	Burst Length		

A9	Write Burst Length
0	Burst
1	Single Bit

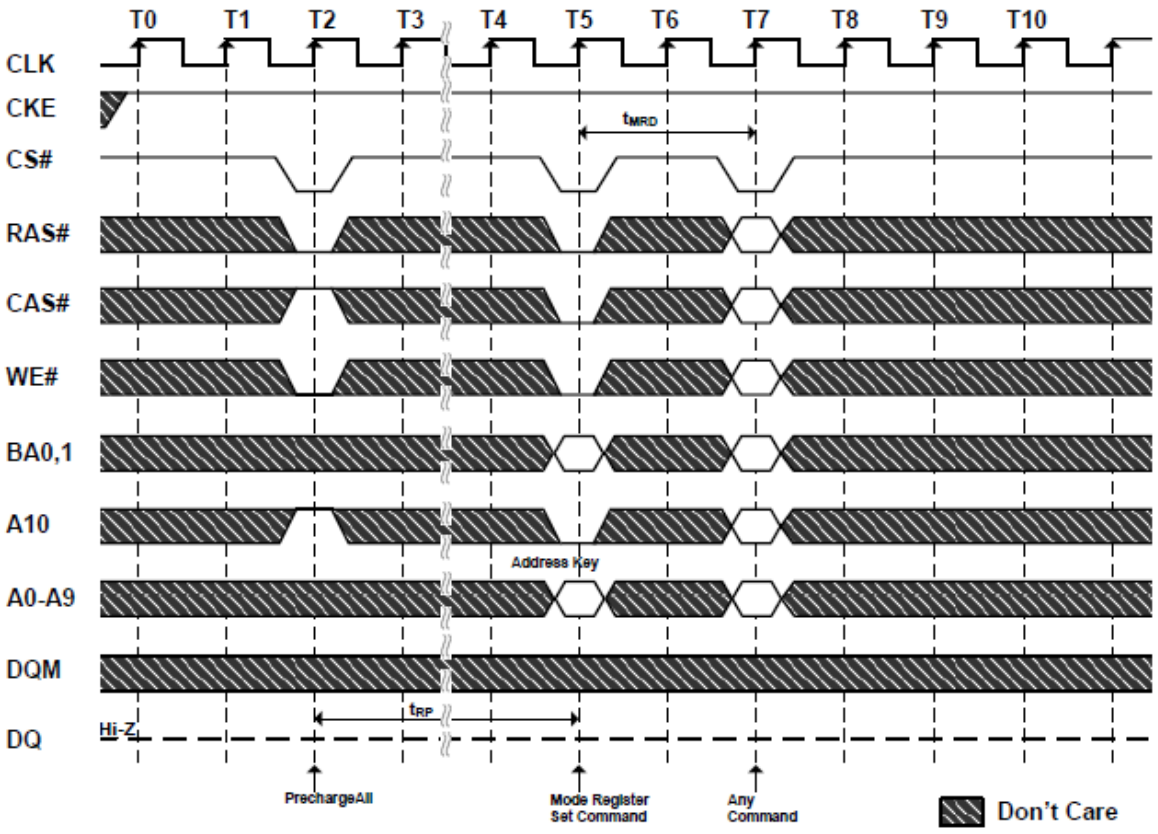
A8	A7	Test Mode
0	0	Normal
1	0	Vendor Use Only
0	1	Vendor Use Only

A3	Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
All other Reserved			

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	Full Page (Sequential)
All other Reserved			

*Note: RFU (Reserved for future use) should stay "0" during MRS cycle.



Burst Definition

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	1	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page*	n	n	n	Cn Cn+1 Cn+2……	-

* Page length is a function of I/O organization and column addressing □ 32 (CA0 ~ CA7): Full page = 256bits

Burst Length Field(A2~A0)

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

Burst Type Field

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency Field (A6~A4)

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 Clocks
0	1	1	3 Clocks
1	X	X	Reserved

Test Mode Field (A8~A7)

A8	A7	Test Mode
0	0	Normal Mode
0	1	Vendor Use only
1	X	Vendor Use only

Write Burst Length (A9)

A9	Write Burst Length
0	Burst-Read-Burst-Write
1	Burst-Read-Single-Write

No-Operation command

(RAS# = "H", CAS# = "H", WE# = "H")

The No-Operation command is used to perform a NOP to the SDRAM which is selected (CS# is Low). This prevents unwanted commands from being registered during idle or wait states.

Burst Stop command

(RAS# = "H", CAS# = "H", WE# = "L")

The Burst Stop command is used to terminate either fixed-length or full-page bursts. This command is only effective in a read/write burst without the auto precharge function.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 4 shows the truth table for the operation commands.

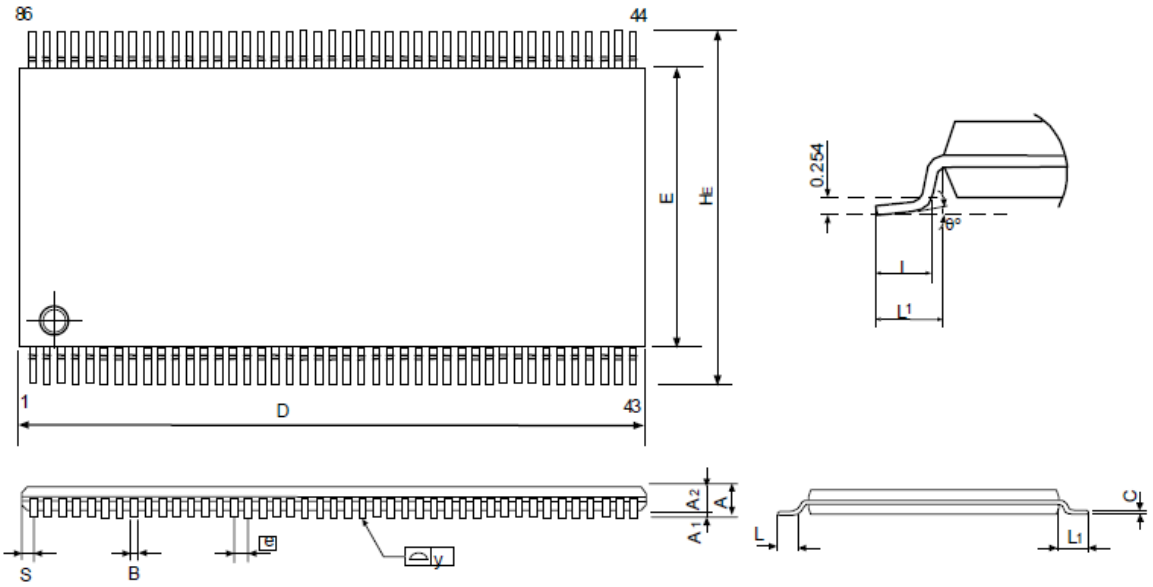
Truth Table

Command	State	CKE_{n-1}	CKE_n	DQM(6)	BA0,1	A10	A0-9	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	V	V	L	Column address (A0 ~ A7)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	V	V	H		L	H	L	L
Read	Active(3)	H	X	V	V	L	Column address (A0 ~ A7)	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	V	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	H	X	X	X
								L	V	V	V
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note :

1. V = Valid, X = Don't care, L = Logic low, H = Logic high
2. CKE_n signal is input level when commands are provided.
   CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
   When this command is asserted in the burst cycle, device state is clock suspend mode.
6. DQM0-3

86 Pin TSOP II Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Normal	Max	Min	Normal	Max
A	—	—	0.047	—	—	1.20
A1	0.002	0.004	0.008	0.05	0.10	0.2
A2	0.035	0.039	0.043	0.9	1	1.1
B	0.007	0.009	0.011	0.17	0.22	0.27
C	—	0.005	—	—	0.127	—
D	0.87	0.875	0.88	22.09	22.22	22.35
E	0.395	0.400	0.405	10.03	10.16	10.29
e	—	0.0197	—	—	0.50	—
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.0315	—	—	0.80	—
S	—	0.024	—	—	0.61	—
y	—	—	0.004	—	—	0.10
θ	0°	—	8°	0°	—	8°

Notes:

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension: mm

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Apr. 2018	Rico Yang	N/A
1.0	First SPEC. release.	Apr. 2018	Rico Yang	N/A