HAA1CG35111S

64GB e•MMC

Datasheet

V1.0

Introduction

General Description

AXEME eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a sim- ple read and write to memory using MMC protocol v5.1 which is a industry standard.

eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VCC) whereas 1.8V or 3V dual supply voltage (VCCQ) is supported for the MMC controller. AXEME eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance.

There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Axeme NAND flash and achieves optimal performance.

Product List

Capacity	Part Number	NAND Flash Type	Package Size	Package Type
64 GB	HAA1CG35111S	128Gbx 4	11.5x13x1.0 (mm)	153 FBGA

Key Feature

e•MMC v5.1 compatible. Detail description is referenced by JEDEC Standard

- (Backward compatible to e•MMC v4.5 to v5.0)

Bus mode

- Data bus width: 1bit(default), 4bit and 8bit
- Data transfer rate: up to 400MB/s (HS400) @ 200MHz DDR with 8bit bus width
- MMC I/F Clock Frequency: 0~200MHz
- MMC I/F Boot Frequency: 0~52MHz
- Non-supported Features : Large Sector Size (4KB)

Operating Voltage Range

- V_{CC} (NAND/Core): 2.7V ~ 3.6V
- V_{CCQ} (CTRL/IO): 1.7V ~ 1.95V / 2.7V ~ 3.6V

Temperature

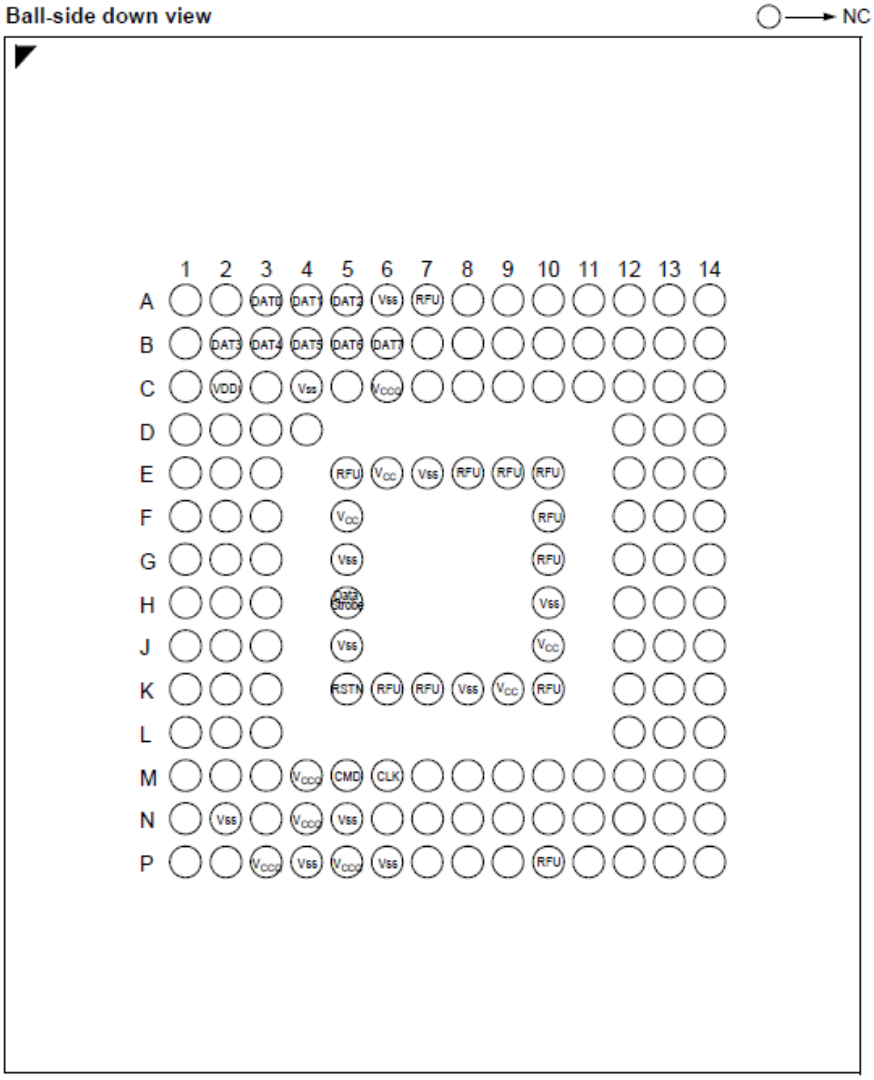
- Operation (-25℃ ~ 85℃)
- Storage without operation (-40℃ ~ 85℃)

Package Configurations

153-FBGA Ball Array View

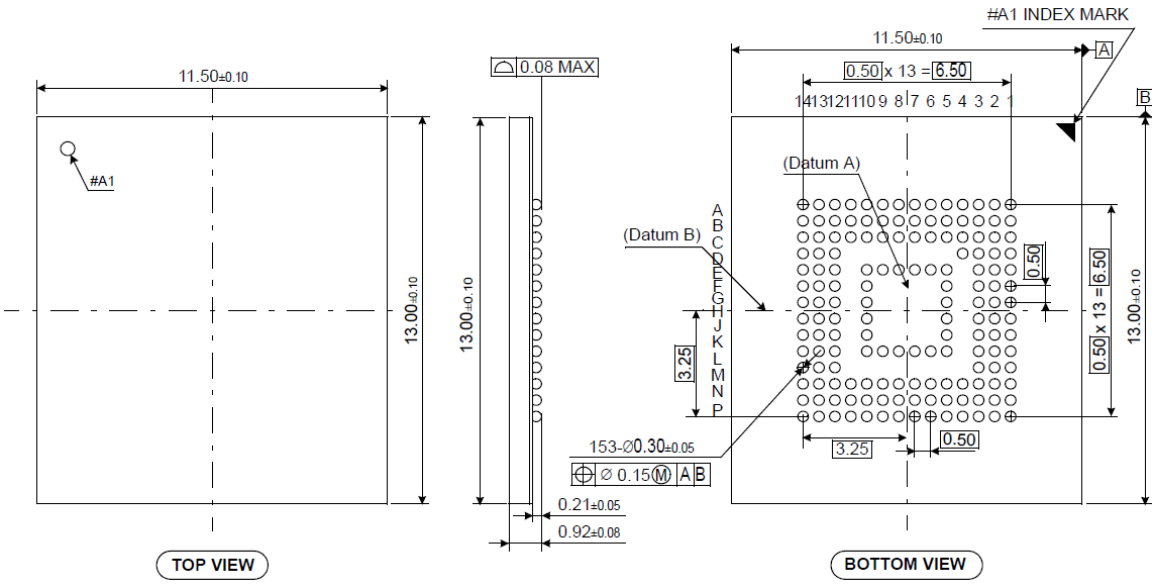
Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	V_{CCQ}
M4	V_{CCQ}
N4	V_{CCQ}
P3	V_{CCQ}
P5	V_{CCQ}
E6	V_{CC}
F5	V_{CC}
J10	V_{CC}
K9	V_{CC}
C2	VDDI
M5	CMD
H5	Data Strobe
M6	CLK
J5	V_{SS}
A6	V_{SS}
C4	V_{SS}
E7	V_{SS}
G5	V_{SS}
H10	V_{SS}
K8	V_{SS}
N2	V_{SS}
N5	V_{SS}
P4	V_{SS}
P6	V_{SS}

Ball-side down view ○ → NC



- CLK : Clock input
- Data Strobe : Data Strobe is generated from eMMC to host.
  In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD : A bidirectional signal used for device initialization and command transfers.
  Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7 : Bidirectional data channels. It operates in push-pull mode.
- RST_n : H/W reset signal pin
- VCC : Supply voltage for flash memory
- VCCQ : Supply voltage for memory controller
- VDDi : Internal power node to stabilize regulator output to controller core logics
- VSS : Ground connections
- RFU : Reserved for future use , do not use for any usage

Package Dimensions

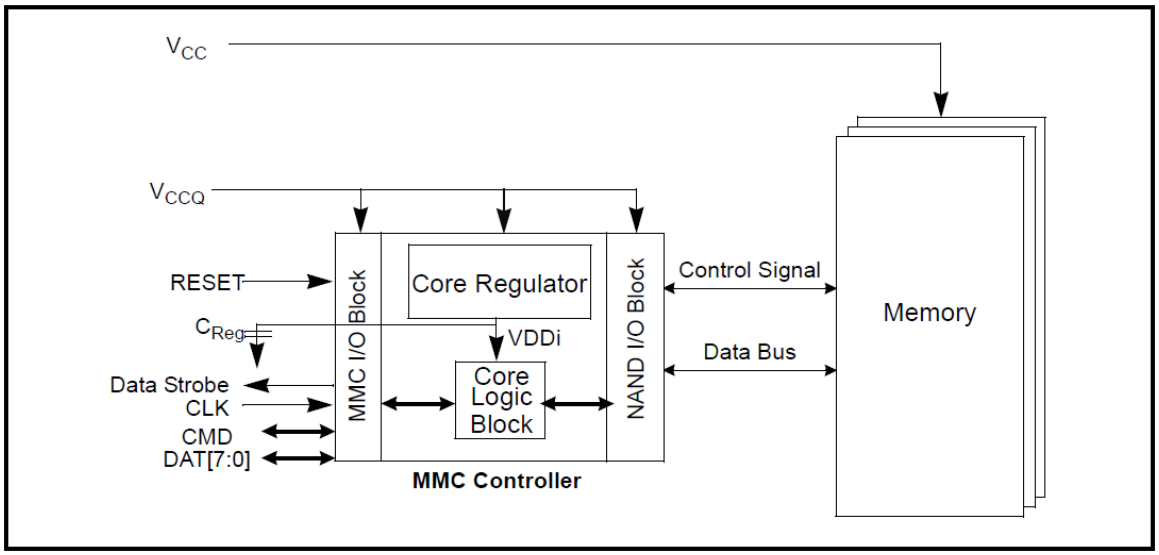


Unit: mm

11.5mm×13mm×1.0mm Package Dimensions

Product Architecture

e•MMC consists of NAND Flash and Controller. V_{CCQ} is for Controller power and V_{CC} is for flash power.



e•MMC Features

HS400 mode

eMMC5.0 product supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply. HS400 mode supports the following features :

- DDR Data sampling method
- CLK frequency up to 200 MHz DDR – up to 400 Mbps.
- Only 8-bits bus width supported
- Signaling levels of 1.8 V
- • Six selectable Drive Strength (refer to the table below)

I/O driver strength types

Driver Type Values	Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0x0	Mandatory	50 Ω	x1	Default Driver Type. Supports up to 200 MHz operation
0x1	Optional	33 Ω	x1.5	Supports up to 200 MHz operation.
0x2	Optional	66 Ω	x0.75	The weakest driver that supports up to 200 MHz operation.
0x3	Optional	100 Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design
0x4	Optional	40 Ω	x1.2	Supports up to 200MHz DDR operation

Note： Supporting Driver types 1~4 are optional for HS200 & HS400 Device.

Device type values (EXT_CSD Register: DEVICE_TYPE [196])

Bit	Device Type	Supportability
7	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate e•MMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate e•MMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed e•MMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed e•MMC @ 26MHz - at rated device voltage(s)	Support

Note： It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

Extended CSD revisions (EXT_CSD Register: EXT_CSD_REV [192])

Value	Timing Interface	EXT_CSD Register Value
255–9	Reserved	-
8	Revision 1.8 (for MMC v5.1)	0x08
7	Revision 1.7 (for MMC V5.0)	-
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-
3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

Note：Current e•MMC standard defined by JEDEC supports up to 0x08 for EXT_CSD_REV value.

High Speed timing values (EXT_CSD Register: HS_TIMING [185])

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

e•MMC 5.1 Features

Overview

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes
Secure Write Protection	Optional	Yes

Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.
Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for execution, its state changes to “ready for execution”.
The host tracks the state of all queued tasks and may order the execution of any task, marked as “ready for execution”, by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command (CMD46/CMD47).

CMD Set Description

■ CMD Set Description and Details

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming [23] Priority: “0” simple / “1” high [20:16] TASK ID [15:0] number of blocks	QUEUED_TASK _PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data blocks
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data blocks
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK _MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID. When TM op-code = 1h these bits are reserved."

New Response: QSR (Queue Status Register)

The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit[15]=”1”), R1’s argument will be the 32- bit Queue Status Register (QSR). Every bit in the QSR represents the task who’s ID corresponds to the bit index. If bit QSR[i] = “0”, then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR[i] = “1”, then the queued task with Task ID i is ready for execution.

Send Status: CMD13

CMD13 for reading the Queue Status Register (QSR) by the host. If bit[15] in CMD13’s argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response.

Mechanism of CMD Queue operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15]bits to 1 . After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at anytime when the CMD line is not in use

CMD Queue Register description

Configuration and capability structures shall be added to the EXT_CSD register, as described below

■ CMD Queuing Support (EXT_CSD register : CMDQ_SUPPORT [308])

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not

0x0: CMD Queue function is not supported
0x1: CMD Queue function is supported

■ Command Queue Mode Enable(EXT_CSD register : CMDQ_MODE_EN [15])

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							0x00

This field is used by the host enable command queuing

0x0: Queue function is not enabled
0x1: Queue function is enabled

■ CMD Queuing Depth(EXT_CSD register : CMDQ_DEPTH [307])

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			0x0F				

This field is used to calculate the depth of the queue supported by the device

Bit encoding:
[7:5]: Reserved
[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.
Queue Depth = N+1.

Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refer to the details as described in eMMC5.1 JEDEC standard.

RPMB Throughput improve

■ Related parameter register in EXT_CSD : WR_REL_PARAM [166]

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit[4]: EN_RPMB_REL_WR(R)
0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).
0x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame), or 8KB(Thirthy two 512B frames).

Secure Write Protection

Configuration and capability structures shall be added to the EXT_CSD register and Authenticated Device Configuration Area as described below.

■ Parameter register in EXT_CSD : SECURE_WP_INFO [211]

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						SECURE_WP_EN_STATUS	SECURE_WP_SUPPORT

Bit[7:2]: Reserved
Bit[1]: SECURE_WP_EN_STATUS(R)
0x0: Legacy Write Protection mode.
0x1: Secure Write Protection mode.
Bit[0]: SECURE_WP_SUPPORT(R)
0x0: Secure Write Protection is NOT supported by this device
0x1: Secure Write Protection is supported by this device

■ Authenticated Device Configuration Area[1] : SECURE_WP_MODE_ENABLE

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							0x00

Bit[7:1] : Reserved
Bit[0] : SECURE_WP_EN (R/W/E)
The default value of this field is 0x0.

- 0x0 : Legacy Write Protection mode, i.e., TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13] is updated by CMD27. USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are updated by CMD6.
- 0x1 : Secure Write Protection mode. The access to the write protection related EXT_CSD and CSD fields depends on the value of SECURE_WP_MASK bit in SECURE_WP_MODE_CONFIG field.

■ Authenticated Device Configuration Area[2] : SECURE_WP_MODE_CONFIG

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							0x00

Bit[7:1] : Reserved
Bit[0] : SECURE_WP_MASK (R/W/E_P)
The default value of this field is 0x0.

- 0x0: Disabling updating WP related EXT_CSD and CSD fields. CMD27 (Program CSD) will generate generic error for setting TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13]. CMD6 for updating USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] generates SWITCH_ERROR. If a force erase command is issued, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. If CMD28 or CMD29 is issued, then generic error will be occurred.Power-on Write Protected boot partitions will keep protected mode after power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.
- 0x1: Enabling updating WP related EXT_CSD and CSD fields. I.e TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13] , USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are accessed using CMD6, CMD8 and CMD27.If a force erase command is issued and accepted, then ALL THE DEVICE CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked Device will get unlocked. If a force erase command is issued and power-on protected or a permanently-write- protected write protect groups exist on the device, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. An attempt to force erase on an unlocked Device will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register. Write Protection is applied to the WPG indicated by CMD28 with the WP type indicated by the bit[2] and bit[0] of USER_WP[171]. All temporary WP Groups and power-on Write Protected boot partitions become writable/erasable temporarily which means write protect type is not changed. All power-on and permanent WP Groups in user area will not become writable/erasable temporarily. Those temporarily writable/erasable area will become write protected when this bit is cleared to 0x0 by the host or when there is power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

Technical Notes

Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

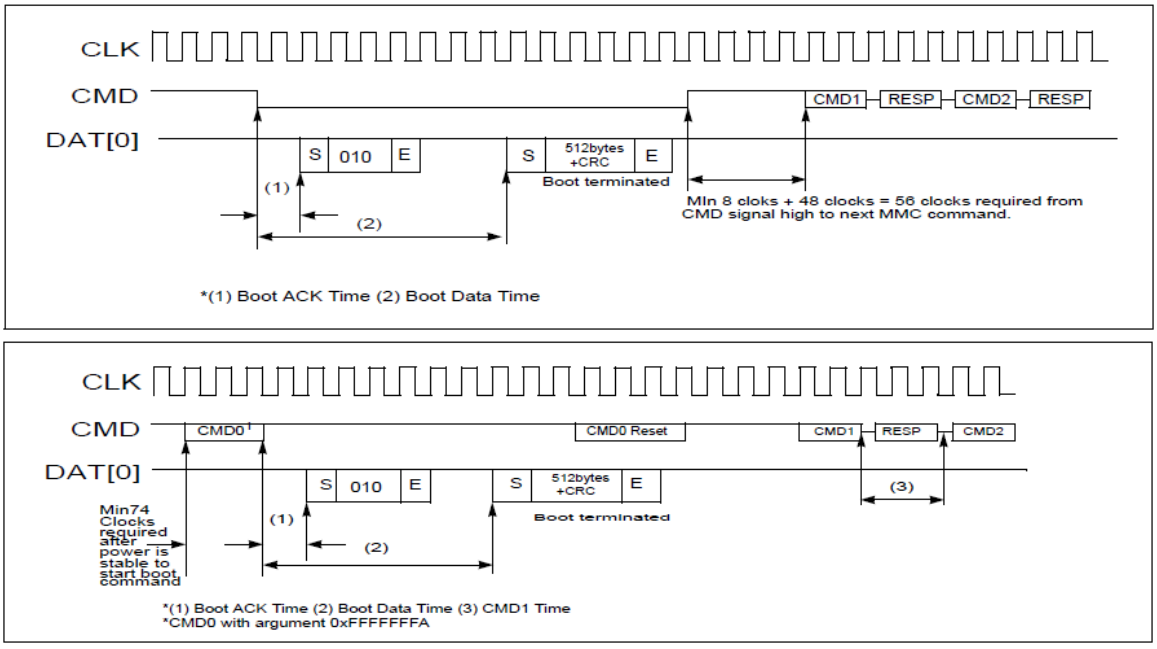
Enhanced Partition (Area)

This eMMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to gen- erate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.



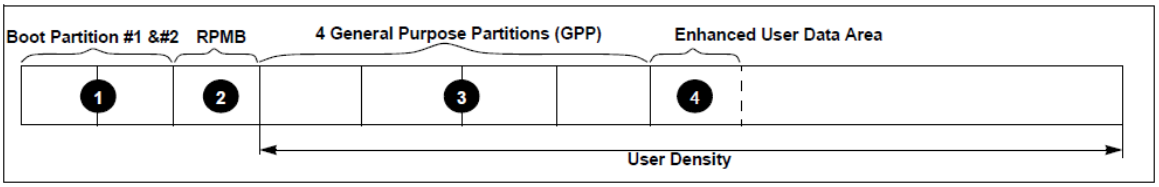
Boot ack, boot data and initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 100 ms
(3) Initialization Time1)	< 3 secs

NOTE: 1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 6.4 Extended CSD Register. Normal initialization time (without partition setting) is completed within 1sec

User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 64MB in MLC.
This results in decreasing of user density



Boot and RPMB Size

	Boot1 Size	Boot2 Size	RPMB Size
Default	4096 KB	4096 KB	4096 KB

User Density Size

Capacity	User Area Capacity
64 GB	62,537,072,640 Byte

Maximum Enhanced Partition Size

Capacity	Max. Enhanced Partition Size
32 GB	31,264,342,016 Byte

Performance

Capacity	Sequential Read (MB/s)	Sequential Write (MB/s)
64 GB	330	200

Test Condition: Bus width x8, HS400 , 512KB data transfer, w/o file system overhead, measured on internal board.

Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.
At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

Auto Power Saving Mode and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
Goto Sleep Time	< 1ms	< 1ms

Device Register

OCR Register

The 32-bit operation conditions register stores the VCCQ voltage profile of the eMMC. In addition, this register includes a status information bit. This status bit is set if the eMMC power up procedure has been finished. The OCR register shall be implemented by all eMMCs.

OCR bit	V_{CCQ} voltage window	e•MMC
[6:0]	Reserved	000 0000b
[7]	1.7–1.95	1b
[14:8]	2.0–2.6	000 0000b
[23:15]	2.7–3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	eMMC power up status bit (busy)*	

Note*： This bit is set to LOW if the e•MMC has not finished the power up routine.

The voltage for internal flash memory(VCC) should be 2.7-3.6v regardless of OCR Register value.

CID Register

The Device IDentification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (e•MMC protocol). Every individual flash or I/O Device shall have a unique identification number. Every type of e•MMC Device shall have a unique identification number. The structure of the CID register is defined in this section.

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved	-	6	[119:114]	--
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	--(1)
Product name	PNM	48	[103:56]	--
Product revision	PRV	8	[55:48]	--(2)
Product serial number	PSN	32	[47:16]	--(3)
Manufacturing date	MDT	8	[15:8]	--(4)
CRC7 checksum	CRC	7	[7:1]	--(5(
Not used, always ‘1’	-	1	[0:0]	--

NOTE :

1) ,4),5) description are same as eMMC JEDEC standard

2) PRV is composed of the revision count of controller and the revision count of F/W patch

3) A 32 bits unsigned binary integer. (Random Number)

CSD Register

The Card-Specific Data register provides information on how to access the eMMC contents. The programmable part of the register can be changed by CMD27. The type of the entries in the table below is coded as follows:
R: Read only
W: One time programmable and not readable. R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x3
System specification version	SPEC_VERS	4	R	[125:122]	0x4
Reserved	-	2	R	[121:120]	--
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x1
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Card command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x9
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x0
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x0
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x0
DSR implemented	DSR_IMP	1	R	[76:76]	0x0
Reserved	-	2	R	[75:74]	--
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x6
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x6
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x6
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x6
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x7
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0xF
Write protect group enable	WP_GRP_MULT	1	R	[31:31]	0x1
Manufacturer default	ECC DEFAULT_ECC	2	R	[30:29]	0x0
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x3
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x9
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x0
Reserved	-	4	R	[20:17]	--
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x0
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x0
Copy flag(OTP)	COPY	1	R/W	[14:14]	0x1
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x0
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x0
File format	FILE_FORMAT	2	R/W	[11:10]	0x0
ECC code	ECC	2	R/W/E	[9:8]	0x0
CRC	CRC	7	R/W/E	[7:1]	--
Not used, always ‘1’	-	1	-	[0:0]	--

Extended CSD Register

The Extended CSD register defines the eMMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the eMMC is working in. These modes can be changed by the host by means of the SWITCH command.

R: Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Properties Segment					
Reserved	-	6	TBD	[511:506]	All ”0”
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x02
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported modes	SUPPORTED_MODES	1	R	[493]	0x03
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0xC7810000
Barrier support	BARRIER_SUPPORT	1	R	[486]	0x00
Reserved	-	177	-	[485:309]	--
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x01
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x0F
Reserved	-	1	--	[306]	--
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x01
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x01
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x00

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x20
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x01
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x00
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01
Device version	DEVICE_VERSION	1	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	3	R	[261:254]	0x01
Power class for 200MHz, DDR at V_{CC}= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x10000
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	--
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200MHz at V_{CCQ} =1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0x00
Power class for 200MHz, at V_{CCQ}=1.3V, V_{CC} = 3.6V	PWR_CL_200_130	1	R	[236]	0x00
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved		1	--	[233]	--
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved		1	--	[227]	--
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	0x07
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current [V_{CC}]	S_C_VCC	1	R	[220]	0x07
Sleep current [V_{CCQ}]	S_C_VCCQ	1	R	[219]	0x07
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x00
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Sleep Notification Timout1	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x07
Sector Count	SEC_COUNT	4	R	[215:212]	0x747C000

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved		1	--	[204]	--
Power class for 26MHz at 3.6 V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52MHz at 3.6 V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26MHz at 1.95 V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52MHz at 1.95 V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x02
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x0A
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved		1	--	[195]	--
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved		1	--	[193]	--
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x08
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved		1	--	[190]	--
Command set revision	CMD_SET_REV		R	[189]	0x00
Reserved		1	--	[188]	--
Power class	POWER_CLASS		R/W/E_P	[187]	0x00
Reserved		1	--	[186]	--
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x01
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved		1	--	[182]	--
Erased memory range	ERASE_MEM_CONT	1	R	[181]	0x00
Reserved		1	--	[180]	--
Partition Configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00
Boot Config protection	BOOT_CONFIG_PROT	1	R/W &R/W/C_P	[178]	0x00

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x0
Reserved		1	--	[176]	--
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protect register	BOOT_WP	1	R/W &R/W/C_P	[173]	0x00
Reserved		1	--	[172]	--
User area write protect register	USER_WP	1	R/W,R/W/C_P &R/W/E_P	[171]	0x00
Reserved		1	--	[170]	--
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x07
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0xE8F
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved		1	--	[135]	--
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01
Reserved		2	--	[129:128]	--
Vendor Specific Fields	NATIVE_SECTOR_SIZE	64	<vendor specific>	[127:64]	--
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved		2	--	[28:27]	--
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	0x00
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x00
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x39
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00
Reserved		15	--	[14:0]	--

Note： Reserved bits should be read as “0”.

AC Parameter

Timing Parameter

Timing Parameter：

Timing Parameter		Max. Value	Unit
Initialization Time (t_{INIT})	Normal	1	s
	After partition setting	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		20	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout		600	ms
Partition Switching Timeout (after Init)		1	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

Note：

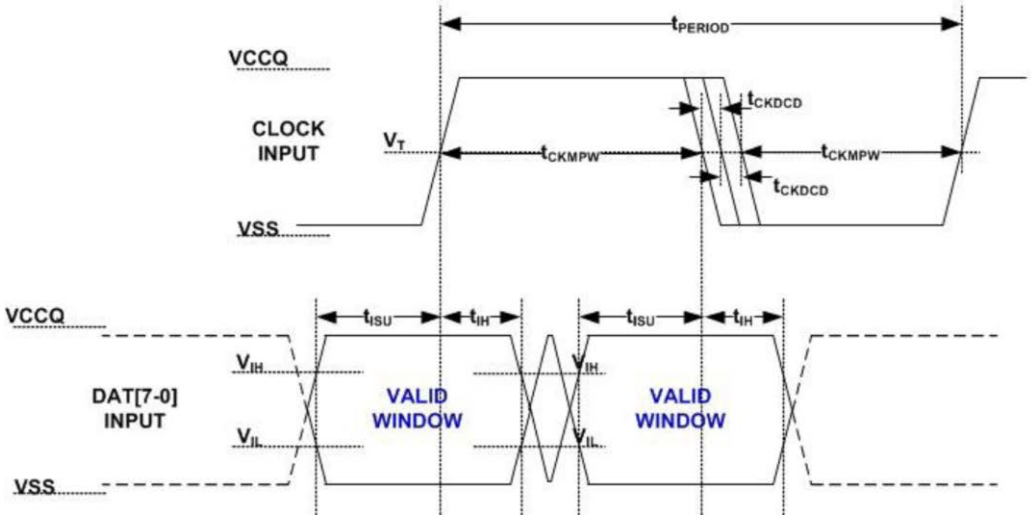
- Normal Initialization Time without partition setting
- Initialization Time after partition setting, refer to INI_TIMEOUT_AP in EXT_CSD register
- Be advised Timeout Values specified in Table above are for testing purposes under internal test pattern only and actual timeout situations may vary
- EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment

Bus Timing Parameters for DDR52 and HS200 are defined by JEDEC standard

Bus Timing Specification in HS400 mode

HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.



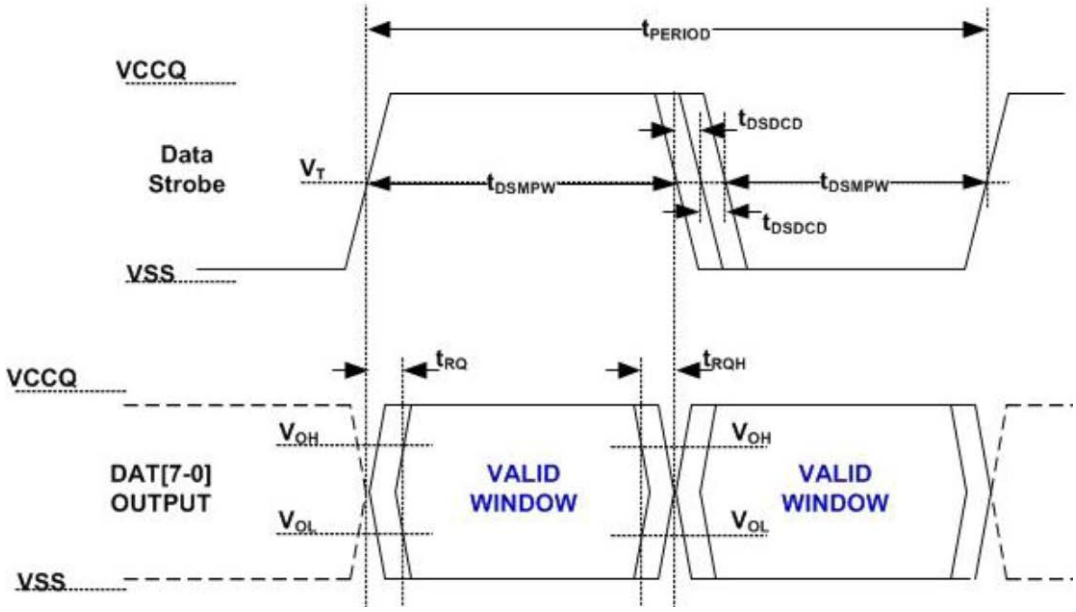
NOTE V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5			200 MHz(max), between rising edges With respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4		ns	C_{Device} ≤ 6 pF With respect to V_{IH}/V_{IL}.
Input hold time	t_{IHddr}	0.4		ns	C_{Device} ≤ 6 pF With respect to V_{IH}/V_{IL}.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.

HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



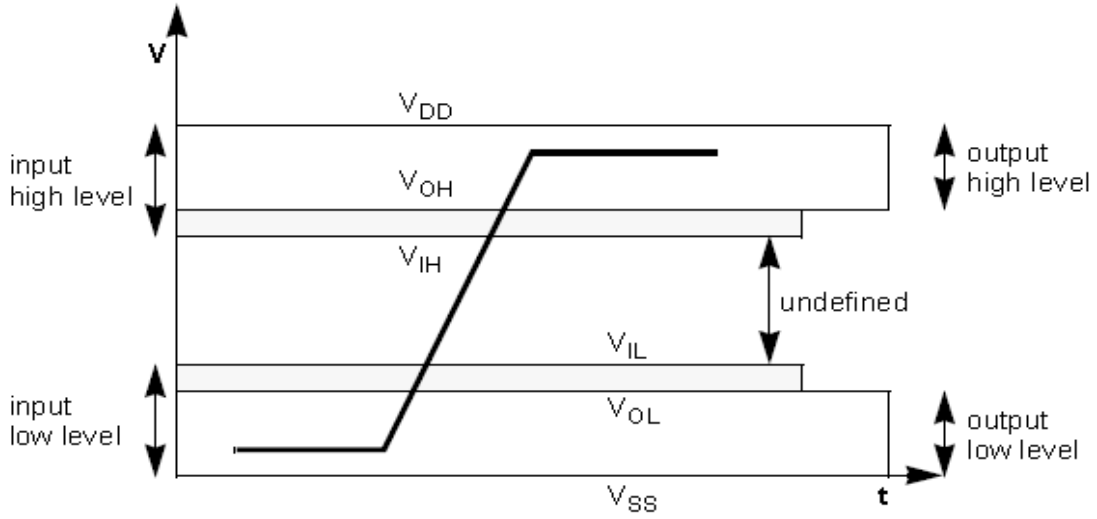
NOTE V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200 MHz(max), between rising edges With respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	T_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



Open-Drain Mode Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2		V	Note
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2mA

Note:

Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

Bus Signal Level (High-Voltage)

The device input and output voltages shall be within the following specified ranges for any V_{CCQ} of the allowed voltage range.

Push-pull signal level—high-voltage e•MMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}	--	V	I_{OH} = -100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	--	0.125 * V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625* V_{CCQ}	V_{CCQ} + 0.3	V	--
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 * V_{CCQ}	V	--

Push-pull signal level—1.70 V -1.95 V V_{CCQ} voltage Range

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	--	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	--	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	--
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{CCQ} (2)	V	--

Note:

- 0.7 * V_{DD} for MMC4.3 and older revisions.
- 0.3 * V_{DD} for MMC4.3 and older revisions.

DC Parameter

Active Power Consumption during operation

Density	NAND TYPE	VCCQ	VCC	Unit
64GB	128Gb x 4	180	200	mA

* Power Measurement conditions: Bus configuration =x8 @HS400
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms

Power Supply Voltage

Symbol	Test Conditions	Min	Max	Unit
VSS	--	-0.5	0.5	V
V_{CC}	--	2.7	3.6	V
V_{CCQ}	--	1.7	1.95	V

Standby Power Consumption

Standby Power Consumption in auto power saving mode and standby state

Capacity	NAND Type	State	VCCQ		VCC		Unit
			25℃	85℃	25℃	85℃	
64 GB	128Gbx 4	Standby	120	400	70	235	uA

Note:

- Power measurement conditions: Bus configuration =x8, No CLK
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

Sleep Power Consumption

Sleep Power Consumption in Sleep State

Capacity	NAND Type	State	VCCQ		VCC	Unit
			25℃	85℃		
64 GB	128Gbx 4	Sleep	120	400	0*	uA

Note:

Power Measurement conditions: Bus configuration =x8, No CLK

* In auto power saving mode, VCC power can not be turned off. However in sleep mode VCC power can be turned off.

Bus Signal Line Load

The total capacitance C_L of each line of the e•MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e•MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Bus Signal Line Load

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	--	100	kΩ	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	--	100	kΩ	to prevent bus floating
Internal pull up resistance DAT1–DAT7	R_{int}	10	--	150	kΩ	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}	--	--	12	pF	Single Device capacitance
Maximum signal line inductance	--	--	--	16	nH	$f_{PP} \leq 52$ MHz

HS400 Capacitance and Resistors

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-down resistance for Data Strobe	R_{DS}	10	--	100	kΩ	
Single Device capacitance	C_{DEVICE}			6	pF	Single Device
Bus signal line capacitance	C_L			13	pF	Single Device

Note: Recommended maximum value is 50 kΩ for 1.8V interface supply voltages.