4Gb (32Mx8Banksx16) DDR3 SDRAM

Descriptions

The H2A404G1666A is a high speed Double Date Rate 3 (DDR3) Synchronous DRAM fabricated with ultra high performance CMOS process containing 4G bits which organized as 32Mbits x 8 banks by 16 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin (DDR3-1866) for general applications. The chip is designed to comply with the following key DDR3 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) On Die Termination (4) programmable driver strength data,(5) seamless BL4 access. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional differential data strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style.

Features

- VDD = VDDQ = 1.5V ± 0.075V (JEDEC Standard Power Supply).
- 8 Internal memory banks (BA0-BA2).
- Differential clock input (CK,/CK).
- Programmable /CAS Latency: 6,7,8,9,10,11,12,13
- /CAS WRITE Latency (CWL): 5,6,7,8,9
- POSTED CAS ADDITIVE Programmable Additive Latency (AL): 0, CL-1, CL-2 clock
- Programmable Sequential / Interleave Burst Type.
- Programmable Burst Length: 4, 8.

  Through ZQ pin (RZQ:240 ohm±1%)
- 8n-bit prefetch architecture.
- Output Driver Impedance Control.
- Differential bidirectional data strobe.
- Internal(self) calibration: Internal self calibration.
- OCD Calibration.
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS compliance and Halogen free
- Packages: 96-Ball BGA for x16 components

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A404G1666ADFC	256M X 16	DDR3-1333MHz 9-9-9	96Ball BGA, 8x13mm	Commercial
H2A404G1666AFFC	256M X 16	DDR3-1600MHz 11-11-11	96Ball BGA, 8x13mm	Commercial
H2A404G1666AGFC	256M X 16	DDR3-1866MHz 13-13-13	96Ball BGA, 8x13mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDDQ	DQ13	DQ15	A	DQ12	VDDQ	VSS
VSSQ	VDD	VSS	B	/UDQS	DQ14	VSSQ
VDDQ	DQ11	DQ9	C	UDQS	DQ10	VDDQ
VSSQ	VDDQ	UDM	D	DQ8	VSSQ	VDD
VSS	VSSQ	DQ0	E	LDM	VSSQ	VDDQ
VDDQ	DQ2	LDQS	F	DQ1	DQ3	VSSQ
VSSQ	DQ6	/LDQS	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	H	DQ7	DQ5	VDDQ
NC	VSS	/RAS	J	CK	VSS	NC
ODT	VDD	/CAS	K	/CK	VDD	CKE
NC	/CS	/WE	L	A10/AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12 , /BC	BA1	VDD
VSS	A5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	/RESET	A13	T	A14	A8	VSS

96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
J7,K7	CK,/CK	**(System Clock)** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK . Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
L2	/CS	**(Chip Select)** All commands are masked when CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
K9	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self- refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including self-refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self -refresh.
N3,P7,P3,N2, P8,P2,R8,R2, T8,R3,L7,R7, N7	A0~A9,A10(AP), A11,A12(/BC),	**(Address)** Provided the row address (RA0 – RA12) for active commands and the column address (CA0-CA9) and auto precharge bit for read/write commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). The address inputs also provide the op-code during Mode Register Set commands. A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
M2,N8,M3	BA0,BA1,BA2	**(Bank Address)** BA0 – BA2 define to which bank an active, read, write or precharge command is being applied. Bank address also determines if the mode register is to be accessed during a MRS cycle.
K1	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ,DQS, DQS DMU and DML signal. The ODT pin will be ignored if the Mode Register MR1 is programmed to disable ODT.

C7,B7,F3,G3	DQSU, /DQSU, DQSL, /DQSL	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQSL, and DQSU are paired with differential signals /DQSU and /DQSL respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
J3,K3,L3	/RAS, /CAS,/WE	**(Command Inputs)** /RAS , /CAS & /WE (along with /CS) define the command being entered.
D3,E7	DMU,DML	**(Input Data Mask)** DMU & DML are input mask signal for write data. Input data is masked when DMU or DML are sampled HIGH coincident with that input data during a write access. DMU & DML is sampled on both edges of DQSU & DQML respectively.
D7,C3,C8,C2, A7,A2,B8,A3	DQU0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
E3,F7,F2,F8, H3,H8,G2,H7	DQL0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
B2,D9,G7,K2,K9,N1, N9,R1,R9/A9,B3,E1, G8,J2,J8,M1,M9,P1, P9,T1,T9	VDD,VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
A1,A8,C1,C9,D2, E9,F1,H2,H9 /B1, B9,D1,D8,E2,E8, F9,G1,G9	VDDQ, VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
L8	ZQ	**(ZQ Calibration)** Reference pin for ZQ calibration
T2	/RESET	**(Active Low Asynchronous Reset)** Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
H1	VREFDQ	**(Reference Voltage)** Reference voltage for DQ
M8	VREFCA	**(Reference Voltage)** Reference voltage for CA
J1,J9,L1,L9, M7,T3,T7	NC	**(No Connection)** No internal electrical connection is present.

Note: Input pins only BA0-BA2, A0-A12, /RAS , /CAS , /WE , /CS , CKE, ODT and /RESET do not supply termination.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.4 ~ +1.80		V
VDD	Power Supply Voltage	-0.4 ~ +1.80		V
VDDQ	Power Supply Voltage	-0.4 ~ +1.80		V
TOP	Operating Temperature Range	Commercial	0 ~ +85	℃
TSTG	Storage Temperature Range	-55 ~ +100		℃
VREFCA	Reference Voltage for Control	-0.4 ~ 0.6*VDD		V
VREFDQ	Reference Voltage for DQ	-0.4 ~ 0.6*VDDQ		V

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Power Supply for I/O Voltage	1.425	1.5	1.575	V

Input/ Output Capacitance

Symbol	Parameters	Pins	Min.	Max.	Unit	Notes
CCK	Input pin capacitance, CK, /CK	CK, /CK	0.8	1.4	pF	1,3
CDCK	Delta input pin capacitance, CK, /CK		0	0.15	pF	1,2
CIN_CTRL	Input pin capacitance, control pins	/CS,CKE,ODT	0.75	1.3	pF	1
CDIN_CTRL	Delta input pin capacitance, control pins		-0.4	0.2	pF	1,4
CIN_ADD_CMD	Input pin capacitance, address and command pins	/RAS,/CAS,/WE, Address	0.75	1.3	pF	1
CDIN_ADD_CMD	Delta input pin capacitance,		-0.4	0.4	pF	1,5
CIO	Input/output pins capacitance	DQ,DQS,/DQS TDQS,/TDQS, DM	1.5	2.5	pF	1,6
CDIO	Delta input/output pins capacitance		-0.5	0.3	pF	1,7,8
CDDQS	Delta input/output pins capacitance	DQS, /DQS	0	0.15	pF	1,10
CZQ	Input/output pin capacitance, ZQ	ZQ	-	3	pF	1,9

Notes1: VDD, VDDQ, VSS, VSSQ applied and all other pins (except the pin under test) floating.

Notes2: Absolute value of CCK(CK-pin) - CCK(/CK-pin).

Notes3: CCK (min.) will be equal to CIN (min.)

Notes4: CDIN_CTRL = CIN_CTRL - 0.5*(CCK(CK-pin) + CCK(/CK-pin))

Notes5: CDIN_ADD_CMD = CIN_ADD_CMD - 0.5*(CCK(CK-pin) + CCK(/CK-pin))

Notes6: Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.

Notes7: DQ should be in high impedance state.

Notes8: CDIO = CIO (DQ, DM) - 0.5*(CIO(DQS-pin) + CIO(/DQS-pin)).

Notes9: Absolute value of CIO(DQS) - CIO(/DQS).

Recommended DC Operating Conditions

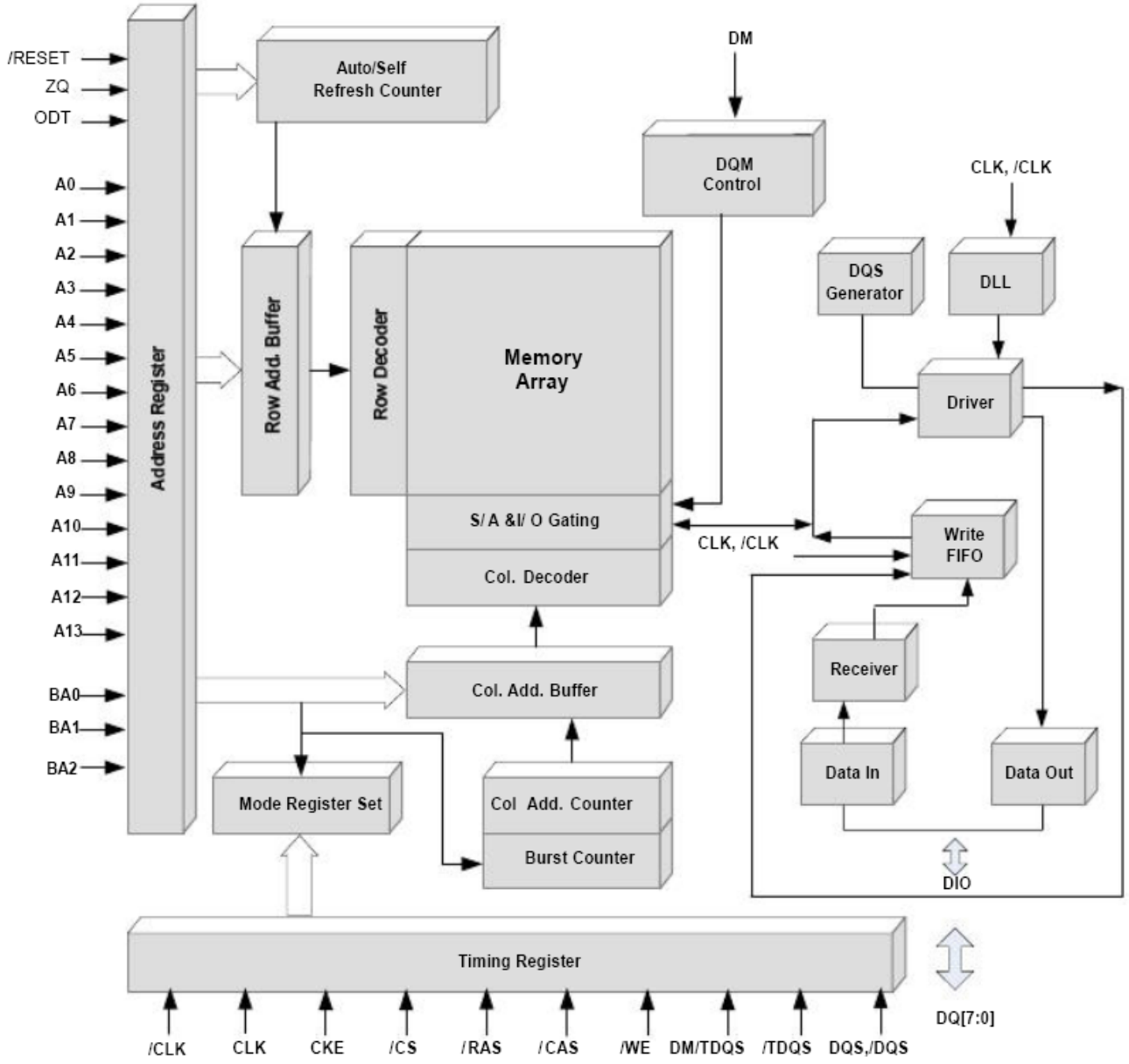
VDD/VDDQ = 1.5V±0.075V

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I_{DD0}	**Operating One Bank Active-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, CL, BL: 8a);AL: 0; CS: High between ACTand PRE ; Command, Address,Bank Address Inputs: partially toggling according to Table ; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0	95	90	85	mA
I_{DD1}	**Operating One Bank Active-Read-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	120	115	110	mA
I_{DD2P1}	**Precharge Power-Down Current Fast Exit:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	43	40	35	mA
I_{DD2N}	**Precharge Standby Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	55	50	45	mA
I_{DD3P}	**Active Power-Down Current:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	60	60	60	mA
I_{DD4W}	**Operating Burst Write Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	240	225	200	mA
I_{DD4R}	**Operating Burst Read Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between RD; Command, Address: par-tially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	240	225	200	mA

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I_{DD5B}	**Burst Refresh Current:** CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; /CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	215	210	195	mA
I_{DD6}	**Self Refresh Current:** Normal Temperature Range; TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL:8 ; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	25	25	25	mA
I_{DD7}	**Operating Bank Interleave Read Current; CKE:** High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0,1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	245	260	285	mA

Note1: SWITCHING for Address and Command Input Signals as described in Definition of SWITCHING for Address and Command Input Signals Table.
Note2: Output Buffer off: set MR1 A[12] = 1
Note3: ODT disable: set MR1 A[9,6,2]=000 and MR2 A[10,9]=00
Note4: Definition of D and D: described in Definition of SWITCHING for Address and Command Input Signals Table; Ax/Rx/Wx: Activate/Read/Write to Bank x.
Note5: BL8 fixed by MRS: set MR0 A[1,0]=00
Note6: Precharge Power Down Mode: set MR0 A12=0/1 for Slow/Fast Exit
Note7: Because it is an exit after precharge power down, the valid commands are: ACT, REF, MRS, Enter Self-Refresh.
Note8: Auto Self-Refresh(ASR): set MR2 A6 = 0/1 to disable/enable feature
Note9: Self-Refresh Temperature Range (SRT): set MR2 A7 = 0/1 for normal/extended temperature range
Note10: Cycle banks as follows: 0,1,2,3,...,7,0,1,...

Block Diagram



AC Operating Test Characteristics

DDR3-1333/ DDR3-1600/ DDR3-1866 Speed Bins

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Paramet	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AA}	Internal read command to first data	13.91	20	13.75	20	13.5	20	ns	8
t_{RCD}	Active to read or write delay	13.91	-	13.75	-	13.5	-	ns	8
t_{RP}	Precharge command period	13.91	-	13.75	-	13.5	-	ns	8
t_{RC}	Active to active/auto refresh	47.91	-	48.75	-	49.5	-	ns	8
t_{RAS}	Active to precharge command period	34	9*tREFI	35	9*tREFI	36	9*tREFI	ns	7
t_{CK} (AVG)	Average Clock Cycle, CL=6, CWL=5	2.5	3.3	2.5	3.3	3.0	3.3	ns	1,2,3,4,5,6
t_{CK} (AVG)	Average Clock Cycle, CL=7, CWL=6	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,4,5,6
t_{CK} (AVG)	Average Clock Cycle, CL=8, CWL=6	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,5,6
t_{CK} (AVG)	Average Clock Cycle, CL=9, CWL=7	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,4,6
t_{CK} (AVG)	Average Clock Cycle, CL=10, CWL=7	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,6
t_{CK} (AVG)	Average Clock Cycle, CL=11, CWL=8	1.25	< 1.5	1.25	< 1.5	-	-	ns	1,2,3
t_{CK} (AVG)	Average Clock Cycle, CL=12, CWL=9	1.07	< 1.25	-	-	-	-	ns	1,2,3,6
t_{CK} (AVG)	Average Clock Cycle, CL=13, CWL=9	1.07	< 1.25	-	-	-	-	ns	1,2,3
-	Support CL Settings	6,7,8,9,10,11,12,13				6,7,8,9,10		nCK	
-	Support CWL Settings	5,6,7,8,9				5,6,7		nCK	

Notes1: The CL setting and CWL setting result in tCK (avg) (min.) and tCK (avg) (max.) requirements. When making a selection of tCK (avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

Notes2: tCK (avg) (min.) limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (avg) value (2.5, 1.875, 1.5, or 1.25ns) when calculating CL (nCK) = tAA (ns) / tCK (avg)(ns), rounding up to the next 'Supported CL'.

Notes3: tCK (avg) (max.) limits: Calculate tCK (avg) + tAA (max.)/CL selected and round the resulting tCK (avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is tCK (avg) (max.) corresponding to CL selected.

Notes4: 'Reserved' settings are not allowed. User must program a different value.

Notes5: Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.

Notes6: Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.

Notes7: tREFI depends on operating case temperature (TC).

Notes8: For devices supporting optional down binning to CL = 7 and CL = 9, tAA/tRCD/tRP(min.) must be 13.125 ns or lower. SPD settings must be programmed to match.

Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0~BA2	A10	A12, A10~A0
		n-1	N							
Device Deselect	DES	H	H	H	X	X	X	X	X	X,X
No Operation	NOP	H	H	L	H	H	H	V	V	V,V
Read (fixed BL8/BC4)	RD	H	H	L	H	L	H	BA	L	V,CA
Read (BC4, OTF)	RDS4	H	H	L	H	L	H	BA	L	L,CA
Read (BL8, OTF)	RDS8	H	H	L	H	L	H	BA	L	H,CA
Read with Auto Pre-charge (fixed BL8/BC4)	RDA	H	H	L	H	L	H	BA	H	V,CA
Read with Auto Pre-charge (BC4, OTF)	RDAS4	H	H	L	H	L	H	BA	H	L,CA
Read with Auto Pre-charge (BL8, OTF)	RDAS8	H	H	L	H	L	H	BA	H	H,CA
Write (fixed BL8/BC4)	WR	H	H	L	H	L	L	BA	L	V,CA
Write (BC4, OTF)	WRS4	H	H	L	H	L	L	BA	L	L,CA
Write (BL8,OTF)	WRS8	H	H	L	H	L	L	BA	L	H,CA
Write with Auto Pre-charge (fixed BL8/BC4)	WRA	H	H	L	H	L	L	BA	H	V,CA
Write with Auto Pre-charge (BC4, OTF)	WRAS4	H	H	L	H	L	L	BA	H	L,CA
Write with Auto Pre-charge (BL8, OTF)	WRAS8	H	H	L	H	L	L	BA	H	H,CA
Bank Activate	ACT	H	H	L	L	H	H	BA	RA	
Pre-charge Single Bank	PRE	H	H	L	L	H	L	BA	L	V,V
Pre-charge All Banks	PREA	H	H	L	L	H	L	V	H	V,V
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code	
Refresh	REF	H	H	L	L	L	H	V	V	V,V
Self Refresh entry	SRE	H	L	L	L	L	H	V	V	V,V
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X,X
				L	H	H	H	V	V	V,V
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X,X
		H	L	L	H	H	H	V	V	V,V
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X,X
		L	H	L	H	H	H	V	V	V,V
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	H	X,X
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	L	X,X

H = High level, L = Low level, X = Don't care, V = Valid, BA=Bank Address, CA=Column Address, RA=Row Address

Note1: All DDR3 SDRAM commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

Note2: /RESET is low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

Note3: Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Note4: "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

Note5: Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly (OTF) BL will be defined by MRS.

Note6: The Power Down Mode does not perform any refresh operation.

Note7: The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note8: Self Refresh Exit is asynchronous.

Note9: VREF(Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note10: The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registerng any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

Note11: The Deselect command performs the same function as No Operation command.

Note12: Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18
For more details with all signals, see “Command Truth Table”					10

Note1: CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

Note2: Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.

Note3: Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.

Note4: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note5: The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

Note6: During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

Note7: DESELECT and NOP are defined in the “Command Truth Table”.

Note8: On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

Note9: Self-Refresh mode can only be entered from the All Banks Idle state.

Note10: Must be a legal command as defined in the “Command Truth Table”.

Note11: Valid commands for power-down entry and exit are NOP and DESELECT only.

Note12: Valid commands for self-refresh exit are NOP and DESELECT only.

Note13: Self-Refresh can not be entered during Read or Write operations.

Note14: The Power-Down does not perform any refresh operations.

Note15: “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

Note16: VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self refresh.operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operationor first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note17: If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

Note18: ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). /RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled “Low” anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
    - VDD and VDDQ are driven from a single power converter output, AND
    - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
    - Vref tracks VDDQ/2. OR
    - Apply VDD without any slope reversal before or at the same time as VDDQ.
    - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
    - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. *(tXPR=max (tXS ; 5 x tCK)*

6. Issue MRS Command to load ***MR2*** with all application settings. (To issue MRS command for ***MR2***, provide “Low” to BA0 and BA2, “High” to BA1.)

7. Issue MRS Command to load ***MR3*** with all application settings. (To issue MRS command for ***MR3***, provide “Low” to BA2, “High” to BA0 and BA1.)

8. Issue MRS Command to load ***MR1*** with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).

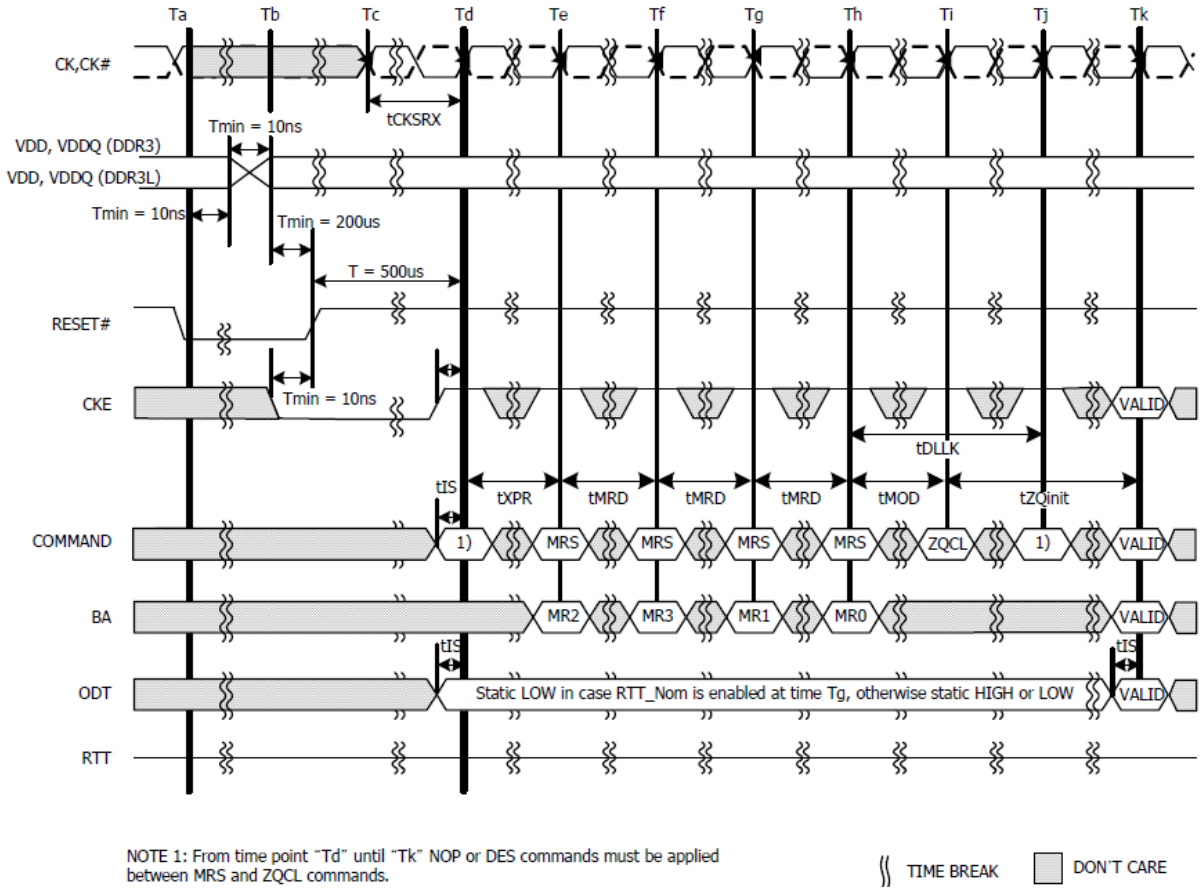
9. Issue MRS Command to load ***MR0*** with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.

12. The DDR3 SDRAM is now ready for normal operation.

Reset and Power up initialization sequence



NOTE 1: From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Mode Register Definition

Mode Register MR0

The Mode Register ***MR0*** stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	OO		0	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL	

DLL Control (for precharge PD)	A12
Slow exit (DLL off)	0
Fast exit (DLL on)	1

DLL Reset	A8
No	0
Yes	1

Mode	A7
Normal	0
Test	1

Read Burst Type	A3
Nibble sequential	0
Interleave	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

BL	A1	A0
8	0	0
4 or 8 (OTF)	0	1
4	1	0
Reserved	1	1

WR for autoprecharge	A11	A10	A9
Reserved	0	0	0
5	0	0	1
6	0	1	0
7	0	1	1
8	1	0	0
10	1	0	1
12	1	1	0
Reserved	1	1	1

CAS Latency	A6	A5	A4	A2
Reserved	0	0	0	0
Reserved	0	0	1	0
6	0	1	0	0
7	0	1	1	0
8	1	0	0	0
9	1	0	1	0
10	1	1	0	0
11	1	1	1	0

Note1: BA2,A13 and A14 are reserved for future use and must be programmed to 0 during MRS.

Note2: WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Burst Type (A3)

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
8 (chop)	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

Note1: In case of burst length being fixed to 4 by ***MR0*** setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12 (/BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Note2: 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

Note3: T: Output driver for data and strobes are in high impedance.

Note4: V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

Note5: X: Don't Care.

CAS Latency

The CAS Latency is defined by ***MR0*** (bits A9-A11). CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by ***MR0*** (bit A7 = 0) and rest bits set to the desired values. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM factory and should NOT be used. No operations or functionality is specified if A7 = 1.

DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

Write Recovery

The programmed WR value ***MR0*** (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/ tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When ***MR0*** (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When ***MR0*** (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register ***MR1*** stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	Qoff	TDQS	0	Rtt	0	Level	Rtt	D.I.C	AL		Rtt	D.I.C	DLL

TDQS enable	A11
Disabled	0
Enabled	1

Qoff	A12
Output buffer enabled	0
Output buffer disabled	1

Write leveling enable	A8
Disabled	0
Enabled	1

Output Driver Impedance Control	A5	A1
RZQ/6	0	0
RZQ/7	0	1
Reserved	1	0
Reserved	1	1

DLL Enable	A0
Enable	0
Disable	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

Rtt_Nom	A9	A6	A2
ODT disabled	0	0	0
RZQ/4	0	0	1
RZQ/2	0	1	0
RZQ/6	0	1	1
RZQ/12	1	0	0
RZQ/8	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Additive Latency	A4	A3
0	0	0
CL - 1	0	1
CL - 2	1	0
Reserved	1	1

Note1: BA2, A8, A10 and A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Note2: Qoff: Outputs disabled - DQs, DQSs, /DQSs.

Note3: In Write leveling Mode (***MR1***[bit7] = 1) with ***MR1***[bit12] = 1, all RTT_Nom settings are allowed; in Write Leveling Mode (***MR1***[bit7] = 1) with ***MR1***[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

DLL Enable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with ***MR1*** (A0 = 0), the DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refers to “DLL-off Mode”.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits ***MR1***{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode. The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, ***MR2*** {A10, A9} = {0,0}, to disable Dynamic ODT externally.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, It allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings.

Write Leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

Output Disable

The outputs may be enabled/disabled by MR1 (bit A12). When this feature is enabled (A12 = 1), all output pins (DQs, DQS, /DQS, etc.) are disconnected from the device, thus removing any loading of the output drivers. For normal operation, A12 should be set to '0'.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, including RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	Rtt_WR		0	SRT	0	CWL			0		

Self refresh temp. range	A7
Normal operating temp. range	0
Extended temp. self refresh	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

Rtt_WR	A10	A9
Dynamic ODT off	0	0
RZQ/4	0	1
RZQ/2	1	0
Reserved	1	1

CAS write latency (CWL)	A6	A4	A3
5(t_{CK} ≧ 2.5ns)	0	0	0
6 (2.5ns > t_{CK} ≧ 1.875ns)	0	0	1
7 (1.875ns > t_{CK} ≧ 1.5ns)	0	1	0
8 (1.5ns > t_{CK} ≧ 1.25ns)	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Note1: BA2, A8, A11 ~ A13 are RFU and must be programmed to 0 during MRS.

Note2: The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

CAS Write Latency (CWL)

The CAS Write Latency is defined by ***MR2*** (bits A3-A5). CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. ***MR2*** Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available.

Mode Register MR3

The Mode Register ***MR3*** controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	MPR	MPR Location	

MPR Operation	A2
Normal operation	0
Dataflow from MPR	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

MPR Location	A1	A0
Predefined pattern	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

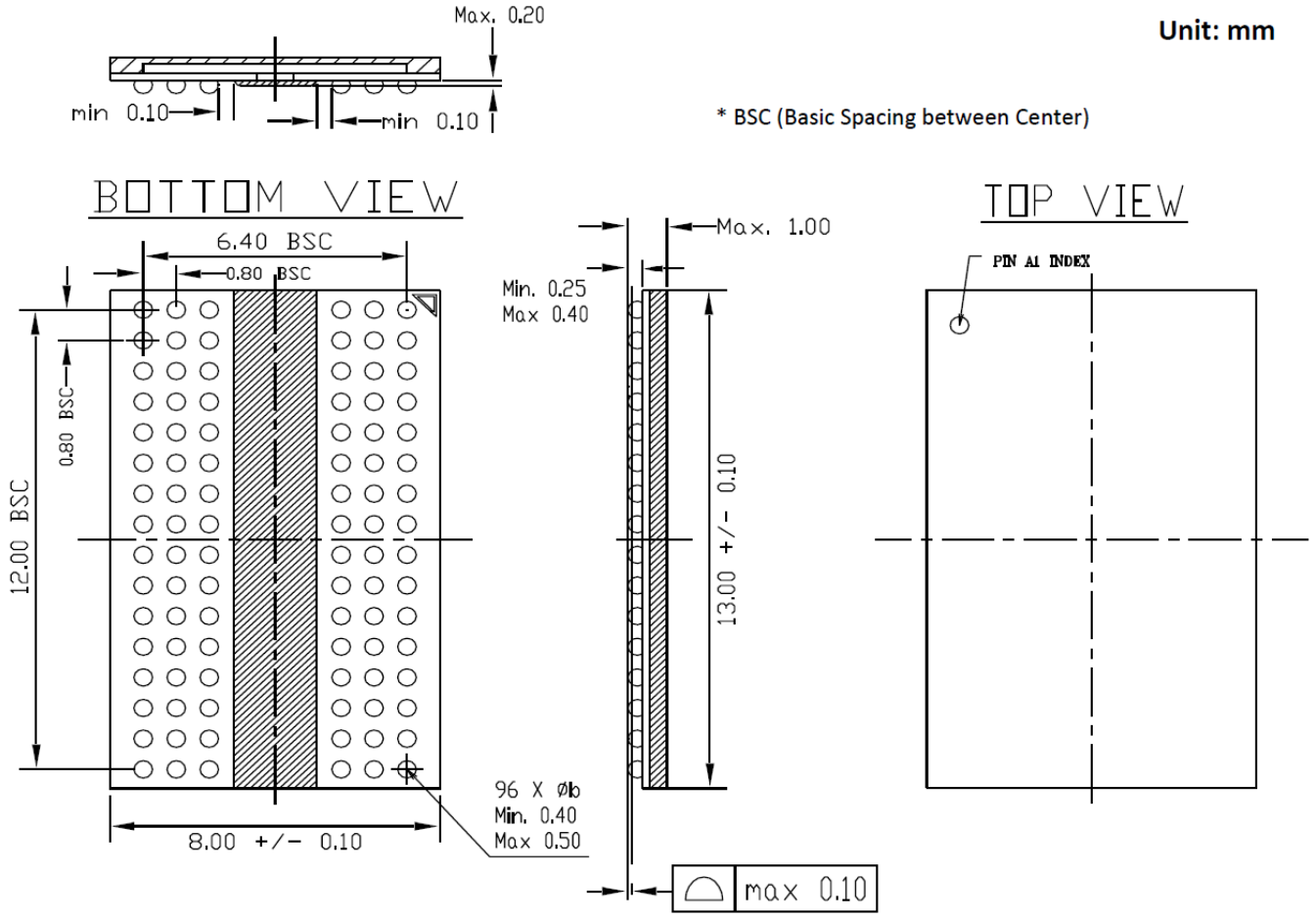
Note1: BA2, A3 - A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.
Note2: The predefined pattern will be used for read synchronization.
Note3: When MPR control is set for normal operation, ***MR3*** A[2] = 0, ***MR3*** A[1:0] will be ignored

Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to ***MR3*** Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (***MR3*** bit A2 = 0). Power-down mode, self-refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Package Description: 96Ball-FBGA(8x13mm)

Solder ball: Lead free (Sn-Ag-Cu)



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Dec. 2017	L.George	N/A
1.0	First SPEC. release.	Dec. 2017	L.George	N/A