# 64Mb (1M×4Bank×16) Synchronous DRAM

## Descriptions

The H2A164M1633B is Synchronous Dynamic Random Access Memory (SDRAM) organized as 1Mega words x 4 banks by 16 bits. All inputs and outputs are synchronized with the positive edge of the clock.

The 64Mb SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 3.3V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVTTL.

Available packages: TSOPII 54P 400mil.

- All Inputs are Sampled at the Rising Edge of the System Clock
- Auto Refresh and Self Refresh
- 4,096 Refresh Cycles / 64ms (15.625us)

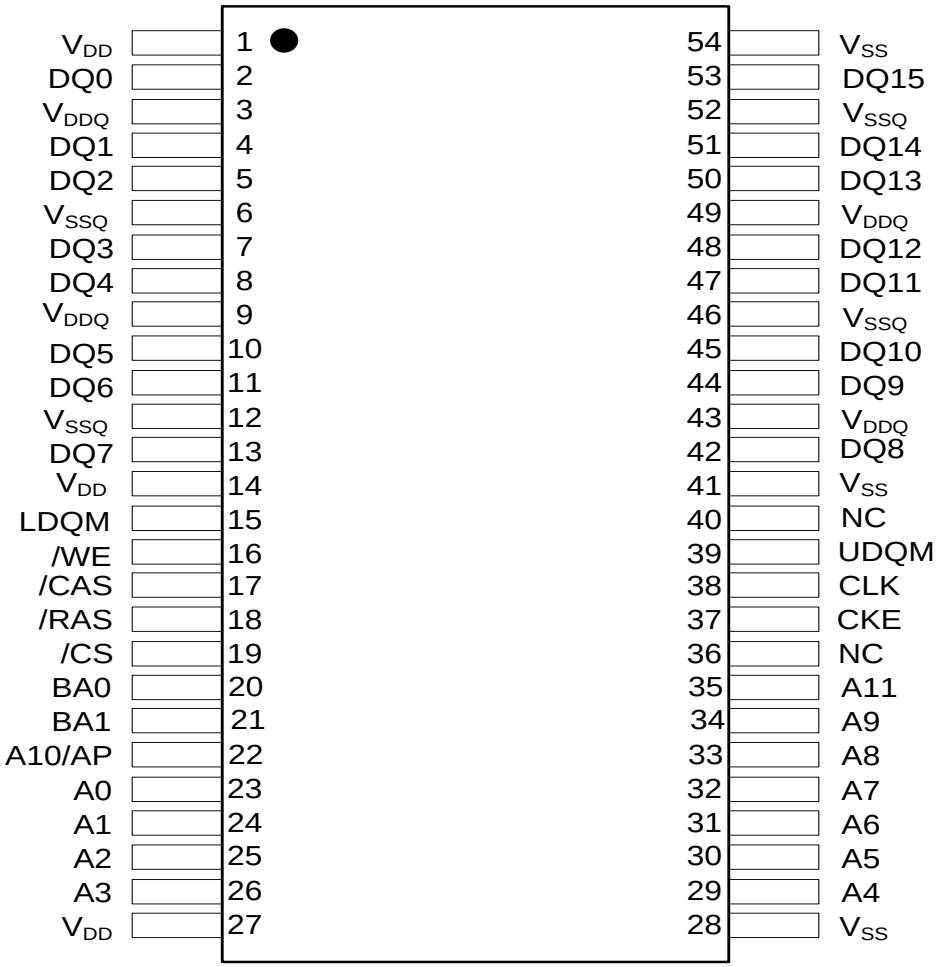
## Features

- Fully Synchronous to Positive Clock Edge
- Single 3.3V ±0.3V Power Supply
- LVTTL Compatible with Multiplexed Address
- Programmable Burst Length (B/L) - 1, 2, 4, 8 or Full Page
- Programmable CAS Latency (C/L) - 3
- Data Mask (DQM) for Read / Write Masking
- Programmable Wrap Sequence
  - – Sequential (B/L = 1/2/4/8/full Page)
  - – Interleave (B/L = 1/2/4/8)
- Burst Read with Single-bit Write Operation

## *Ordering Information*

| Part No | Organization | Max. Freq | Package | Grade |
|---|---|---|---|---|
| H2A164M1633BL1C | 4M X 16 | SDR-143MHz (3-3-3) | 54pin TSOP(II) | Commercial |
| H2A164M1633BM1C | 4M X 16 | SDR-166MHz (3-3-3) | 54pin TSOP(II) | Commercial |

## *Pin Assignment*




**54pin TSOP-II / (400mil × 875mil) / (0.8mm Pin pitch)**

## *Pin Description (Simplified)*

| Pin | Name | Function |
|---|---|---|
| 38 | CLK | **(System Clock)**<br>Master clock input (Active on the positive rising edge) |
| 19 | /CS | **(Chip Select)**<br>Selects chip when active |
| 37 | CKE | **(Clock Enable)**<br>Activates the CLK when “H” and deactivates when “L”.<br>CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. |
| 23~26, 22, 29~35 | A0~A11 | **(Address)**<br>Row address (A0 to A11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge.<br>CA (CA0 to CA7) is determined by A0 to A7 level at the read or write command cycle CLK rising edge.<br>And this column address becomes burst access start address.<br>A10 defines the pre-charge mode. When A10= High at the pre-charge command cycle, all banks are pre-charged.<br>But when A10= Low at the pre-charge command cycle, only the bank that is selected by BA0/BA1 is pre-charged. |
| 20, 21 | BA0, BA1 | **(Bank Address)**<br>Selects which bank is to be active. |
| 18 | /RAS | **(Row Address Strobe)**<br>Latches Row Addresses on the positive rising edge of the CLK with /RAS “L”. Enables row access & pre-charge. |
| 17 | /CAS | **(Column Address Strobe)**<br>Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access. |
| 16 | /WE | **(Write Enable)**<br>Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access. |
| 39/15 | UDQM / LDQM | **(Data Input / Output Mask)**<br>DQM controls I/O buffers. |
| 2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53 | DQ0~DQ15 | **(Data Input/Output)**<br>DQ pins have the same function as I/O pins on a conventional DRAM. |
| 1,14,27/ 28,41,54 | $V_{DD}$ / $V_{SS}$ | **(Power Supply/Ground)**<br>$V_{DD}$ and $V_{SS}$ are power supply pins for internal circuits. |
| 3, 9, 43, 49/ 6, 12, 46, 52 | $V_{DDQ}$ / $V_{SSQ}$ | **(Power Supply/Ground)**<br>$V_{DDQ}$ and $V_{SSQ}$ are power supply pins for the output buffers. |
| 36,40 | NC | **(No Connection)**<br>This pin is recommended to be left No Connection on the device. |

## *Absolute Maximum Rating*

| Symbol | Item | Rating | | Units |
|---|---|---|---|---|
| $V_{IN}$, $V_{OUT}$ | Input, Output Voltage | -0.5 ~ $V_{DD}$+0.5 (≦ 4.6V max.) | | V |
| $V_{DD}$, $V_{DDQ}$ | Power Supply Voltage | -0.3 ~ +4.6 | | V |
| $T_{OP}$ | Operating Temperature Range | Commercial | 0 ~ +70 | °C |
| $T_{STG}$ | Storage Temperature Range | -55 ~ +150 | | °C |
| $P_D$ | Power Dissipation | 1 | | W |
| $I_{OS}$ | Short Circuit Current | 50 | | mA |

***Note:*** Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## *Capacitance ($V_{CC}$=3.3V, f=1MHz, $T_A$=25°C)*

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{CLK}$ | Clock Capacitance | 2.5 | - | 4 | pF |
| $C_I$ | Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU | 2.5 | - | 4 | pF |
| $C_O$ | Input / Output Capacitance | 4 | - | 6.5 | pF |

## *Recommended DC Operating Conditions ($T_A$=-0°C ~+70°C)*

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{DDQ}$ | Power Supply Voltage (for I/O Buffer) | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | Input Logic High Voltage | 2.0 | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input Logic Low Voltage | -0.3 | | 0.8 | V |

***Note:*** * All voltages referred to $V_{SS}$.

* $V_{IH}$ (max.) = $V_{DD}$ / $V_{DDQ}$ +1.5V for pulse width ≦ 5ns

* $V_{IL}$ (min.) = $V_{DD}$ / $V_{SSQ}$ -1.5V for pulse width ≦ 5ns

## *Recommended DC Operating Conditions*

($V_{DD}$=3.3V±0.3V, $T_A$=0°C ~ 70°C)

| Symbol | Parameter | Test Conditions | Max. | | Units |
|---|---|---|---|---|---|
| | | | 143 | 166 | |
| $I_{CC1}$ | Operating Current<br>tCK = min., tRC = min.<br>Active precharge command cycling without burst operation ***(Note 3)*** | 1 Bank Operation | 45 | 50 | mA |
| $I_{CC2}$ | Standby Current<br>tCK = min., /CS = VIH<br>VIH/L = VIH (min.)/VIL (max.)<br>***(Note 3)*** | CKE = VIH | 20 | 25 | mA |
| $I_{CC2P}$ | Bank: Inactive State ***(Note 3)*** | CKE = VIL<br>(Power Down mode) | 2 | 2 | mA |
| $I_{CC2S}$ | Standby Current<br>CLK = VIL, /CS = VIH<br>VIH/L=VIH (min.)/VIL (max.) | CKE = VIH | 12 | 12 | mA |
| $I_{CC2PS}$ | Bank: Inactive State | CKE = VIL<br>(Power Down mode) | 2 | 2 | mA |
| $I_{CC3}$ | No Operating Current<br>tCK = min., /CS = VIH (min.) | CKE = VIH | 30 | 35 | mA |
| $I_{CC3P}$ | Bank: Active State (4 Banks) | CKE = VIL<br>(Power Down mode) | 12 | 12 | mA |
| $I_{CC4}$ | Burst Operating Current<br>(tCK = min.)<br>Read/ Write command cycling ***(Note 3,4)*** | | 70 | 75 | mA |
| $I_{CC5}$ | Auto Refresh Current<br>(tCK = min.)<br>Auto refresh command cycling ***(Note 3)*** | | 55 | 60 | mA |
| $I_{CC6}$ | Self Refresh Current<br>(CKE = 0.2V)<br>Self refresh mode | | 2 | 2 | mA |

*All voltages referenced to $V_{SS}$.

***Note 1:*** $I_{CC1}$ depends on output loading and cycle rates.

Specified values are obtained with the output open.

Input signals are changed only one time during $t_{CK}$ (min.)

***Note 2:*** $I_{CC4}$ depends on output loading and cycle rates.

Specified values are obtained with the output open.

Input signals are changed only one time during $t_{CK}$ (min.)

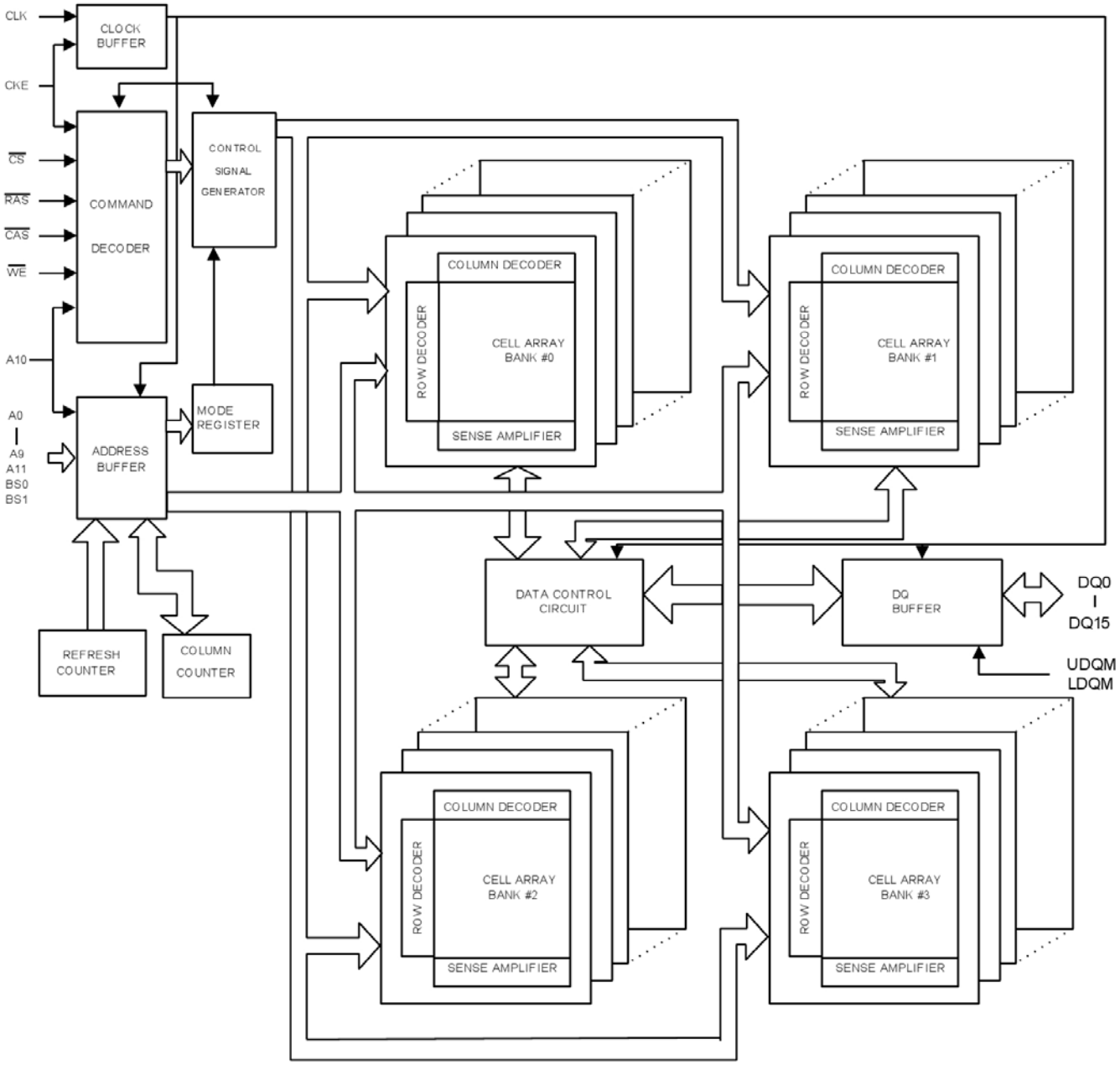
***Note 3:*** Input signals are changed only one time during $t_{CK}$ (min.)

***Note 4:*** Standard power version.

## *Recommended DC Operating Conditions (Continued)*

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | $0 \le V_I \le V_{DDQ}$, $V_{DDQ}=V_{DD}$<br>All other pins not under test=0V | -5 | - | 5 | uA |
| $I_{OL}$ | Output Leakage Current | $0 \le V_O \le V_{DDQ}$, $D_{OUT}$ is disabled | -5 | - | 5 | uA |
| $V_{OH}$ | High Level Output Voltage | $I_O$=-4mA | 2.4 | - | - | V |
| $V_{OL}$ | Low Level Output Voltage | $I_O$=+4mA | - | - | 0.4 | V |

## *Block Diagram*

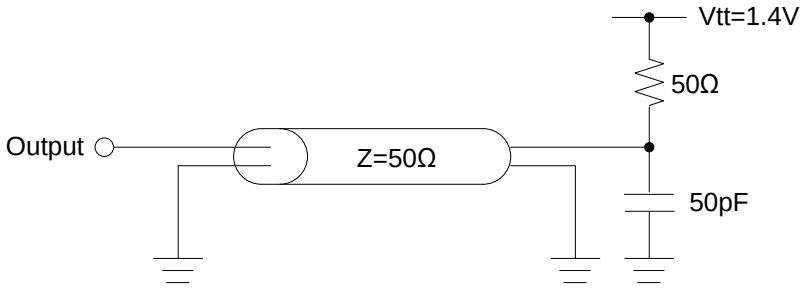



NOTE:
The cell array configuration is 4096 * 256 * 16

## AC Operating Test Conditions

($V_{DD}$=3.3V±0.3V, $T_A$=0°C ~70°C)

| Item | Conditions |
|---|---|
| Output Reference Level | 1.4V/1.4V |
| Output Load | See diagram as below |
| Input Signal Level | 2.4V/0.4V |
| Transition Time of Input Signals | 2ns |
| Input Reference Level | 1.4V |




## AC Operating Test Characteristics

($V_{DD}$=3.3V±0.3V, $T_A$=0°C ~70°C)

| Symbol | Parameter | | 166MHz | | 143MHz | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{CK}$ | Clock Cycle Time | CL=3 | 6 | 1000 | 7 | 1000 | ns |
| | | CL=2 | 8 | 1000 | 9 | 1000 | |
| $t_{AC}$ | Access Time form CLK | CL=3 | - | 5 | - | 5 | ns |
| | | CL=2 | - | 6 | - | 6 | |
| $t_{CH}$ | CLK High Level Width | | 2 | - | 2 | - | ns |
| $t_{CL}$ | CLK Low Level Width | | 2 | - | 2 | - | ns |
| $t_{OH}$ | Data-out Hold Time | CL=3 | - | - | - | - | ns |
| | | CL=2 | - | - | - | - | |
| $t_{HZ}$ | Data-out High Impedance Time *(Note 5)* | CL=3 | 2 | 5 | 2 | 6 | ns |
| | | CL=2 | - | - | - | - | |
| $t_{LZ}$ | Data-out Low Impedance Time | | 0 | - | 0 | - | ns |
| $t_{IH}$ | Input Hold Time | | 1 | - | 1 | - | ns |
| $t_{IS}$ | Input Setup Time | | 1.5 | - | 2 | - | ns |

* All voltages referenced to $V_{SS}$.

***Note 5:*** $t_{HZ}$ defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.

## AC Operating Test Characteristics (Continued)

($V_{DD}$=3.3V±0.3V, $T_A$=0°C ~70°C)

| Symbol | Parameter | | 166MHz | | 143MHz | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | ACTIVE to ACTIVE Command Period *(Note 6)* | | 60 | | 63 | | ns |
| $t_{RAS}$ | ACTIVE to PRECHARGE Command Period *(Note 6)* | | 40 | 100k | 42 | 100k | ns |
| $t_{RP}$ | PRECHARGE to ACTIVE Command Period *(Note 6)* | | 15 | | 18 | | ns |
| $t_{RCD}$ | ACTIVE to READ/WRITE Delay Time *(Note 6)* | | 15 | | 20 | | ns |
| $t_{RRD}$ | ACTIVE(one) to ACTIVE(another) Command *(Note 6)* | | 12 | | 14 | | ns |
| $t_{CCD}$ | READ/WRITE Command to READ/WRITE Command | | 1 | | 1 | | CLK |
| $t_{DPL}$ | Date-in to PRECHARGE Command | | 2 | | 2 | | CLK |
| $t_{BDL}$ | Date-in to BURST Stop Command | | 1 | | 1 | | CLK |
| $t_{ROH}$ | Data-out to High Impedance from PRECHARGE Command | CL=3 | 3 | | 3 | | CLK |
| | | CL=2 | 2 | | 2 | | |
| $t_{REF}$ | Refresh Time (4,096 cycle) | | | 64 | | 64 | ms |

* All voltages referenced to $V_{SS}$.

***Note 6:*** These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows:

The number of clock cycles = Specified value of timing/clock period (Count Fractions as a whole number)

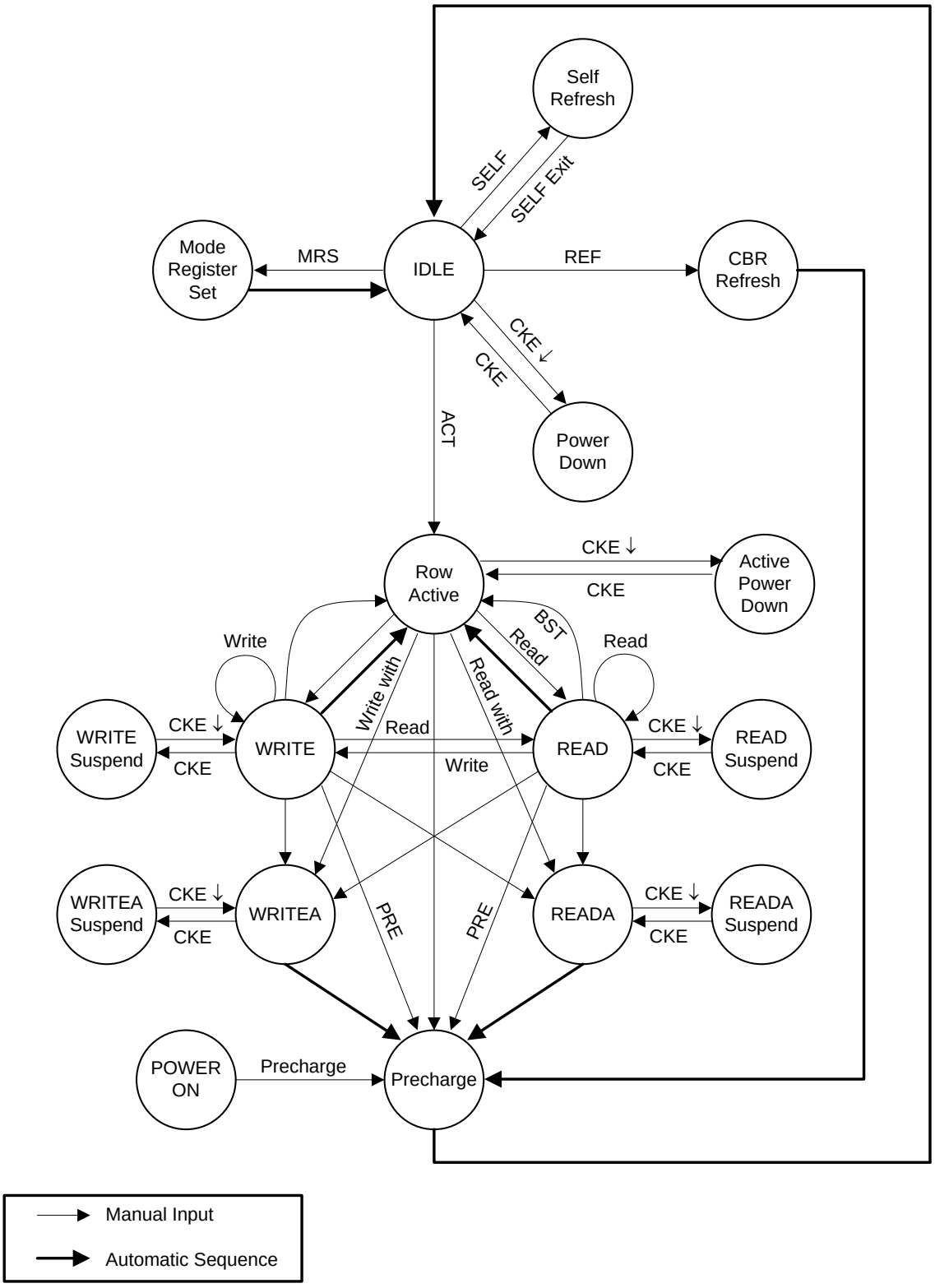
## Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. (Like a conventional DRAM) During power on, all $V_{DD}$ and $V_{DDQ}$ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed $V_{DD}$+0.3V on any of the input pins or $V_{DD}$ supplies. (CLK signal started at same time)

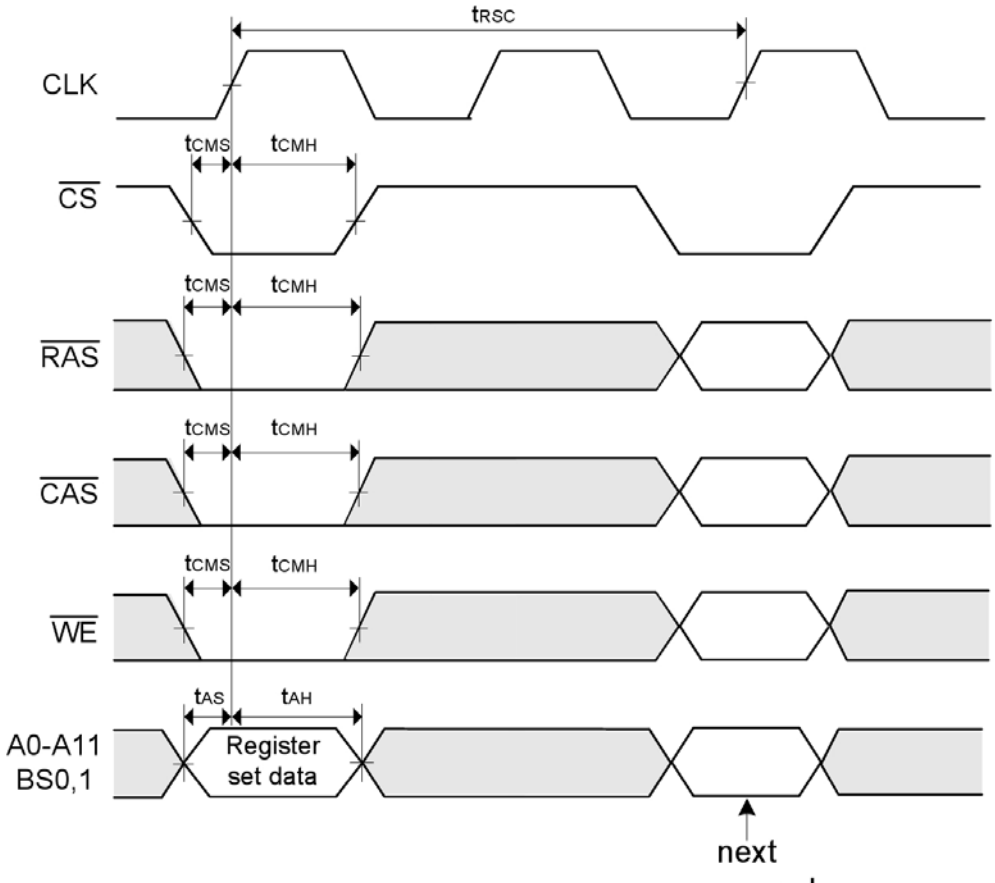
After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command.

To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

## *Simplified State Diagram*



## *Address Input for Mode Register Set*




| | | |
|---|---|---|
| A0 | Burst Length | |
| A1 | | |
| A2 | | |
| A3 | Addressing Mode | |
| A4 | CAS Latency | |
| A5 | | |
| A6 | | |
| A7 | "0" | (Test Mode) |
| A8 | "0" | Reserved |
| A9 | Write Mode | |
| A10 | "0" | Reserved |
| A11 | "0" | |
| BS0 | "0" | |
| BS1 | "0" | |

| | Burst Length | |
|---|---|---|
| A2 A1 A0 | Sequential | Interleave |
| 0 0 0 | 1 | 1 |
| 0 0 1 | 2 | 2 |
| 0 1 0 | 4 | 4 |
| 0 1 1 | 8 | 8 |
| 1 0 0 | Reserved | Reserved |
| 1 0 1 | | |
| 1 1 0 | | |
| 1 1 1 | Full Page | |

| A3 | Addressing Mode |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A6 A5 A4 | CAS Latency |
|---|---|
| 0 0 0 | Reserved |
| 0 0 1 | Reserved |
| 0 1 0 | 2 |
| 0 1 1 | 3 |
| 1 0 0 | Reserved |

| A9 | Single Write Mode |
|---|---|
| 0 | Burst read and Burst write |
| 1 | Burst read and single write |

* "Reserved" should stay "0" during MRS cycle.

## *Burst Type (A3)*

| Burst Length | A2 | A1 | A0 | Sequential Addressing | Interleave Addressing |
|---|---|---|---|---|---|
| 2 | X | X | 0 | 0 1 | 0 1 |
| | X | X | 0 | 1 0 | 1 0 |
| 4 | X | 0 | 0 | 0 1 2 3 | 0 1 2 3 |
| | X | 0 | 1 | 1 2 3 0 | 1 0 3 2 |
| | X | 1 | 0 | 2 3 0 1 | 2 3 0 1 |
| | X | 1 | 1 | 3 0 1 2 | 3 2 1 0 |
| 8 | 0 | 0 | 0 | 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 |
| | 0 | 0 | 1 | 1 2 3 4 5 6 7 0 | 1 0 3 2 5 4 7 6 |
| | 0 | 1 | 0 | 2 3 4 5 6 7 0 1 | 2 3 0 1 6 7 4 5 |
| | 0 | 1 | 1 | 3 4 5 6 7 0 1 2 | 3 2 1 0 7 6 5 4 |
| | 1 | 0 | 0 | 4 5 6 7 0 1 2 3 | 4 5 6 7 0 1 2 3 |
| | 1 | 0 | 1 | 5 6 7 0 1 2 3 4 | 5 4 7 6 1 0 3 2 |
| | 1 | 1 | 0 | 6 7 0 1 2 3 4 5 | 6 7 4 5 2 3 0 1 |
| | 1 | 1 | 1 | 7 0 1 2 3 4 5 6 | 7 6 5 4 3 2 1 0 |
| Full Page* | n | n | n | Cn Cn+1 Cn+2…… | - |

* Page length is a function of I/O organization and column addressing ×16 (CA0 ~ CA7):

Full page = 256bits

## *1. Command Truth Table*

| Command | Symbol | CKE | | /CS | /RAS | /CAS | /WE | BA0, BA1 | A10 | A11, A9~A10 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | n-1 | n | | | | | | | |
| Ignore Command | DESL | H | X | H | X | X | X | X | X | X |
| No Operation | NOP | H | X | L | H | H | H | X | X | X |
| Burst Stop | BSTH | H | X | L | H | H | L | X | X | X |
| Read | READ | H | X | L | H | L | H | V | L | V |
| Read with Auto Pre-charge | READA | H | X | L | H | L | H | V | H | V |
| Write | WRIT | H | X | L | H | L | L | V | L | V |
| Write with Auto Pre-charge | WRITA | H | X | L | L | H | H | V | H | V |
| Bank Activate | ACT | H | X | L | L | H | H | V | V | V |
| Pre-charge Select Bank | PRE | H | X | L | L | H | L | V | L | X |
| Pre-charge All Banks | PALL | H | X | L | L | H | L | X | H | X |
| Mode Register Set | MRS | H | X | L | L | L | L | L | L | V |

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

## 2. DQM Truth Table

| Command | Symbol | CKE | | /CS |
|---|---|---|---|---|
| | | n-1 | n | |
| Data Write/Output Enable | ENB | H | X | H |
| Data Mask/Output Disable | MASK | H | X | L |
| Upper Byte Write Enable/Output Enable | BSTH | H | X | L |
| Read | READ | H | X | L |
| Read with Auto Pre-charge | READA | H | X | L |
| Write | WRIT | H | X | L |
| Write with Auto Pre-charge | WRITA | H | X | L |
| Bank Activate | ACT | H | X | L |
| Pre-charge Select Bank | PRE | H | X | L |
| Pre-charge All Banks | PALL | H | X | L |
| Mode Register Set | MRS | H | X | L |

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

## 3. CKE Truth Table

| Item | Command | Symbol | CKE | | /CS | /RAS | /CAS | /WE | Addr. |
|---|---|---|---|---|---|---|---|---|---|
| | | | n- | n | | | | | |
| Activating | Clock Suspend Mode Entry | | H | L | X | X | X | X | X |
| Any | Clock Suspend Mode | | L | L | X | X | X | X | X |
| Clock Suspend | Clock Suspend Mode Exit | | L | H | X | X | X | X | X |
| Idle | CBR Refresh Command | REF | H | H | L | L | L | H | X |
| Idle | Self Refresh Entry | SELF | H | L | L | L | L | H | X |
| Self Refresh | Self Refresh Exit | | L | H | L | H | H | H | X |
| | | | L | H | H | X | X | X | X |
| Idle | Power Down Entry | | H | L | X | X | X | X | X |
| Power Down | Power Down Exit | | L | H | X | X | X | X | X |

**Remark** H = High level, L = Low level, X = High or Low level (Don't care)

## 4. Operative Command Table (Note 7)

| Current State | /CS | /R | /C | /W | Addr. | Command | Action |
|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X | DESL | Nop or power down (Note 8) |
| | L | H | H | X | X | NOP or BST | Nop or power down (Note 8) |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL (Note 9) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL (Note 9) |
| | L | L | H | H | BA/RA | ACT | Row activating |
| | L | L | H | L | BA, A10 | PRE/PALL | Nop |
| | L | L | L | H | X | REF/SELF | Refresh or self refresh (Note 10) |
| | L | L | L | L | Op-Code | MRS | Mode register accessing |
| Row Active | H | X | X | X | X | DESL | Nop |
| | L | H | H | X | X | NOP or BST | Nop |
| | L | H | L | H | BA/CA/A10 | READ/READA | Begin read: Determine AP (Note 11) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | Begin write: Determine AP (Note 11) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | Pre-charge (Note 12) |
| | L | L | L | H | X | REF/SELF | ILLEGAL (Note 10) |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Read | H | X | X | X | X | DESL | Continue burst to end → Row active |
| | L | H | H | H | X | NOP | Continue burst to end → Row active |
| | L | H | H | L | X | BST | Burst stop → Row active |
| | L | H | L | H | BA/CA/A10 | READ/READA | Terminate burst, new read: Determine AP (Note 13) |
| | L | L | L | L | BA/CA/A10 | WRIT/WRITA | Terminate burst, start write: Determine AP (Note 13, 14) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | Terminate burst, pre-charging (Note 10) |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Write | H | X | X | X | X | DESL | Continue burst to end → Write recovering |
| | L | H | H | H | X | NOP | Continue burst to end → Write recovering |
| | L | H | H | L | X | BST | Burst stop → Row active |
| | L | H | L | H | BA/CA/A10 | READ/READA | Terminate burst, start read: Determine AP 7, 8 (Note 13, 14) |
| | L | L | L | L | BA/CA/A10 | WRIT/WRITA | Terminate burst, new write: Determine AP 7 (Note 13) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | Terminate burst, pre-charging (Note 15) |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |

**Remark** H = High level, L = Low level, X = High or Low level (Don't care)

## 4. Operative Command Table (Continued) (Note 7)

| Current State | /CS | /R | /C | /W | Addr. | Command | Action |
|---|---|---|---|---|---|---|---|
| Read with AP | H | X | X | X | X | DESL | Continue burst to end → Pre-charging |
| | L | H | H | H | X | NOP | Continue burst to end → Pre-charging |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL (Note 9) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL (Note 9) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL (Note 9) |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Write with AP | H | X | X | X | X | DESL | Burst to end → Write recovering with auto pre-charge |
| | L | H | H | H | X | NOP | Continue burst to end → Write recovering with auto pre-charge |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL (Note 9) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL (Note 9) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL (Note 9) |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Pre-charging | H | X | X | X | X | DESL | Nop → Enter idle after $t_{RP}$ |
| | L | H | H | H | X | NOP | Nop → Enter idle after $t_{RP}$ |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL (Note 9) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL (Note 9) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | Nop → Enter idle after $t_{RP}$ |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Row Activating | H | X | X | X | X | DESL | Nop → Enter idle after $t_{RCD}$ |
| | L | H | H | H | X | NOP | Nop → Enter idle after $t_{RCD}$ |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL (Note 9) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL (Note 9) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9, 16) |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL (Note 9) |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |

**Remark** H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

## 4. Operative Command Table (Continued) (Note 7)

| Current State | /CS | /R | /C | /W | Addr. | Command | Action |
|---|---|---|---|---|---|---|---|
| Write Recovering | H | X | X | X | X | DESL | Nop → Enter row active after $t_{DPL}$ |
| | L | H | H | H | X | NOP | Nop → Enter row active after $t_{DPL}$ |
| | L | H | H | L | X | BST | Nop → Enter row active after $t_{DPL}$ |
| | L | H | L | H | BA/CA/A10 | READ/READA | Start read, Determine AP |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | New write, Determine AP (Note 14) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL (Note 9) |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Write Recovering with AP | H | X | X | X | X | DESL | Nop → Enter pre-charge after $t_{DPL}$ |
| | L | H | H | H | X | NOP | Nop → Enter pre-charge after $t_{DPL}$ |
| | L | H | H | L | X | BST | Nop → Enter pre-charge after $t_{DPL}$ |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL (Note 9, 14) |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL (Note 9) |
| | L | L | H | H | BA/RA | ACT | ILLEGAL (Note 9) |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL |
| | L | L | L | H | X | REF/SELF | ILLEGAL |
| | L | L | L | L | Op-Code | MRS | ILLEGAL |
| Refreshing | H | X | X | X | X | DESL | Nop → Enter idle after $t_{RC}$ |
| | L | H | H | X | X | NOP/BST | Nop → Enter idle after $t_{RC}$ |
| | L | H | L | X | X | READ/WRIT | ILLEGAL |
| | L | L | H | X | X | ACT/PRE/PALL | ILLEGAL |
| | L | L | L | X | X | REF/SELF/MRS | ILLEGAL |
| Mode Register Accessing | H | X | X | X | X | DESL | Nop |
| | L | H | H | H | X | NOP | Nop |
| | L | H | H | L | X | BST | ILLEGAL |
| | L | H | L | X | X | READ/WRIT | ILLEGAL |
| | L | L | X | X | X | ACT/PRE/PALL/ REF/SELF/MRS | ILLEGAL |

**Remark** H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

***Note 7:*** All entries assume that CKE was active (High level) during the preceding clock cycle.

***Note 8:*** If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode.

All input buffers except CKE will be disabled.

***Note 9:*** Illegal to bank in specified states;

Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

***Note 10:*** If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode.

All input buffers except CKE will be disabled.

***Note 11:*** Illegal if $t_{RCD}$ is not satisfied.

***Note 12:*** Illegal if $t_{RAS}$ is not satisfied.

***Note 13:*** Must satisfy burst interrupt condition.

***Note 14:*** Must satisfy bus contention, bus turn around, and/or write recovery requirements.

***Note 15:*** Must mask preceding data which don't satisfy $t_{DPL}$.

***Note 16:*** Illegal if $t_{RRD}$ is not satisfied.

## 5. Command Truth Table for CKE

| Current State | CKE | | /CS | /R | /C | /W | Addr. | Action |
|---|---|---|---|---|---|---|---|---|
| | n-1 | n | | | | | | |
| Self Refresh | H | X | X | X | X | X | X | INVALID, CLK(n-1) would exit self refresh |
| | L | H | H | X | X | X | X | Self refresh recovery |
| | L | H | L | H | H | X | X | Self refresh recovery |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | Maintain self refresh |
| Self Refresh Recovery | H | H | H | X | X | X | X | Idle after $t_{RC}$ |
| | H | H | L | H | H | X | X | Idle after $t_{RC}$ |
| | H | H | L | H | L | X | X | ILLEGAL |
| | H | H | L | L | X | X | X | ILLEGAL |
| | H | L | H | X | X | X | X | ILLEGAL |
| | H | L | L | H | H | X | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | X | X | X | ILLEGAL |
| Power Down | H | X | X | X | X | X | X | INVALID, CLK(n-1) would exit power down |
| | L | H | X | X | X | X | X | Exit power down → Idle |
| | L | L | X | X | X | X | X | Maintain power down mode |
| Both Banks Idle | H | H | H | X | X | X | | Refer to operations in Operative Command Table |
| | H | H | L | H | X | X | | |
| | H | H | L | L | H | X | | |
| | H | H | L | L | L | H | X | Refresh |
| | H | H | L | L | L | L | Op-Code | Refer to operations in Operative Command Table |
| | H | L | H | X | X | X | | |
| | H | L | L | H | X | X | | |
| | H | L | L | L | H | X | | |
| | H | L | L | L | L | H | X | Self refresh *(Note 17)* |
| | H | L | L | L | L | L | Op-Code | Refer to operations in Operative Command Table |
| | L | X | X | X | X | X | X | Power down *(Note 17)* |
| Row Active | H | X | X | X | X | X | X | Refer to operations in Operative Command Table |
| | L | X | X | X | X | X | X | Power down *(Note 17)* |
| Any State Other than Listed above | H | H | X | X | X | X | | Refer to operations in Operative Command Table |
| | H | L | X | X | X | X | X | Begin clock suspend next cycle *(Note 18)* |
| | L | H | X | X | X | X | X | Exit clock suspend next cycle |
| | L | L | X | X | X | X | X | Maintain clock suspend |

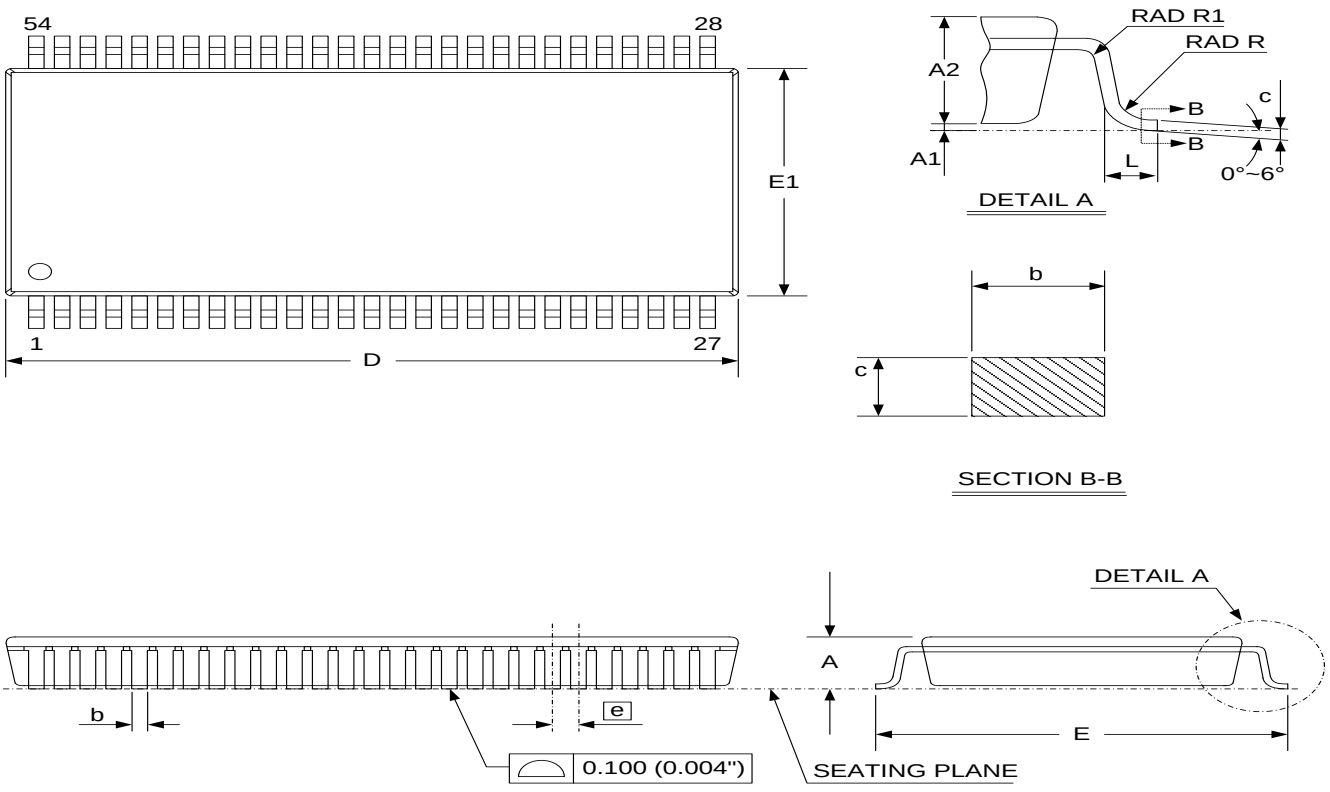
**Remark:** H = High level, L = Low level, X = High or Low level (Don't care)

***Notes 17:*** Self refresh can be entered only from the both banks idle state.

Power down can be entered only from both banks idle or row active state.

***Notes 18:*** Must be legal command as defined in Operative Command Table

## *Package Description*




| DIM | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | – | – | 1.20 | – | – | 0.047 |
| A1 | 0.05 | – | 0.15 | 0.002 | – | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | – | 0.45 | 0.012 | – | 0.018 |
| c | 0.12 | – | 0.21 | 0.005 | – | 0.008 |
| D | 22.09 | 22.22 | 22.35 | 0.870 | 0.875 | 0.880 |
| e | 0.80 BASIC | | | 0.0315 BASIC | | |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| R | 0.12 | – | 0.25 | 0.005 | – | 0.010 |
| R1 | 0.12 | – | – | 0.005 | – | – |

* Controlling dimension: millimeters

* Dimension D does not include mold protrusion. Mold protrusion shall not exceed 0.15mm (0.006”) per side. Dimension E1 does not include interlead protrusion. Interlead protrusion shall not exceed 0.25mm (0.01”) per side.

* Dimension b does not include dambar protrusions/intrusion. Allowable dambar protrusion shall not cause the lead to be wider than the MAX b dimension by more than 0.13mm. Dambar intrusion shall not cause the lead to be narrower than the MIN b dimension by more than 0.07mm.

## *Revision History*

| Revision No. | History | Draft Date | Editor | Remark |
|---|---|---|---|---|
| 0.1 | Initial Release. | Sep. 2014 | David Chen | N/A |
| 1.0 | First SPEC. release. | Sep. 2014 | David Chen | N/A |