

**1Gb (4Mx8Banksx32)
Low Power DDR3 SDRAM**

Descriptions

This LPDDR3 is a high-speed SDRAM device internally configured as an 8-Bank memory and contains 1,073,741,824 bits.

This LPDDR3 device uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

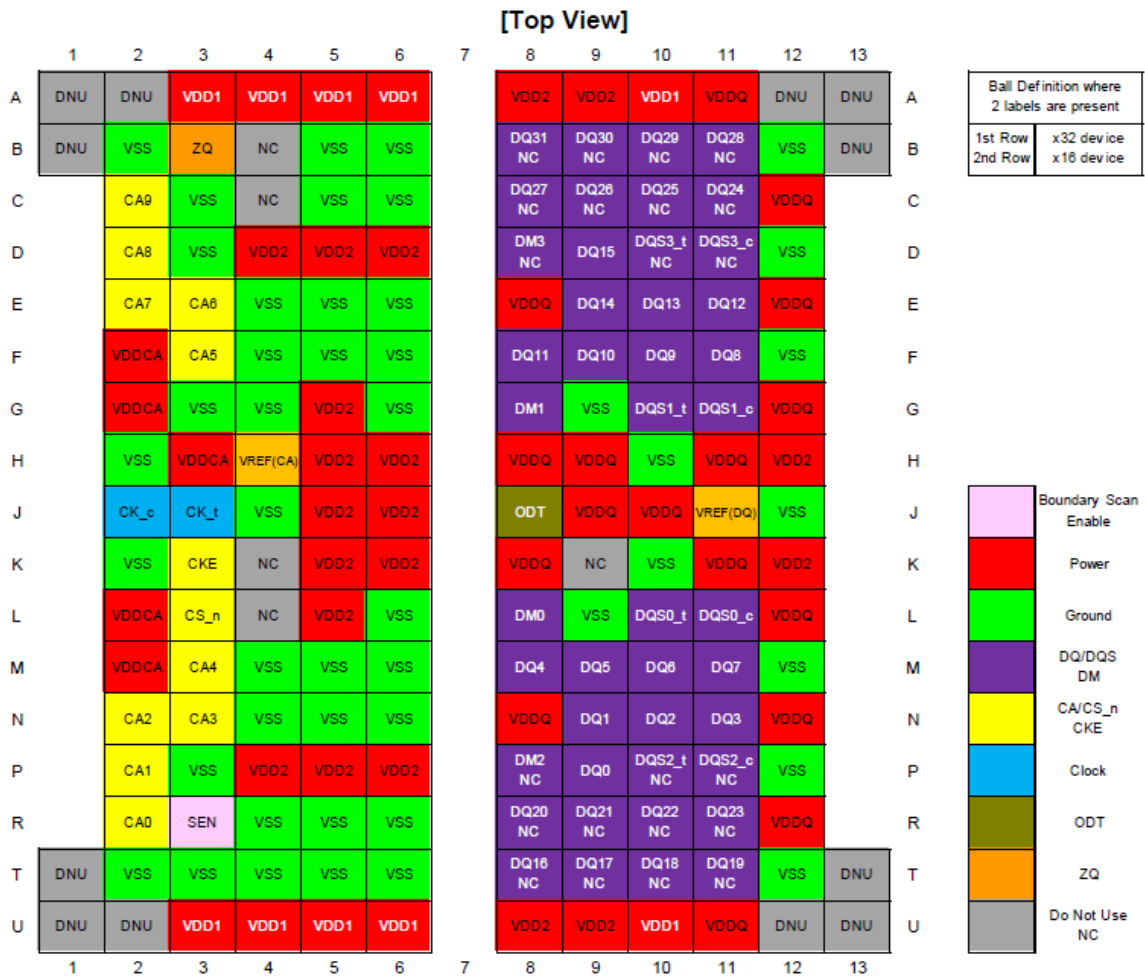
Features

- VDD1 = 1.7~1.95V
- VDD2/VDDCA/ VDDQ = 1.14V~1.30V
- Data width: x32
- Clock rate: up to 1066 MHz
- Data rate: up to 2133 Mbps
- 8 internal banks for concurrent operation
- 8n pre-fetch operation
- Burst length: 8
- Per Bank Refresh
- Partial Array Self-Refresh(PASR)
- On-die termination (ODT)
- Deep Power Down Mode (DPD Mode)
- Double data rate architecture
- Clock Stop capability
- Programmable Read and Write Latencies (RL/WL)
- Bidirectional differential data strobe
- VFBGA178 (11mm x11.5mm)

Ordering Information

Part No	Organization	Max. Data Rate	Package	Grade
H2A801G32B6BFHC	32M X 32	LPDDR3-1600	178Ball BGA,11x11.5mm	Commercial
H2A801G32B6BGHC	32M X 32	LPDDR3-1866		Commercial
H2A801G32B6BHHC	32M X 32	LPDDR3-2133		Commercial

Pin Assignment



178-Ball FBGA

Pin Description (Simplified)

Name	Type	Description
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See 7.5.1 “ Command Truth Table ” for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. See 7.5.1 “ Command Truth Table ” for command code descriptions. CS_n is sampled at the positive Clock edge.
CA[9:0]	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code. See 7.5.1 “ Command Truth Table ” for command code descriptions.
DQ[n:0]	I/O	Data Inputs/Output: Bi-directional data bus. DQ[15:0] for x16, DQ[31:0] for x32.
DQSn_t, DQSn_c	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15; DQS2_t and DQS2_c to the data on DQ16-23; DQS3_t and DQS3_c to the data on DQ24-31.
DMn	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
ODT	Input	On-Die Termination: This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
VDD1	Supply	Core Power Supply 1: Core Power supply.
VDD2	Supply	Core Power Supply 2: Core Power supply.
VDDCA	Supply	Input Receiver Power Supply: Power supply for CA[9:0], CKE, CS_n, CK_t, and CK_c input buffers.
VDDQ	Supply	I/O Power Supply: Power supply for Data input/output buffers.
VREF(CA)	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA[9:0], CKE, CS_n, CK_t, and CK_c input buffers.
VREF(DQ)	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
VSS	Supply	Ground: Ground of core logic, input receivers and data input/output buffers.
ZQ	I/O	Reference Pin for Output Drive Strength Calibration
SEN	Input	Scan Enable: SEN must be asserted HIGH for enabling boundary scan function. Must be tied to Ground or NC (No Connection) when not in use.
NC	--	No Connection
DNU	--	Do Not Use

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative	-0.4 ~ 1.6	V
V_{DD1}	Voltage on VDD1 pin relative	-0.4 ~ 2.3	V
V_{DD2}	Voltage on VDD2 pin relative	-0.4 ~ 1.6	V
V_{DDCA}	Voltage on VDDCA pin relative	-0.4 ~ 1.6	V
V_{DDQ}	Voltage on VDDQ pin relative	-0.4 ~ 1.6	V
T_{STG}	Storage Temperature (plastic)	-55 ~ 125	°C

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2: Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Note 3: $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$, provided that $V_{REFCA} \leq 300\text{mV}$.

Note 4: $V_{REFDQ} \leq 0.7 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$, provided that $V_{REFDQ} \leq 300\text{mV}$.

Capacitance

Symbol	Parameter	Min.	Max.	Units
C_{CK}	Input Capacitance (CK, /CK)	0.5	1.2	pF
C_{DCK}	Input capacitance delta, CK and /CK	0	0.15	pF
C_I	Input capacitance, all other input-only pins	0.5	1.1	pF
C_{DI}	Input capacitance delta, all other input-only pins	-0.2	0.2	pF
C_{IO}	Input/output capacitance, DQ, DM, DQS,/DQS	1.0	1.8	pF
C_{DDQS}	Input/output capacitance delta, DQS, /DQS	0	0.2	pF
C_{DIO}	Input/output capacitance delta, DQ, DM	-0.25	0.25	pF
C_{ZQ}	Input/output capacitance ZQ Pin	0	2.0	pF

Note 1: This parameter is not subject to production testing. It is verified by design and characterization.

Note 2: These parameters are measured on $f = 100\text{ MHz}$, $V_{OUT} = V_{DDQ}/2$, $T_A = +25\text{ °C}$.

Note 3: DOUT circuits are disabled.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V
V_{DD2}	Core Supply voltage 2	1.14	1.20	1.30	V
V_{DDCA}	Input Supply Voltage (Command/Address)	1.14	1.20	1.30	V
V_{DDQ}	I/O Supply voltage (DQ)	1.14	1.20	1.30	V

Notes: 1. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1 MHz at the DRAM package ball.

Notes: 2. VDD1 uses significantly less power than VDD2.

DC Characteristics

(IDD Specifications; VDD2, VDDQ, VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V)

Symbol		Supply	Speed			Unit
			1600	1866	2133	
IDD0	IDD01	VDD1	7	7	7	mA
	IDD02	VDD2	36	37	39	
	IDD0IN	VDDCA, VDDQ	8	8	8	
IDD2P	IDD2P1	VDD1	0.3	0.3	0.3	mA
	IDD2P2	VDD2	2	2	2	
	IDD2PIN	VDDCA, VDDQ	50	50	50	
IDD2PS	IDD2PS1	VDD1	0.3	0.3	0.3	mA
	IDD2PS2	VDD2	2	2	2	
	IDD2PSIN	VDDCA, VDDQ	50	50	50	
IDD2N	IDD2N1	VDD1	0.9	0.9	0.9	mA
	IDD2N2	VDD2	9	10	11	
	IDD2NIN	VDDCA, VDDQ	8	8	8	
IDD2NS	IDD2NS1	VDD1	0.9	0.9	0.9	mA
	IDD2NS2	VDD2	4	4	4	
	IDD2NSIN	VDDCA, VDDQ	8	8	8	
IDD3P	IDD3P1	VDD1	1.1	1.1	1.1	mA
	IDD3P2	VDD2	5	5	5	
	IDD3PIN	VDDCA, VDDQ	50	50	50	
IDD3PS	IDD3PS1	VDD1	1.1	1.1	1.1	mA
	IDD3PS2	VDD2	5	5	5	
	IDD3PSIN	VDDCA, VDDQ	50	50	50	
IDD3N	IDD3N1	VDD1	1.3	1.3	1.3	mA
	IDD3N2	VDD2	13	14	15	
	IDD3NIN	VDDCA, VDDQ	8	8	8	
IDD3NS	IDD3NS1	VDD1	1.3	1.3	1.3	mA
	IDD3NS2	VDD2	5	5	5	
	IDD3NSIN	VDDCA, VDDQ	8	8	8	
IDD4R	IDD4R1	VDD1	1.5	1.5	1.5	mA
	IDD4R2	VDD2	162	186	210	
	IDD4RIN	VDDCA	8	8	8	
IDD4W	IDD4W1	VDD1	1.5	1.5	1.5	mA
	IDD4W2	VDD2	163	189	215	
	IDD4WIN	VDDCA, VDDQ	34	34	34	

DC Characteristics(Continued)

(IDD Specifications; VDD2, VDDQ, VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V)

Symbol		Supply	Speed			Unit
			1600	1866	2133	
IDD5	IDD51	VDD1	18	18	18	mA
	IDD52	VDD2	60	62	63	
	IDD5IN	VDDCA , VDDQ	8	8	8	
IDD5AB	IDD5AB1	VDD1	1.22	1.22	1.22	mA
	IDD5AB2	VDD2	10.5	11	12	
	IDD5ABIN	VDDCA , VDDQ	8	8	8	
IDD5PB	IDD5PB1	VDD1	1.3	1.3	1.3	mA
	IDD5PB2	VDD2	11	11	12	
	IDD5PBIN	VDDCA , VDDQ	8	8	8	
IDD8	IDD81	VDD1	50	50	50	uA
	IDD82	VDD2	50	50	50	
	IDD8IN	VDDCA , VDDQ	50	50	50	

IDD6 Partial Array Self-refresh current; VDD2, VDDQ, VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V

PASR	Symbol	Supply	85°C	Condition	Unit
Full Array	IDD61	VDD1	600	Self refresh current CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	uA
	IDD62	VDD2	3000		
	IDD6IN	VDDCA , VDDQ	50		
1/2 Array	IDD61	VDD1	500		
	IDD62	VDD2	2500		
	IDD6IN	VDDCA , VDDQ	50		
1/4 Array	IDD61	VDD1	400		
	IDD62	VDD2	2300		
	IDD6IN	VDDCA , VDDQ	50		
1/8 Array	IDD61	VDD1	350		
	IDD62	VDD2	2200		
	IDD6IN	VDDCA , VDDQ	50		

Single-Ended AC and DC Output Levels

Symbol	Parameter	Value	Units	
$V_{OH(AC)}$	AC output HIGH measurement level	$V_{REF} + 0.12$	V	
$V_{OL(AC)}$	AC output LOW measurement level	$V_{REF} - 0.12$	V	
$V_{OH(DC)}$	DC output HIGH measurement level	$0.9 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output LOW measurement level	$0.1 \times V_{DDQ}$	V	
$V_{OL(DC)ODT,enabled}$	DC output LOW measurement level (for I-V curve linearity);ODT enabled DQS_t	$V_{DDQ} \times \{0.1 + 0.9 \times [RON / (RTT + RON)]\}$	V	
I_{OZ}	Output leakage current (DQ, DM, DQS) (DQ, DQS are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	Min	-5	uA
		Max	5	uA

Note 1: $I_{OH} = -0.1mA$.

Note 2: $I_{OL} = 0.1mA$.

Note 3: The minimum value is derived when using RTT,min and RON,max ($\pm 30\%$ uncalibrated, $\pm 15\%$ calibrated).

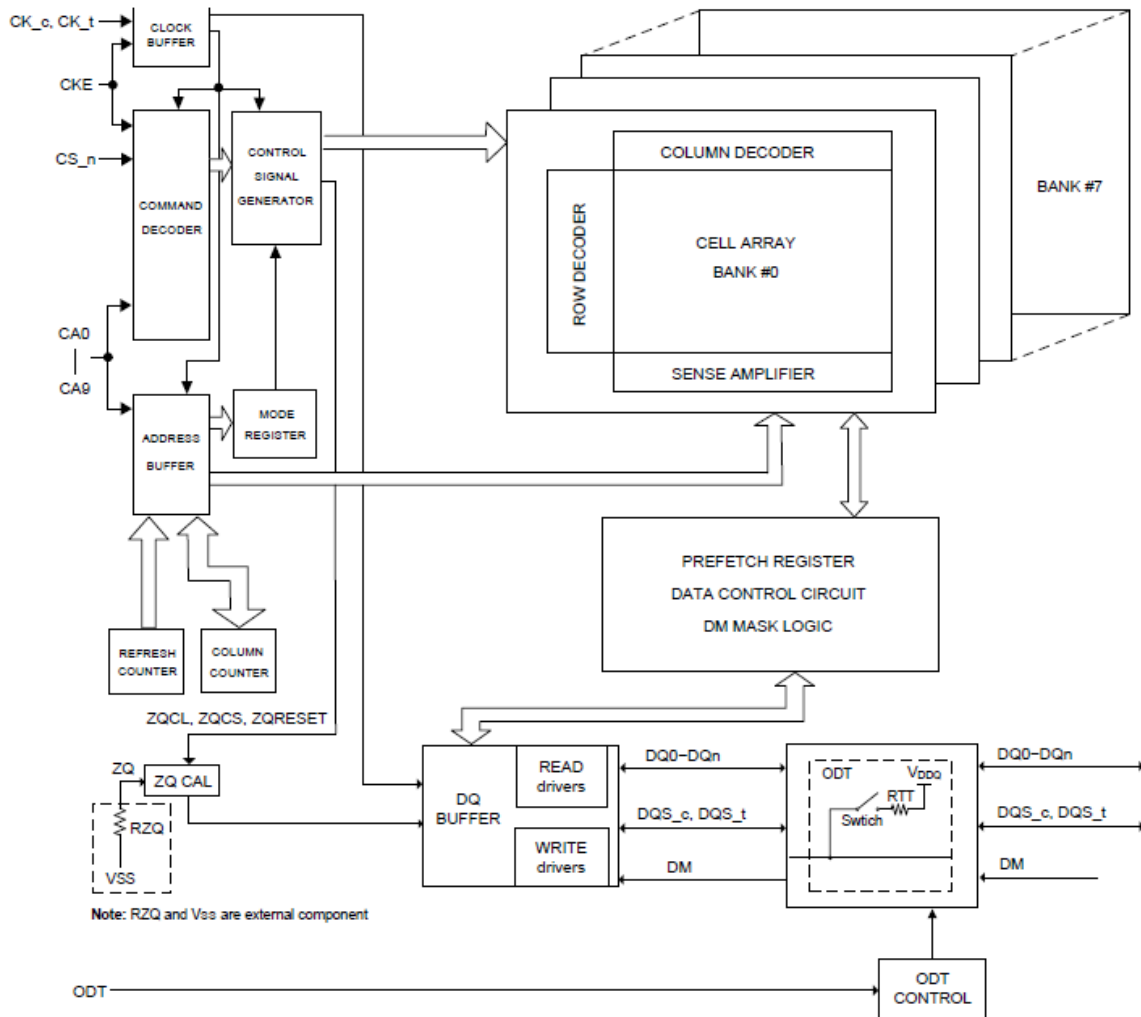
Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2 200-1066	Units
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level	$+ 0.20 \times V_{DDQ}$	V
$V_{OLdiff(AC)}$	AC differential output LOW measurement level	$- 0.20 \times V_{DDQ}$	V

Note 1: $I_{OH} = -0.1mA$.

Note 2: $I_{OL} = 0.1mA$.

BLOCK DIAGRAM



AC Characteristics
 $(V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14 \sim 1.30V, V_{DD1} = 1.70 \sim 1.95V)$

Parameter	Symbol	min / max	Data Rate			Unit
			1600	1866	2133	
Max. clock Frequency	fCK	-	800	933	1066	MHz
Clock Timing						
Average clock period	tCK(avg)	MIN	1.25	1.071	0.938	nS
		MAX	100			
Average HIGH pulse width	tCH(avg)	MIN	0.45			tCK(avg)
		MAX	0.55			
Average LOW pulse width	tCL(avg)	MIN	0.45			tCK(avg)
		MAX	0.55			
Absolute clock period	tCK(abs)	MIN	tCK(avg)min + tJIT(per)min			nS
Absolute clock HIGH pulse width	tCH(abs), allowed	MIN	0.43			tCK(avg)
		MAX	0.57			
Absolute clock LOW pulse width	tCL(abs), allowed	MIN	0.43			tCK(avg)
		MAX	0.57			
Clock Period Jitter (with supported jitter)	tJIT(per), allowed	MIN	-70	-60	-50	pS
		MAX	70	60	50	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	MAX	140	120	100	pS
Duty cycle Jitter (with supported jitter)	tJIT(duty), allowed	MIN	min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg)			pS
		MAX	max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg)			pS
Cumulative error across 2 cycles	tERR(2per), allowed	MIN	-103	-88	-74	pS
		MAX	103	88	74	
Cumulative error across 3 cycles	tERR(3per), allowed	MIN	-122	-105	-87	pS
		MAX	122	105	87	
Cumulative error across 4 cycles	tERR(4per), allowed	MIN	-136	-117	-97	pS
		MAX	136	117	97	
Cumulative error across 5 cycles	tERR(5per), allowed	MIN	-147	-126	-105	pS
		MAX	147	126	105	
Cumulative error across 6 cycles	tERR(6per), allowed	MIN	-155	-133	-111	pS
		MAX	155	133	111	
Cumulative error across 7 cycles	tERR(7per), allowed	MIN	-163	-139	-116	pS
		MAX	163	139	116	
Cumulative error across 8 cycles	tERR(8per), allowed	MIN	-169	-145	-121	pS
		MAX	169	145	121	
Cumulative error across 9 cycles	tERR(9per), allowed	MIN	-175	-150	-125	pS
		MAX	175	150	125	
Cumulative error across 10 cycles	tERR(10per), allowed	MIN	-180	-154	-128	pS
		MAX	180	154	128	
Cumulative error across 11 cycles	tERR(11per), allowed	MIN	-184	-158	-132	pS
		MAX	184	158	132	
Cumulative error across 12 cycles	tERR(12per), allowed	MIN	-188	-161	-134	pS
		MAX	188	161	134	
Cumulative error across n = 13, 14, 15..., 19, 20 cycles	tERR(nper), allowed	MIN	tERR(nper),allowed MIN = (1 + 0.68ln(n)) x tJIT(per),allowed MIN			pS
		MAX	tERR(nper),allowed,max = (1 + 0.68ln(n)) x tJIT(per),allowed MAX			

ZQ Calibration Parameters						
Initialization calibration time	tzQINIT	MIN	1			μS
Long calibration time	tzQCL	MIN	360			nS
Short calibration time	tzQCS	MIN	90			nS
Calibration Reset time	tzQRESET	MIN	max(50nS,3nCK)			nS
Read Parameters ⁴						
DQS output access time from CK_t/CK_c	tdQSCK	MIN	2500			pS
		MAX	5500			
DQSCK delta short ⁵	tdQSCKDS	MAX	220	190	165	pS
DQSCK delta medium ⁵	tdQSCKDM	MAX	511	435	380	pS
DQSCK delta long ⁷	tdQSCKDL	MAX	614	525	460	pS
DQS-DQ skew	tdQSQ	MAX	135	115	100	pS
DQS output High pulse width	tQSH	MIN	tCH(abs) - 0.05			tCK(avg)
DQS output Low pulse width	tQSL	MIN	tCL(abs) - 0.05			tCK(avg)
DQ/DQS output hold time from DQS	tQH	MIN	min(tQSH, tQSL)			tCK(avg)
Read preamble ^{8,10}	tRPRE	MIN	0.9			tCK(avg)
Read postamble ^{8,11}	tRPST	MIN	0.3			tCK(avg)
DQS Low-Z from clock ⁸	tLZ(DQS)	MIN	tdQSCK(MIN) - 300			pS
DQ Low-Z from clock ⁸	tLZ(DQ)	MIN	tdQSCK(MIN) - 300			pS
DQS High-Z from clock ⁸	tHZ(DQS)	MAX	tdQSCK(MAX) - 100			pS
DQ High-Z from clock ⁸	tHZ(DQ)	MAX	tdQSCK(MAX) + (1.4 x tdQSQ(MAX))			pS
Write Parameters ⁴						
DQ and DM input hold time (VREF based)	tDH	MIN	150	130	115	pS
DQ and DM input setup time (VREF based)	tDS	MIN	150	130	115	pS
DQ and DM input pulse width	tDIPW	MIN	0.35			tCK(avg)
Write command to 1st DQS latching transition	tdQSS	MIN	0.75			tCK(avg)
		MAX	1.25			
DQS input high-level width	tdQSH	MIN	0.4			tCK(avg)
DQS input low-level width	tdQSL	MIN	0.4			tCK(avg)
DQS falling edge to CK setup time	tDSS	MIN	0.2			tCK(avg)
DQS falling edge hold time from CK	tDSh	MIN	0.2			tCK(avg)
Write postamble	tWPST	MIN	0.4			tCK(avg)
Write preamble	tWPRE	MIN	0.8			tCK(avg)
CKE Input Parameters						
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	MIN	max(7.5nS,3nCK)			nS
CKE input setup time	tISCKE ¹²	MIN	0.25			tCK(avg)
CKE input hold time	tIHCKE ¹³	MIN	0.25			tCK(avg)
Command path disable delay	tCPDED	MIN	2			tCK(avg)
Command Address Input Parameters ⁴						
Address and control input setup time	tISCA ¹⁴	MIN	150	130	115	pS
Address and control input hold time	tIHCA ¹⁴	MIN	150	130	115	pS
CS_n input setup time	tISCS ¹⁴	MIN	270	230	205	pS
CS_n input hold time	tIHCS ¹⁴	MIN	270	230	205	pS
Address and control input pulse width	tIPWCA	MIN	0.35			tCK(avg)
CS_n input pulse width	tIPWCS	MIN	0.7			tCK(avg)
Boot Parameters (10 MHz–55 MHz) ^{15, 16, 17}						
Clock Cycle Time	tCKb	MAX	100			nS
		MIN	18			
CKE Input setup time	tISCKEb	MIN	2.5			nS
CKE Input hold time	tIHCKEb	MIN	2.5			nS
Address and control input setup time	tISb	MIN	1150			pS

Address and control input hold time	tIHb	MIN	1150			pS
DQS output data access time from CK_t/CK_c	tDQSKb	MIN	2.0			nS
		MAX	10.0			
Data strobe edge to output data edge	tDQSqb	MAX	1.2			nS
Mode Register Parameters						
Mode Register Write command period	tMRW	MIN	10			tCK(avg)
Mode Register Read command period	tMRR	MIN	4			tCK(avg)
Additional time after tXP has expired until MRR command may be issued	tMRRi	MIN	tRCD(MIN)			nS
Core Parameters¹⁸						
Read Latency	RL	MIN	12	14	16	tCK(avg)
Write Latency (set A)	WL	MIN	6	8	8	tCK(avg)
Activate to Activate command period	tRC	MIN	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)			nS
CKE minimum pulse width during Self Refresh (low pulse width during Self Refresh)	tCKESR	MIN	max(15nS, 3nCK)			nS
Self Refresh exit to next valid command delay	tXSR	MIN	max(tRFCab + 10nS, 2nCK)			nS
Exit power-down to next valid command delay	tXP	MIN	max(7.5nS, 3nCK)			nS
CAS-to-CAS delay	tCCD	MIN	4			tCK(avg)
Internal Read to Precharge command delay	tRTP	MIN	max(7.5nS, 4nCK)			nS
RAS to CAS Delay	tRCD (typ)	MIN	max(18nS, 3nCK)			nS
Row precharge time (single bank)	tRPpb (typ)	MIN	max(18nS, 3nCK)			nS
Row precharge time (all banks)	tRPab (typ)	MIN	max(21nS, 3nCK)			nS
Row active time	tRAS	MIN	max(42nS, 3nCK)			nS
		MAX	min(70.2, 9 x RM x tREFI)			μS
Write Recovery Time	tWR	MIN	max(15nS, 4nCK)			nS
Internal Write-to-Read command delay	tWTR	MIN	max(7.5nS, 4nCK)			nS
Active bank A to active bank B	tRRD	MIN	max(10nS, 2nCK)			nS
Four-bank Activate Window	tFAW	MIN	max(50nS, 8nCK)			nS
Minimum deep power-down time	tDPD	MIN	500			μS
ODT Parameters						
Asynchronous RTT turn-on delay from ODT input	tODTon	MIN	1.75			nS
		MAX	3.5			
Asynchronous RTT turn-off delay from ODT input	tODToff	MIN	1.75			nS
		MAX	3.5			
Automatic RTT turn-on delay after Read data	tAODTon	MAX	tDQSK + 1.4 × tDQSQ,max + tCK(avg,min)			pS
Automatic RTT turn-off delay after Read data	tAODToff	MIN	tDQSK,min - 300			pS
RTT disable delay from power down entry	tODTd	MAX	12			nS
RTT disable delay from self-refresh, and deep power down entry	tODTd	MAX	12 + 0.5 tck			nS
RTT enable delay from power down and self refresh exit	tODTe	MAX	12			nS
CA Training Parameters						
First CA calibration command after CA calibration mode is programmed	tCAMRD	MIN	20			tCK(avg)
First CA calibration command after CKE is LOW	tCAENT	MIN	10			tCK(avg)
CA calibration exit command after CKE is HIGH	tCAEXT	MIN	10			tCK(avg)
CKE LOW after CA calibration mode is programmed	tCACKEL	MIN	10			tCK(avg)
CKE HIGH after the last CA calibration results are driven	tCACKEH	MIN	10			tCK(avg)
Data out delay after CA training calibration command is programmed	tADR	MAX	20			nS
MRW CA exit command to DQ tri-state	tMRZ	MIN	3			nS
CA calibration command to CA calibration command delay	tCACD	MIN	RU(tADR+2 × tck)			tCK(avg)

Write Leveling Parameters						
DQS_t/DQS_c delay after write leveling mode is programmed	twLDQSEN	MIN	25			nS
		MAX	-			
First DQS_t/DQS_c edge after write leveling mode is programmed	twLMRD	MIN	40			nS
		MAX	-			
Write leveling output delay	twLO	MIN	0			nS
		MAX	20			
Write leveling hold time	twLH	MIN	175	150	135	pS
Write leveling setup time	twLS	MIN	175	150	135	pS
Mode register set command delay	tMRD	MIN	max(14nS, 10nCK)			nS
		MAX	-			
Temperature Derating ¹⁷						
DQS output access time from CK_t/CK_c (derated)	tDQSC	MAX	5620			pS
RAS-to-CAS delay (derated)	tRCD	MIN	tRCD + 1.875			nS
Activate -to- Activate command period (derated)	tRC	MIN	tRC + 1.875			nS
Row active time (derated)	tRAS	MIN	tRAS + 1.875			nS
Row precharge time (derated)	tRP	MIN	tRP + 1.875			nS
Active bank A to active bank B (derated)	tRRD	MIN	tRRD + 1.875			nS

Note 1: Frequency values are for reference only. Clock cycle time (Tck) is used to determine device capabilities.

Note 2: All AC timings assume an input slew rate of 2 V/ns.

Note 3: Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal VIX

Note 4: READ, WRITE, and input setup and hold values are referenced to VREF.

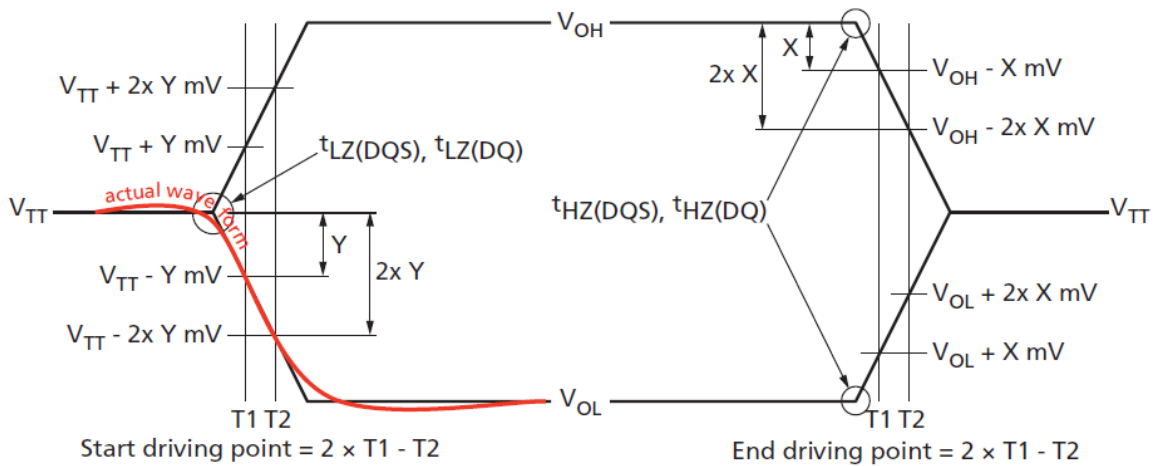
Note 5: tDQCKDS is the absolute value of the difference between any two tDQCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQCKDS is not tested and is guaranteed by design. Temperature drift in the system is <math><10^{\circ}\text{C/s}</math>. Values do not include clock jitter.

Note 6: tDQCKDM is the absolute value of the difference between any two tDQCK measurements (in a byte lane) within a 1.6 μs rolling window. tDQCKDM is not tested and is guaranteed by design. Temperature drift in the system is <math><10^{\circ}\text{C/s}</math>. Values do not include clock jitter.

Note 7: tDQCKDL is the absolute value of the difference between any two tDQCK measurements (in a byte lane) within a 32ms rolling window. tDQCKDL is not tested and is guaranteed by design. Temperature drift in the system is <math><10^{\circ}\text{C/s}</math>. Values do not include clock jitter.

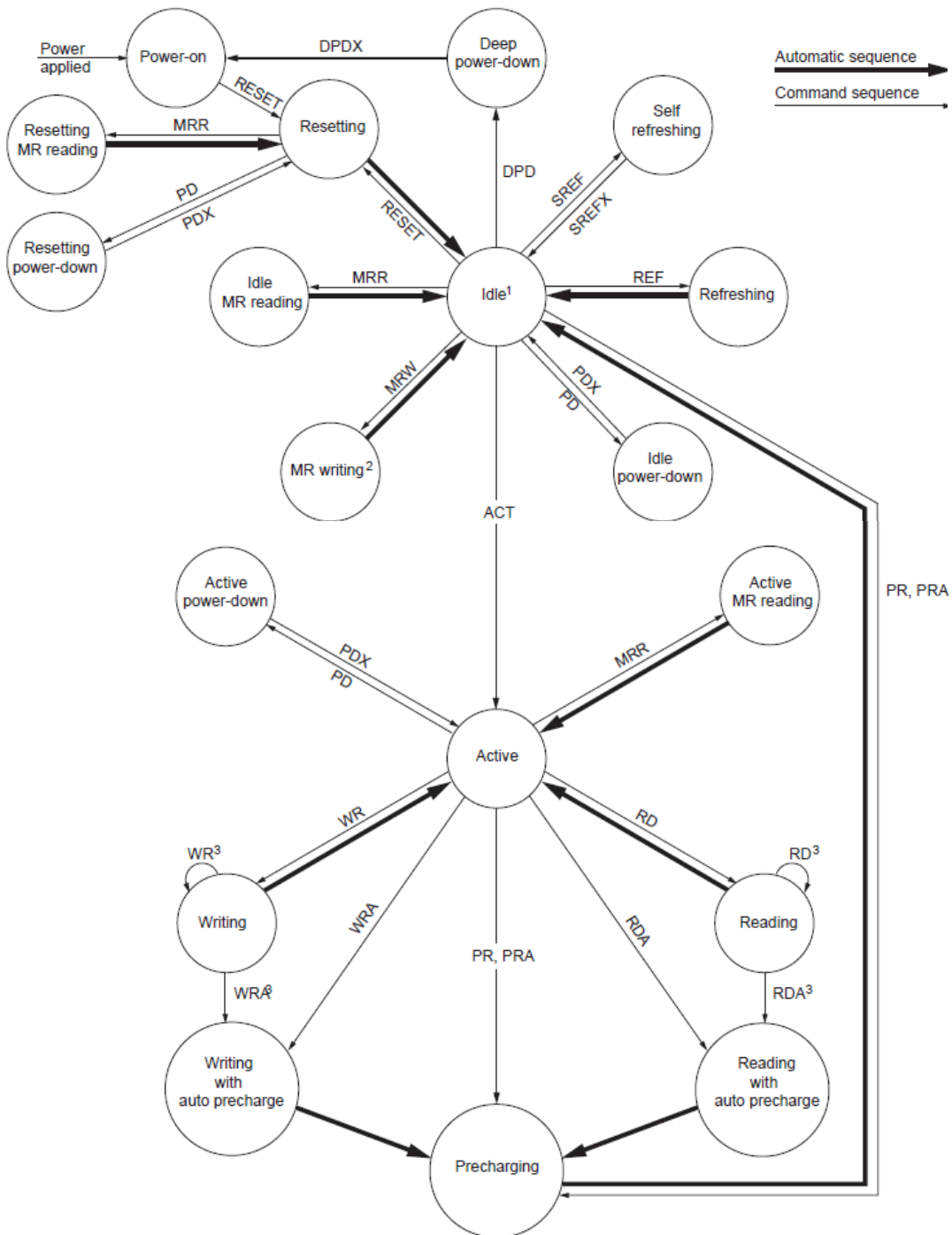
Note 8: For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS) and tLZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ) or begins driving tLZ(DQS) and tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS.

Output Transition Timing



- Note 9:** Measured from the point when DQS begins driving the signal, to the point when DQS begins driving the first rising strobe edge.
- Note 10:** Measured from the last falling strobe edge of DQS to the point when DQS finishes driving the signal.
- Note 11:** CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK crossing.
- Note 12:** CKE input hold time is measured from CK crossing to CKE reaching a HIGH/LOW voltage level.
- Note 13:** Input setup/hold time for signal (CA[9:0], /CS).
- Note 14:** To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
- Note 15:** Mobile LPDDR3 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
- Note 16:** The output skew parameters are measured with default output impedance settings using the reference load.
- Note 17:** The minimum tCK column applies only when tCK is greater than 6ns.

Simplified State Diagram



Command Truth Table

SDRAM Command	SDR Command Pins		DDR CA Pins (10)												CK_t EDGE
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9		
	CK_t(n-1)	CK_t(n)		MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7		
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↕	
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↘	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↕	
			X	MA6	MA7	X									
Refresh (per bank)	H	H	L	L	L	H	L	X						↕	
			X	X											↘
Refresh (all bank)	H	H	L	L	L	H	H	X						↕	
			X	X											↘
Enter Self Refresh	H	L	L	L	L	H	X						↕		
	X		X											↘	
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↕	
			X	R0	R1	R2	R3	R4	R5	R6	R7	X	X	↘	
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↕	
			X	AP ⁴³	C3	C4	C5	C6	C7	C8	C9	X	X	↘	
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↕	
			X	AP ⁴³	C3	C4	C5	C6	C7	C8	C9	X	X	↘	
Precharge ¹¹ (per bank, all bank)	H	H	L	H	H	L	H	AB ¹¹	X	X	BA0	BA1	BA2	↕	
			X	X	X	X	X	X	X	X	X	X	X	↘	
Enter Deep Power Down	H	L	L	H	H	L	X						↕		
	X		X											↘	
NOP	H	H	L	H	H	H	X						↕		
			X	X											↘
Maintain PD, SREF, DPD (NOP) See note 4	L	L	L	H	H	H	X						↕		
			X	X											↘
NOP	H	H	H	X											↕
			X	X											↘
Maintain PD, SREF, DPD See note 4	L	L	X	X											↕
			X	X											↘
Enter Power Down	H	L	H	X											↕
	X		X											↘	
Exit PD, SREF,DPD	L	H	H	X											↕
	X		X											↘	

- Note 1:** All commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
- Note 2:** Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
- Note 3:** AP “high” during a Read or Write command indicates that an auto-precharge will occur to the bank associated with the Read or Write command.
- Note 4:** “X” means “H or L (but a defined logic level)”, except when the LPDDR3 SDRAM is in PD, SREF, or DPD, in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure.
- Note 5:** Self refresh exit and Deep Power Down exit are asynchronous.
- Note 6:** VREF must be between 0 and VDDQ during Self Refresh and Deep Down operation.
- Note 7:** CAx_r refers to command/address bit “x” on the rising edge of clock.
- Note 8:** CAx_f refers to command/address bit “x” on the falling edge of clock.

Note 9: CS_n and CKE are sampled at the rising edge of clock.

Note 10: The least significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.

Note 11: AB HIGH during a PRECHARGE command indicates that an all-bank precharge will occur. In this case, bank address is a "Don't Care."

Note 12: When CS_n is HIGH, LPDDR3 CA bus can be floated.

CKE Truth Table

Item	Command(n)	Operation	/CS	CKE		Notes
				n-1	n	
Active Power Down	X	Maintain Active Power Down	X	L	L	
	NOP	Exit Active Power Down	H	L	H	6,7
Idle Power Down	X	Maintain Idle Power Down	X	L	L	
	NOP	Exit Idle Power Down	H	L	H	6,7
Resetting Power Down	X	Maintain Resetting Power Down	X	L	L	
	NOP	Exit Resetting Power Down	H	L	H	6,7,8
Deep Power Down	X	Maintain Deep Power Down	X	L	L	
	NOP	Exit Deep Power Down	H	L	H	9
Self Refresh	X	Maintain Self Refresh	X	L	L	
	NOP	Exit Self Refresh	H	L	H	10,11
Bank(s) Active	NOP	Enter Active Power Down	H	H	L	
All Banks Idle	NOP	Enter Idle Power Down	H	H	L	12
	Enter Self-Refresh	Enter Self Refresh	L	H	L	12
	DPD	Enter Deep Power Down	L	H	L	12
Resetting	NOP	Enter Resetting Power Down	H	H	L	
Other states	Refer to the Command Truth Table			H	H	

Note 1: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note 2: 'X' means 'Don't care'.

Note 3: "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.

Note 4: "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.

Note 5: "CS_n" is the logic state of CS_n at the clock rising edge n;

Note 6: "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".

Note 7: Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XP} period.

Note 8: Self-Refresh exit time (t_{XS}) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the t_{XS} time.

Note 9: The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.

Note 10: Upon exiting Resetting Power Down, the device will return to the idle state if t_{INIT5} has expired.

Note 11: In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

Current State Bank n – Command to Bank n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (AllBank)	7
	MRW	Load value from Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle / MR Reading	
	Reset	Begin Device Auto-initialization	Resetting	7,8
Row Active	Precharge	Deactivate row in bank or banks	Precharging	9,10
	Read	Select column, Read and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
Reading	Precharge	Deactivate row in bank or banks	Precharging	9
	Read	Select column, and start new read burst	Reading	11,12
Writing	Write	Select column, and start write burst	Writing	11,12, 13
	Read	Select column, and start new read burst	Reading	11,12, 14
Power On	MRW Reset	Begin Device Auto-initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note 1: Values in this table apply when both CKEn -1 and CKEn are HIGH, and after tXSR or tXP has been met, if the previous state was power-down.

Note 2: All states and sequences not shown are illegal or reserved.

Note 3: Current state definitions:

State	Definition
Idle	The bank or banks have been precharged, and tRP has been met.
Active	A row in the bank has been activated, and tRCD has been met. No data bursts or accesses, and no register accesses, are in progress.
Reading	A READ burst has been initiated with auto precharge disabled, and has not yet terminated.
Writing	A WRITE burst has been initiated with auto precharge disabled, and has not yet terminated.

Note 4: The states listed below must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in the table: Current State Bank n to Command to Bank m..

State	Starts With...	Ends When..	Notes
Precharging	Registration of a PRECHARGE command	tRP is met	After tRP is met, the bank is in the idle state.

State	Starts With...	Ends When..	Notes
Row activating	Registration of an ACTIVATE command	tRCD is met	After tRCD is met, the bank is in the active state.
READ with AP enabled	Registration of a READ command with auto precharge enabled	tRP is met	After tRP is met, the bank is in the idle state.
WRITE with AP enabled	Registration of a WRITE command with auto precharge enabled	tRP is met	After tRP is met, the bank is in the idle state.

Note 5: The states listed below must not be interrupted by any executable command. NOP commands must be applied to each positive clock edge during these states.

State	Starts With...	Ends When..	Notes
Refreshing (per bank)	Registration of a REFRESH (per bank) command	tRFCpb is met	After tRFCpb is met, the bank is in the idle state.
Refreshing (all banks)	Registration of a REFRESH (all banks) command	tRFCab is met	After tRFCab is met, the device is in the all banks idle state.
Idle MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks idle state.
Resetting MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks idle state.
Active MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	tMRW is met	After tMRW is met, the device is in the all banks idle state.
Precharging all	Registration of a PRECHARGE ALL command	tRP is met	After tRP is met, the device is in the all banks idle state.

Note 6: Bank-specific; requires that the bank is idle and no bursts are in progress.

Note 7: Not bank-specific; requires that all banks are idle and no bursts are in progress.

Note 8: Not bank-specific. reset command is achieved through Mode Register Write command.

Note 9: This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.

Note 10: If a PRECHARGE command is issued to a bank in the idle state, tRP still applies.

Note 11: A command other than NOP should not be issued to the same bank while a READ or WRITE with auto precharge is enabled.

Note 12: The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.

Note 13: A WRITE command can be issued only after the completion of the READ burst.

Note 14: A READ command can be issued only after completion of the WRITE burst.

Current State Bank n – Command to Bank m

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10, 11
Reading (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,12
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	7,13
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	7,14
	Write	Select column, and start write burst to Bank m	Writing	7,12, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	7,13, 14
	Write	Select column, and start write burst to Bank m	Writing	7,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Power On	Reset	Begin Device Auto-initialization	Resetting	15,16
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note 1: This table applies when:

- The previous state was self refresh or power-down;
- After tXSR or tXP has been met; and when both CKEn -1 and CKEn are HIGH.

Note 2: All states and sequences not shown are illegal or reserved..

Note 3: Current state definitions:.

State	Condition	And...	And...
Idle	The bank has been precharged	tRP is met	
Active	A row in the bank has been activated	tRCD is met	No data bursts/accesses and no register accesses are in progress.
Reading	A READ burst has been initiated with auto precharge disabled	The READ has not yet terminated	
Writing	A WRITE burst has been initiated with auto precharge disabled	The WRITE has not yet terminated	

Note 4: Refresh, self refresh, and MRW commands can only be issued when all banks are idle.

Note 5: The states listed below must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:

State	Starts With...	Ends When..	Notes
Idle MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks idle state.
Resetting MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks reset state.
Active MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	tMRW is met	After tMRW is met, the device is in the all banks idle state.

Note 6: tRRD must be met between the ACTIVATE command to bank n and any subsequent ACTIVATE command to bank m.

Note 7: READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.

Note 8: This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.

Note 9: MRR is supported in the row-activating state.

Note 10: MRR is supported in the precharging state.

Note 11: The next state for bank m depends on the current state of bank m (idle, row-activating, precharging, or active).

Note 12: A WRITE command can be issued only after the completion of the READ burst.

Note 13: A READ command can be issued only after the completion of the WRITE burst.

Note 14: A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks, provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.

Note 15: Not bank-specific; requires that all banks are idle and no bursts are in progress.

Note 16: RESET command is achieved through the MODE REGISTER WRITE command.

IDD Measurement Conditions

Switching for CA Input Signals

	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)
Cycle	N		N+1		N+2		N+3	
/CS	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes 1: CS_n must always be driven HIGH.

Notes 2: For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.

Notes 3: The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Switching for IDD4R

Clock	CKE	CS _n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	LLL	LLLLLLL	L
Rising	H	H	N+2	NOP	LLL	LLLLLLL	H
Falling	H	H	N+2	NOP	LLL	LLLLLLL	H
Rising	H	H	N+3	NOP	LLL	LLLLLLL	H
Falling	H	H	N+3	NOP	HLH	HLHLLHL	L
Rising	H	L	N+4	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N+4	Read_Falling	LHH	HHHHHHH	H
Rising	H	H	N+5	NOP	HHH	HHHHHHH	H
Falling	H	H	N+5	NOP	HHH	HHHHHHH	L
Rising	H	H	N+6	NOP	HHH	HHHHHHH	L
Falling	H	H	N+6	NOP	HHH	HHHHHHH	L
Rising	H	H	N+7	NOP	HHH	HHHHHHH	H
Falling	H	H	N+7	NOP	HLH	LHLHLHL	L

Notes 1: Data strobe (DQS_t) is changing between HIGH and LOW with every clock cycle.

Notes 2: The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

Switching for IDD4W

Clock	CKE	CS _n	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	LLL	LLLLLLL	L
Rising	H	H	N+2	NOP	LLL	LLLLLLL	H
Falling	H	H	N+2	NOP	LLL	LLLLLLL	H
Rising	H	H	N+3	NOP	LLL	LLLLLLL	H
Falling	H	H	N+3	NOP	HLL	HLHLLHL	L
Rising	H	L	N+4	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N+4	Write_Falling	LHH	HHHHHHH	H
Rising	H	H	N+5	NOP	HHH	HHHHHHH	H
Falling	H	H	N+5	NOP	HHH	HHHHHHH	L
Rising	H	H	N+6	NOP	HHH	HHHHHHH	L
Falling	H	H	N+6	NOP	HHH	HHHHHHH	L
Rising	H	H	N+7	NOP	HHH	HHHHHHH	H
Falling	H	H	N+7	NOP	HLL	LHLHLHL	L

Notes 1: Data strobe (DQS_t) is changing between HIGH and LOW with every clock cycle.

Notes 2: Data masking (DM) must always be driven LOW.

Notes 3: The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4W

Burst Sequence

Burst Length	C2	C1	C0	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
8	0b	0b	0b	0	1	2	3	4	5	6	7
	0b	1b	0b	2	3	4	5	6	7	0	1
	1b	0b	0b	4	5	6	7	0	1	2	3
	1b	1b	0b	6	7	0	1	2	3	4	5

Notes 1: C0 input is not present on CA bus. It is implied zero.

Notes 2: The burst address represents C2 – C0.

Power-up, Initialization, and Power-Off

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure are mandatory.

Power Ramp

While applying power (after T_a), CKE must be held LOW ($\leq 0.2 \times VDDCA$) and all other inputs must be between V_{ILmin} and V_{IHmax} . The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (T_b), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSS and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Table below..

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2 - 200mV
	VDD1 and VDD2 must be greater than VDDCA - 200mV
	VDD1 and VDD2 must be greater than VDDQ - 200mV
	VREF must always be less than all other supply voltages

Notes 1: T_a is the point when any power supply first reaches 300mV.

Notes 2: Noted conditions apply between T_a and power-down (controlled or uncontrolled).

Notes 3: T_b is the point at which all supply and reference voltages are within their defined operating ranges.

Notes 4: Power ramp duration t_{INIT0} ($T_b - T_a$) must not exceed 20 mS.

Notes 5: The voltage difference between of VSS pin must not exceed 100 mV.

Beginning at T_b , CKE must remain LOW for at least t_{INIT1} , after which CKE can be asserted HIGH. The clock must be stable at least t_{INIT2} prior to the first CKE LOW-to-HIGH transition (T_c). CKE, CS_n, and CA inputs must observe setup and hold requirements (t_{IS} , t_{IH}) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRR commands are issued, the clock period must be within the range defined for t_{CKb} . MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least t_{INIT3} (T_d). The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{ZQINIT} .

Reset command

After t_{INIT3} is satisfied, a MRW(Reset) command must be issued (T_d). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during t_{INIT4} .

Mode Registers Reads and Device Auto-Initialization (DAI) polling

After t_{INIT4} is satisfied (T_e), only MRR commands and POWER-DOWN ENTRY/EXIT commands are supported, and CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down). MRR commands are valid at this time only when the CA bus does not need to be trained. CA training can begin only after time T_f . The MRR command can be initiated to poll the DAI bit, which indicates whether device auto initialization is complete. When the bit indicates completion, the device is in an idle state. The device is also in an idle state after t_{INIT5} (MAX) has expired, regardless whether the DAI bit has been read by the MRR command. Because the memory output buffers are not properly configured by T_e , some AC parameters must use relaxed timing specifications before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (T_f). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than t_{INIT5} after the RESET command. The controller must wait at least t_{INIT5} (MAX) or until the DAI bit is set before proceeding.

ZQ Calibration

If CA training is not required, the MRW INITIALIZATION CALIBRATION (ZQ_CAL) command can be issued to the memory (MR10) after T_f . No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA training. After the completion of CA training (T_f'), the MRW INITIALIZATION CALIBRATION (ZQ_CAL) command can be issued to the memory. This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after t_{ZQINIT} .

Normal Operation

After t_{ZQINIT} (T_g), MRW commands must be used to properly configure the memory (for example, output buffer drive strength, latencies, and so on). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration. After the initialization sequence is complete, the device is ready for any valid command. After T_g , the clock frequency can be changed using the procedure described in the Input Clock Frequency Changes and Clock Stop Events section.

Mode Register Definition

For LPDDR3, a set of mode registers is used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment and Definition

The table listed below shows the mode registers for LPDDR3 SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Mode Register Assignments

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00H	Device Info.	R	RL3	WL (Set B)	(RFU)	RZQI		(RFU)		DAI
1	01H	Device Feature 1	W	nWR (for AP)			(RFU)	BL			
2	02H	Device Feature 2	W	WR Lev	WL Select	(RFU)	nWRE	RL & WL			
3	03H	I/O Config-1	W	(RFU)				DS			
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05H	Basic Config-1	R	Manufacturer ID							
6	06H	Basic Config-2	R	Revision ID1							
7	07H	Basic Config-3	R	Revision ID2							
8	08H	Basic Config-4	R	I/O width		Density				Type	
9	09H	(Reserved)	W	(RFU)							
10	0AH	I/O Calibration	W	Calibration Code							
11	0BH	ODT Feature	-	(RFU)					PD CTL	DQ ODT	
12:15	0CH~0FH	(Reserved)	-	(RFU)							
16	10H	PASR_Bank	W	PASR Bank Mask							
17	11H	PASR_Seg	W	PASR Segment Mask							
18-31	12H~1FH	(Reserved)	-	(RFU)							
32	20H	DQ Calibration Pattern A	R	DQ Calibration Pattern A							
33:39	21H~27H	(Do Not Use)	-								
40	28H	DQ Calibration Pattern B	R	DQ Calibration Pattern B							
41	29H	CA Training 1	W	CA Training 1							
42	2AH	CA Training 2	W	CA Training 2							
43:47	2BH~2FH	(Do Not Use)	-								
48	30H	CA Training 3	W	CA Training 3							
49:62	31H~3EH	(Reserved)	-	(RFU)							
63	3FH	Reset	W	X							
64:255	40H~FFH	(Reserved)	-	(RFU)							

Notes 1: RFU bits must be set to “0” during Mode Register writes.

Notes 2: RFU bits must be read as “0” during Mode Register reads.

Notes 3: All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.

Notes 4: All mode registers that are specified as RFU shall not be written.

Notes 5: Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA[7:0] = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI		(RFU)		DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0_b : DAI complete 1_b : DAI still in progress	
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	00_b : RZQ self test not executed. 01_b : ZQ-pin may connect to VDDCA or float 10_b : ZQ-pin may short to GND 11_b : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)	1-4
WL (Set B) Support	Read-only	OP[6]	0_b : DRAM does not support WL (Set B)	
RL3 Option Support	Read-only	OP[7]	0_b : DRAM does not support RL=3, nWR=3, WL=1	

Notes 1: RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.

Notes 2: If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

Notes 3: In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

Notes 4: In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ±1%).

MR1_Device Feature 1 (MA[7:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)		BL		

BL	Write-only	OP[2:0]	011_b : BL8 (default) All others : Reserved	
nWR	Write-only	OP[7:5]	If nWRE (MR2 OP<4>) = 0 001_b : nWR=3 100_b : nWR=6 110_b : nWR=8 111_b : nWR=9 If nWRE (MR2 OP<4>) = 1 000_b : nWR=10 (default) 001_b : nWR=11 010_b : nWR=12 100_b : nWR=14 110_b : nWR=16 All others : Reserved	1

Notes 1: Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

MR2_Device Feature 2 (MA[7:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	nWRE	RL & WL			
RL & WL	Write-only	OP[3:0]	OP<6>=0 (WL Set A, default) 0001_b : (Reserved) 0100_b : RL = 6 / WL = 3 (≤400 MHz) 0110_b : RL = 8 / WL = 4 (≤533 MHz) 0111_b : RL = 9 / WL = 5 (≤600 MHz) 1000_b : RL = 10 / WL = 6 (≤667 MHz, default) 1001_b : RL = 11 / WL = 6 (≤733 MHz) 1010_b : RL = 12 / WL = 6 (≤800 MHz) 1100_b : RL = 14 / WL = 8 (≤933 MHz) 1110_b : RL = 16 / WL = 8 (≤1066 MHz) All others : Reserved				
nWRE	Write-only	OP[4]	0_b : enable nWR programming ≤ 9 1_b : enable nWR programming > 9 (default)				
WL Select	Write-only	OP[6]	0_b : Select WL Set A (default) 1_b : (Reserved)				
WR Leveling	Write-only	OP[7]	0_b : Disable (default) 1_b : Enable				

MR3_I/O Configuration 1 (MA[7:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			
DS	Write-only	OP[3:0]	0001_b : 34.3Ω typical pull-down/pull-up 0010_b : 40Ω typical pull-down/pull-up (default) 0011_b : 48Ω typical pull-down/pull-up 0100_b : 60Ω typical pull-down/pull-up 0110_b : 80Ω typical pull-down/pull-up 1001_b : 34.3Ω typical pull-down, 40Ω typical pull-up 1010_b : 40Ω typical pull-down, 48Ω typical pull-up 1011_b : 34.3Ω typical pull-down, 48Ω typical pull-up All others : Reserved				

MR4_Device Temperature (MA[7:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		
SDRAM Refresh Rate, Refresh Multiplier (RM)	Read-only	OP[2:0]	000_b : SDRAM Low temperature operating limit exceeded 001_b : RM = 4; tREFIM = 4 x tREFI, tREFIMpb = 4 x tREFIpb, tREFWM = 4 x tREFW 010_b : RM = 2; tREFIM = 2 x tREFI, tREFIMpb = 2 x tREFIpb, tREFWM = 2 x tREFW 011_b : RM = 1; tREFIM = tREFI, tREFIMpb = tREFIpb, tREFWM = tREFW (≤ 85°C) 100_b : RM = 0.5; tREFIM = 0.5 x tREFI, tREFIMpb = 0.5 x tREFIpb, tREFWM = 0.5 x tREFW, do not de-rate SDRAM AC timing 101_b : RM = 0.25; tREFIM = 0.25 x tREFI, tREFIMpb = 0.25 x tREFIpb, tREFWM = 0.25 x tREFW, do not de-rate SDRAM AC timing 110_b : RM = 0.25; tREFIM = 0.25 x tREFI, tREFIMpb = 0.25 x tREFIpb, tREFWM = 0.25 x tREFW, de-rate SDRAM AC timing 111_b : SDRAM High temperature operating limit exceeded				
Temperature Update Flag (TUF)	Read-only	OP7	0_b : OP[2:0] value has not changed since last read of MR4 1_b : OP[2:0] value has changed since last read of MR4				

Notes 1: A Mode Register Read from MR4 will reset OP7 to '0'.

Notes 2: OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.

Notes 3: If OP2 equals '1', the device temperature is greater than 85°C.

Notes 4: OP7 is set to '1' if OP[2:0] has changed at any time since the last read of MR4.

Notes 5: SDRAM might not operate properly when OP[2:0] = 000b or 111b.

MR5_Basic Configuration 1 (MA[7:0] = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR3 Manufacturer ID							
LPDDR3 Manufacturer ID		Read-only		OP[7:0]		0000 1000b:	

MR8_Basic Configuration 4 (MA[7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	
Type	Read-only		OP[1:0]		11 _b : LPDDR3 SDRAM All others: Reserved		
Density	Read-only		OP[5:2]		0100 _b : 1Gb All others: Reserved		
I/O width	Read-only		OP[7:6]		00 _b : x32 01 _b : x16 All others: Reserved		

MR10_Calibration (MA[7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							
Calibration Code		Write-only		OP[7:0]		0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset All others: Reserved	

Notes 1: Host processor shall not write MR10 with “Reserved” values.

Notes 2: LPDDR3 devices shall ignore calibration command when a “Reserved” value is written into MR10.

Notes 3: See AC timing table for the calibration latency.

Notes 4: The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11_ODT Control (MA[7:0] = 0BH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					PD CTL		DQ ODT
DQ ODT	Write-only		OP[1:0]		00 _b : Disable (Default) 01 _b : RZQ /4 10 _b : RZQ /2 11 _b : RZQ /1		
PD Control	Write-only		OP[2]		0 _b : ODT disabled by DRAM during power down (default) 1 _b : ODT enabled by DRAM during power down		

MR16_PASR_Bank Mask (MA[7:0] = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							
Bank [7:0] Mask		Write-only	OP[7:0]		0_b : Refresh enable to the bank (= unmasked, default) 1_b : Refresh blocked (= masked)		
OP	Bank Mask			8-Bank SDRAM			
0	XXXXXXX1			Bank 0			
1	XXXXXX1X			Bank 1			
2	XXXXX1XX			Bank 2			
3	XXXX1XXX			Bank 3			
4	XXX1XXXX			Bank 4			
5	XX1XXXXX			Bank 5			
6	X1XXXXXX			Bank 6			
7	1XXXXXXX			Bank 7			

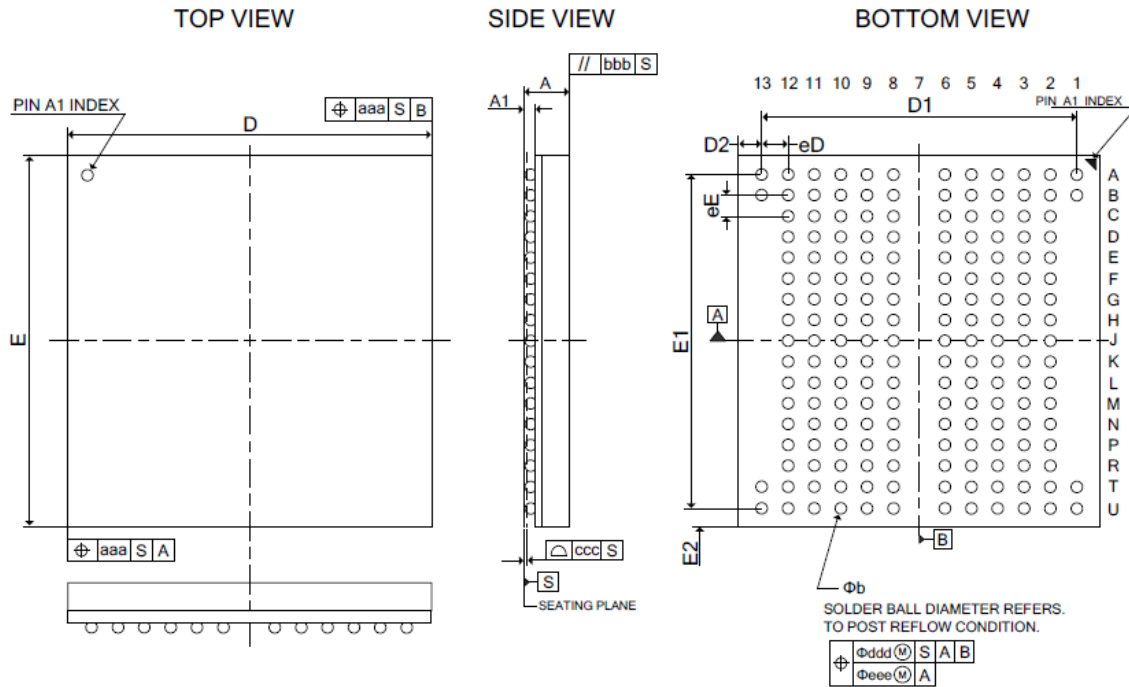
MR17_PASR_Segment Mask (MA[7:0] = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							
Segment [7:0] Mask		Write-only	OP[7:0]		0_b : Refresh enable to the bank (= unmasked, default) 1_b : Refresh blocked (= masked)		
Segment	OP	Segment Mask			R[12:10]		
0	0	XXXXXXX1			000b		
1	1	XXXXXX1X			001b		
2	2	XXXXX1XX			010b		
3	3	XXXX1XXX			011b		
4	4	XXX1XXXX			100b		
5	5	XX1XXXXX			101b		
6	6	X1XXXXXX			110b		
7	7	1XXXXXXX			111b		

Notes 1: This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

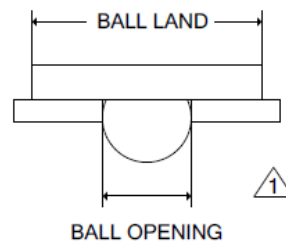
Package Description

178-ball FBGA



Controlling Dimension: Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.18	0.23	0.28	0.007	0.009	0.011
b	0.26	0.31	0.36	0.010	0.012	0.014
D	10.90	11.00	11.10	0.429	0.433	0.437
E	11.40	11.50	11.60	0.449	0.453	0.457
D1	9.60 BSC.			0.378 BSC.		
E1	10.40 BSC.			0.409 BSC.		
D2	0.70 BSC.			0.028 BSC.		
E2	0.55 BSC.			0.022 BSC.		
eD	0.80 BSC.			0.032 BSC.		
eE	0.65 BSC.			0.026 BSC.		
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.15	---	---	0.006
eee	---	---	0.05	---	---	0.002



Note:
 1. Ball land: 0.38mm, Ball opening: 0.28mm,
 PCB Ball land suggested \leq 0.38mm

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	June. 2023	Rico Yang	N/A
1.0	First SPEC. release.	July. 2023	Rico Yang	N/A