

256Mb (4Mx4Banksx16) Low Power DDR2 SDRAM

Descriptions

LPDDR2 is a high-speed SDRAM device internally configured as a 4-Bank memory. These devices contains 256Mb has 268,435,456 bits.

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

For LPDDR2 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

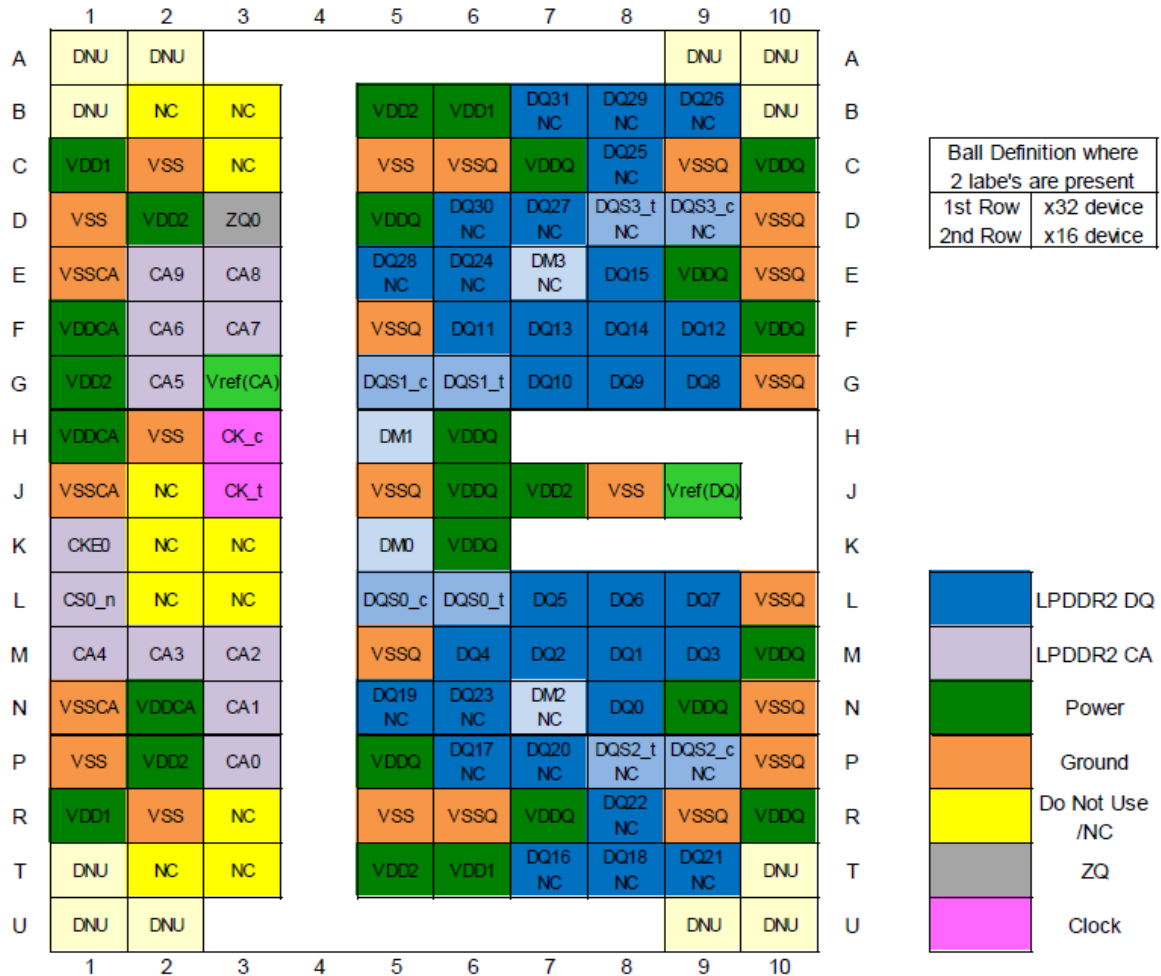
Features

- VDD1 = 1.7~1.95V
- VDD2/VDDCA/VDDQ = 1.14V~1.30V
- Data width: x16
- Clock rate: up to 533 MHz
- Data rate: up to 1066 Mbps
- Four-bit prefetch DDR architecture
- Four internal banks
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Auto refresh: All bank refresh mode only
- Partial Array Self-Refresh (PASR):
All bank or per bank, bank mask is supported but segment mask is not supported
- Precharge command: All bank or per bank
- Read/Write with auto-precharge
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Double data rate for data output
- Differential clock inputs
- Bidirectional differential data strobe
- Interface: HSUL_12
- JEDEC LPDDR2-S4B compliance
- Support package:
Single channel: VFBGA 134 ball (10mm x11.5mm)

Ordering Information

Part No	Organization	Max. Data Rate	Package	Grade
H2A725616B6BBSC	16M X 16	LPDDR2-800	134Ball	Commercial
H2A725616B6BCSC	16M X 16	LPDDR2-1066	BGA,10x11.5mm	Commercial

Pin Assignment



134-Ball FBGA

Pin Description (Simplified)

Name	Type	Description
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See 7.5.1 “ Command Truth Table ” for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. See 7.5.1 “ Command Truth Table ” for command code descriptions. CS_n is sampled at the positive Clock edge.
CA[9:0]	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code. See 7.5.1 “ Command Truth Table ” for command code descriptions.
DQ[n:0]	I/O	Data Inputs/Output: Bi-directional data bus. n=15 for 16 bits DQ; n=31 for 32 bits DQ.
DQSn_t, DQSn_c	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15; DQS2_t and DQS2_c to the data on DQ16-23; DQS3_t and DQS3_c to the data on DQ24-31.
DMn	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	Core Power Supply 1: Power supply for core.
VDD2	Supply	Core Power Supply 2: Power supply for core.
VDDCA	Supply	Input Receiver Power Supply: Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
VDDQ	Supply	I/O Power Supply: Power supply for Data input/output buffers.
VREF(CA)	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
VREF(DQ)	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
VSS	Supply	Ground
VSSCA	Supply	Ground for CA Input Receivers
VSSQ	Supply	I/O Ground
ZQ	I/O	Reference Pin for Output Drive Strength Calibration

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative	-0.4 ~ 1.6	V
V_{DD1}	Voltage on VDD1 pin relative	-0.4 ~ 2.3	V
V_{DD2}	Voltage on VDD2 pin relative	-0.4 ~ 1.6	V
V_{DDCA}	Voltage on VDDCA pin relative	-0.4 ~ 1.6	V
V_{DDQ}	Voltage on VDDQ pin relative	-0.4 ~ 1.6	V
T_{STG}	Storage Temperature (plastic)	-55 ~ 125	°C

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2: Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Note 3: $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$, provided that $V_{REFCA} \leq 300\text{mV}$.

Note 4: $V_{REFDQ} \leq 0.6 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$, provided that $V_{REFDQ} \leq 300\text{mV}$.

Capacitance

Symbol	Parameter	Min.	Max.	Units
C_{CK}	Input Capacitance (CK, /CK)	1	3	pF
C_{DCK}	Input capacitance delta, CK and /CK	0	0.2	pF
C_I	Input capacitance, all other input-only pins	1	3	pF
C_{DI}	Input capacitance delta, all other input-only pins	-0.5	0.5	pF
C_{IO}	Input/output capacitance, DQ, DM, DQS,/DQS	1.25	3.5	pF
C_{DDQS}	Input/output capacitance delta, DQS, /DQS	0	0.25	pF
C_{DIO}	Input/output capacitance delta, DQ, DM	-0.5	0.5	pF
C_{ZQ}	Input/output capacitance ZQ Pin	0	3.5	pF

Note 1: This parameter is not subject to production testing. It is verified by design and characterization.

Note 2: $CDI = CI - 0.5 * (CDQS_t + CDQS_c)$.

Note 3: $CDIO = CIO - 0.5 * (CDQS_t + CDQS_c)$ in byte lane.

Note 4: Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5 pF.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V
V_{DD2}	Core Supply voltage 2	1.14	1.20	1.30	V
V_{DDCA}	Input Supply Voltage (Command/Address)	1.14	1.20	1.30	V
V_{DDQ}	I/O Supply voltage (DQ)	1.14	1.20	1.30	V

Notes: 1. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1 MHz at the DRAM package ball.

Notes: 2. VDD1 uses significantly less power than VDD2.

DC Characteristics

(IDD Specifications; VDD2, VDDQ, VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V)

Parameter/Condition	Symbol	Power Supply	400 MHz	533 MHz	Unit	Notes
Operating one bank active-precharge current: tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD0 ₁	VDD1	4	4	mA	1
	IDD0 ₂	VDD2	22.5	22.5	mA	1
	IDD0 _{IN}	VDDCA VDDQ	5.5	5.5	mA	1, 2
Idle power-down standby current: tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2P ₁	VDD1	300	300	μA	1
	IDD2P ₂	VDD2	400	400	μA	1
	IDD2P _{IN}	VDDCA VDDQ	35	35	μA	1, 2
Idle power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS_n is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2PS ₁	VDD1	300	300	μA	1
	IDD2PS ₂	VDD2	400	400	μA	1
	IDD2PS _{IN}	VDDCA VDDQ	35	35	μA	1, 2
Idle non power-down standby current: tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2N ₁	VDD1	0.3	0.3	mA	1
	IDD2N ₂	VDD2	10	12	mA	1
	IDD2N _{IN}	VDDCA VDDQ	4.1	4.1	mA	1, 2
Idle non power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS_n is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2NS ₁	VDD1	0.3	0.3	mA	1
	IDD2NS ₂	VDD2	9	11	mA	1
	IDD2NS _{IN}	VDDCA VDDQ	4.1	4.1	mA	1, 2
Active power-down standby current: tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3P ₁	VDD1	500	500	μA	1
	IDD3P ₂	VDD2	500	500	μA	1
	IDD3P _{IN}	VDDCA VDDQ	35	35	μA	1, 2
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS_n is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3PS ₁	VDD1	500	500	μA	1
	IDD3PS ₂	VDD2	500	500	μA	1
	IDD3PS _{IN}	VDDCA VDDQ	35	35	μA	1, 2
Active non power-down standby current: tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; One bank/RB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3N ₁	VDD1	0.5	0.5	mA	1
	IDD3N ₂	VDD2	12.6	14	mA	1
	IDD3N _{IN}	VDDCA VDDQ	4.1	4.1	mA	1, 2
Active non power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS_n is HIGH; One bank/RB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3NS ₁	VDD1	0.5	0.5	mA	1
	IDD3NS ₂	VDD2	11	12.6	mA	1
	IDD3NS _{IN}	VDDCA VDDQ	4.1	4.1	mA	1, 2

DC Characteristics(Continued)

(IDD Specifications; VDD2, VDDQ, VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V)

Parameter/Condition	Symbol	Power Supply	400 MHz	533 MHz	Unit	Notes
Operating burst read current: tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank/RB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4R ₁	VDD1	1.2	1.2	mA	1
	IDD4R ₂	VDD2	150	160	mA	1
	IDD4R _{IN}	VDDCA	4.1	4.1	mA	1
Operating burst write current: tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank/RB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	IDD4W ₁	VDD1	1.2	1.2	mA	1
	IDD4W ₂	VDD2	175	175	mA	1
	IDD4W _{IN}	VDDCA VDDQ	19.1	19.1	mA	1, 2
All Bank Refresh Burst current: tCK = tCK(avg)min; CKE is HIGH between valid commands; TRC = TRFCabmin; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5 ₁	VDD1	14	14	mA	1
	IDD5 ₂	VDD2	40	40	mA	1
	IDD5 _{IN}	VDDCA VDDQ	4.1	4.1	mA	1, 2
All Bank Refresh Average current: tCK = tCK(avg)min; CKE is HIGH between valid commands; TRC = tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5AB ₁	VDD1	0.9	0.9	mA	1
	IDD5AB ₂	VDD2	12	12	mA	1
	IDD5AB _{IN}	VDDCA VDDQ	4.1	4.1	mA	1, 2
Deep Power-Down current: CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	IDD8 ₁	VDD1	10	10	μA	1
	IDD8 ₂	VDD2	10	10	μA	1
	IDD8 _{IN}	VDDCA VDDQ	35	35	μA	1, 2

Note 1: IDD values published are the maximum of the distribution of the arithmetic mean.

Note 2: Measured currents are the summation of VDDQ and VDDCA.

Note 3: IDD current specifications are tested after the device is properly initialized.

IDD6 Partial Array Self-refresh current; VDD2, VDDQ, VDDCA = 1.14~1.30V, VDD1 = 1.70~1.95V

Parameter	Symbol	Power Supply	400 MHz	533 MHz	Condition	Unit	
IDD6 Partial Array Self-Refresh Current	Full Array	IDD6 ₁	VDD1	500	500	Self refresh current CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	μA
		IDD6 ₂	VDD2	600	600		
		IDD6 _{IN}	VDDCA VDDQ	35	35		
	1/2 Array	IDD6 ₁	VDD1	450	450		μA
		IDD6 ₂	VDD2	500	500		
		IDD6 _{IN}	VDDCA VDDQ	35	35		
	1/4 Array	IDD6 ₁	VDD1	400	400		μA
		IDD6 ₂	VDD2	450	450		
		IDD6 _{IN}	VDDCA VDDQ	35	35		

Note 1: LPDDR2-S4 SDRAM uses the same PASR scheme & IDD6 current value categorization as LPDDR.

Note 2: IDD values published are the maximum of the distribution of the arithmetic mean.

Single-Ended AC and DC Output Levels

Symbol	Parameter	Value	Units	
$V_{OH(AC)}$	AC output HIGH measurement level	$V_{REF} + 0.12$	V	
$V_{OL(AC)}$	AC output LOW measurement level	$V_{REF} - 0.12$	V	
$V_{OH(DC)}$	DC output HIGH measurement level	$0.9 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output LOW measurement level	$0.1 \times V_{DDQ}$	V	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min.=-15 , Max.= 15	V	
I_{OZ}	Output leakage current (DQ, DM, DQS) (DQ, DQS are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	Min	-5	uA
		Max	5	uA

Note 1: $I_{OH} = -0.1mA$.

Note 2: $I_{OL} = 0.1mA$.

Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2 200-1066	Units
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level	$+ 0.20 \times V_{DDQ}$	V
$V_{OLdiff(AC)}$	AC differential output LOW measurement level	$- 0.20 \times V_{DDQ}$	V

Note 1: $I_{OH} = -0.1mA$.

Note 2: $I_{OL} = 0.1mA$.

Output Slew Rate (Single-Ended)

Symbol	Parameter	LPDDR2-800/1066		Units
		Min	Max	
SRQse	Single-ended Output Slew Rate (RON = $40\Omega \pm 30\%$)	1.5	3.5	V/nS
SRQse	Single-ended Output Slew Rate (RON = $60\Omega \pm 30\%$)	1.0	2.5	V/nS
	Output slew-rate matching Ratio (Pull-up to Pull-down)	0.7	1.4	

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

Differential Output Slew Rate

Symbol	Parameter	LPDDR2-800/1066		Units
		Min	Max	
SRQdiff	Differential Output Slew Rate (RON = $40\Omega \pm 30\%$)	3.0	7.0	V/nS
SRQdiff	Differential Output Slew Rate (RON = $60\Omega \pm 30\%$)	2.0	5.0	V/nS

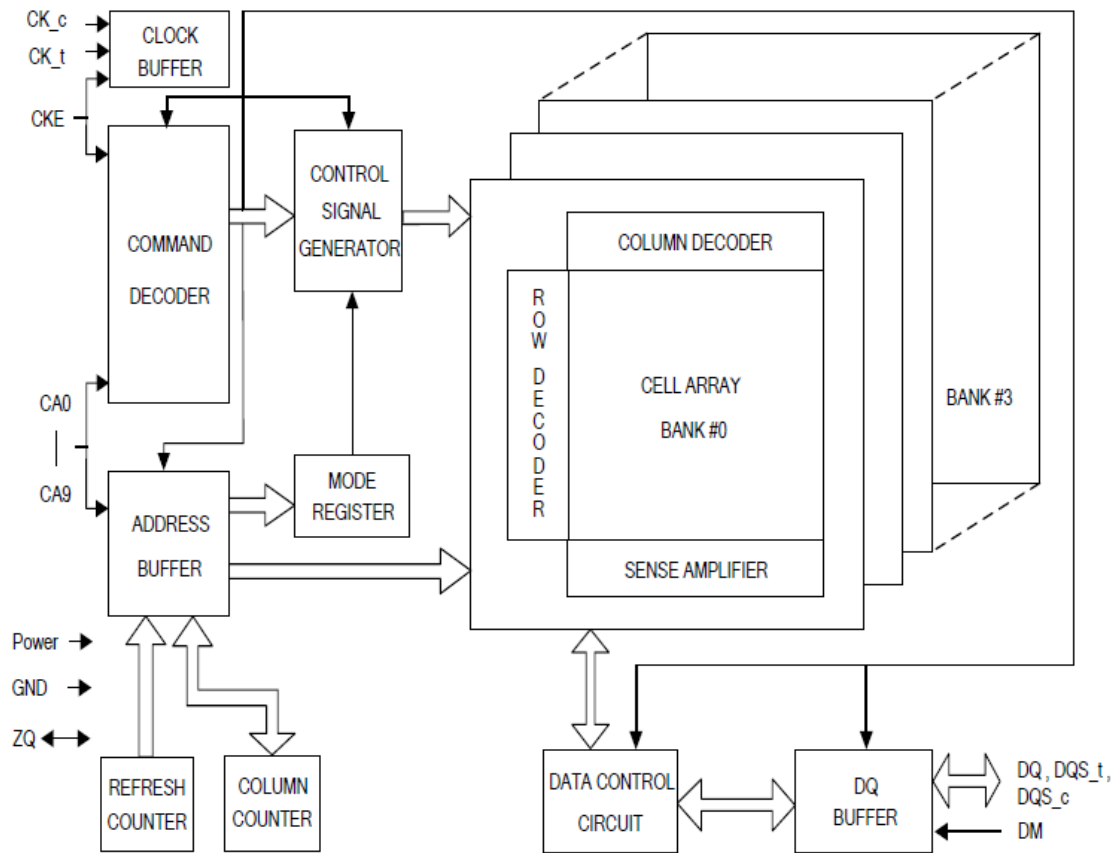
Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: differential Signals

BLOCK DIAGRAM



AC Characteristics

(V_{DD2} , V_{DDQ} , $V_{DDCA}=1.14\sim 1.30V$, $V_{DD1}=1.70\sim 1.95V$)

Parameter	Symbol	min / max	min tCK	Data Rate							Unit
				1066	933	800	667	533	400	333	
Max. Frequency ⁴		~		533	466	400	333	266	200	166	MHz
Clock Timing											
Average Clock Period	tCK(avg)	MIN		1.875	2.15	2.5	3	3.75	5	6	nS
		MAX		100							
Average high pulse width	tCH(avg)	MIN		0.45							tCK(avg)
		MAX		0.55							
Average low pulse width	tCL(avg)	MIN		0.45							tCK(avg)
		MAX		0.55							
Absolute Clock Period	tCK(abs)	MIN		tCK(avg)min + tJIT(per)min							pS
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	MIN		0.43							tCK(avg)
		MAX		0.57							
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), (allowed)	MIN		0.43							tCK(avg)
		MAX		0.57							
Clock Period Jitter (with allowed jitter)	tJIT(per), (allowed)	MIN		-90	-95	-100	-110	-120	-140	-150	pS
		MAX		90	95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	MAX		180	190	200	220	240	280	300	pS
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	MIN		MIN ((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg)							pS
		MAX		MAX ((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg)							pS
Cumulative error across 2 cycles	tERR(2per), (allowed)	MIN		-132	-140	-147	-162	-177	-206	-221	pS
		MAX		132	140	147	162	177	206	221	
Cumulative error across 3 cycles	tERR(3per), (allowed)	MIN		-157	-166	-175	-192	-210	-245	-262	pS
		MAX		157	166	175	192	210	245	262	
Cumulative error across 4 cycles	tERR(4per), (allowed)	MIN		-175	-185	-194	-214	-233	-272	-291	pS
		MAX		175	185	194	214	233	272	291	
Cumulative error across 5 cycles	tERR(5per), (allowed)	MIN		-188	-199	-209	-230	-251	-293	-314	pS
		MAX		188	199	209	230	251	293	314	
Cumulative error across 6 cycles	tERR(6per), (allowed)	MIN		-200	-211	-222	-244	-266	-311	-333	pS
		MAX		200	211	222	244	266	311	333	
Cumulative error across 7 cycles	tERR(7per), (allowed)	MIN		-209	-221	-232	-256	-279	-325	-348	pS
		MAX		209	221	232	256	279	325	348	
Cumulative error across 8 cycles	tERR(8per), (allowed)	MIN		-217	-229	-241	-266	-290	-338	-362	pS
		MAX		217	229	241	266	290	338	362	
Cumulative error across 9 cycles	tERR(9per), (allowed)	MIN		-224	-237	-249	-274	-299	-349	-374	pS
		MAX		224	237	249	274	299	349	374	
Cumulative error across 10 cycles	tERR(10per), (allowed)	MIN		-231	-244	-257	-282	-308	-359	-385	pS
		MAX		231	244	257	282	308	359	385	
Cumulative error across 11 cycles	tERR(11per), (allowed)	MIN		-237	-250	-263	-289	-316	-368	-395	pS
		MAX		237	250	263	289	316	368	395	
Cumulative error across 12 cycles	tERR(12per), (allowed)	MIN		-242	-256	-269	-296	-323	-377	-403	pS
		MAX		242	256	269	296	323	377	403	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper), (allowed)	MIN		tERR(nper),allowed,min = (1 + 0.68ln(n)) * tJIT(per),allowed,min							pS
		MAX		tERR(nper),allowed,max = (1 + 0.68ln(n)) * tJIT(per),allowed,max							

Parameter	Symbol	min / max	min tCK	Data Rate							Unit
				1066	933	800	667	533	400	333	
ZQ Calibration Parameters											
Initialization Calibration Time	tZQINIT	MIN		1							μS
Full Calibration Time	tZQCL	MIN	6	360							nS
Short Calibration Time	tZQCS	MIN	6	90							nS
Calibration Reset Time	tZQRESET	MIN	3	50							nS
Read Parameters^{**1}											
DQS output access time from CK_t/CK_c	tDQSCK	MIN		2500							pS
		MAX		5500							
DQSCK Delta Short ^{**15}	tDQSCKDS	MAX		330	380	450	540	670	900	1080	pS
DQSCK Delta Medium ^{**16}	tDQSCKDM	MAX		680	780	900	1050	1350	1800	1900	pS
DQSCK Delta Long ^{**17}	tDQSCKDL	MAX		920	1050	1200	1400	1800	2400	-	pS
DQS - DQ skew	tDQSQ	MAX		200	220	240	280	340	400	500	pS
Data hold skew factor	tQHS	MAX		230	260	280	340	400	480	600	pS
DQS Output High Pulse Width	tQSH	MIN		tCH(abs) - 0.05							tCK(avg)
DQS Output Low Pulse Width	tQSL	MIN		tCL(abs) - 0.05							tCK(avg)
Data Half Period	tQHP	MIN		min(tQSH, tQSL)							tCK(avg)
DQ / DQS output hold time from DQS	tQH	MIN		tQHP - tQHS							pS
Read preamble ^{**12,13}	tRPRE	MIN		0.9							tCK(avg)
Read postamble ^{**12,14}	tRPST	MIN		tCL(abs) - 0.05							tCK(avg)
DQS low-Z from clock ^{**12}	tLZ(DQS)	MIN		tDQSCK(MIN) - 300							pS
DQ low-Z from clock ^{**12}	tLZ(DQ)	MIN		tDQSCK(MIN) - (1.4 * tQHS(MAX))							pS
DQS high-Z from clock ^{**12}	tHZ(DQS)	MAX		tDQSCK(MAX) - 100							pS
DQ high-Z from clock ^{**12}	tHZ(DQ)	MAX		tDQSCK(MAX) + (1.4 * tDQSQ(MAX))							pS
Write Parameters^{**1}											
DQ and DM input hold time (Vref based)	tDH	MIN		210	235	270	350	430	480	600	pS
DQ and DM input setup time (Vref based)	tDS	MIN		210	235	270	350	430	480	600	pS
DQ and DM input pulse width	tDIPW	MIN		0.35							tCK(avg)
Write command to 1st DQS latching transition	tDQSS	MIN		0.75							tCK(avg)
		MAX		1.25							
DQS input high-level width	tDQSH	MIN		0.4							tCK(avg)
DQS input low-level width	tDQSL	MIN		0.4							tCK(avg)
DQS falling edge to CK setup time	tDSS	MIN		0.2							tCK(avg)
DQS falling edge hold time from CK	tDSH	MIN		0.2							tCK(avg)
Write postamble	tWPST	MIN		0.4							tCK(avg)
Write preamble	tWPRE	MIN		0.35							tCK(avg)
CKE Input Parameters											
CKE min. pulse width (high and low pulse width)	tCKE	MIN	3	3							tCK(avg)
CKE input setup time	tISCKE ^{**2}	MIN		0.25							tCK(avg)
CKE input hold time	tIHCKE ^{**3}	MIN		0.25							tCK(avg)

Parameter	Symbol	min / max	min tCK	Data Rate							Unit
				1066	933	800	667	533	400	333	
Command Address Input Parameters^{*11}											
Address and control input setup time (Vref based)	tIS ^{*1}	MIN		220	250	290	370	460	600	740	pS
Address and control input hold time (Vref based)	tIH ^{*1}	MIN		220	250	290	370	460	600	740	pS
Address and control input pulse width	tIPW	MIN		0.40							tCK(avg)
Boot Parameters (10 MHz - 55 MHz)^{*5, 7, 8}											
Clock Cycle Time	tCKb	MAX		100							nS
		MIN		18							
CKE Input Setup Time	tISCKEb	MIN		2.5							nS
CKE Input Hold Time	tIHCKEb	MIN		2.5							nS
Address & Control Input Setup Time	tISb	MIN		1150							pS
Address & Control Input Hold Time	tIHb	MIN		1150							pS
DQS Output Data Access Time from CK_t/CK_c	tDQSCkCb	MIN		2.0							nS
		MAX		10.0							
Data Strobe Edge to Output Data Edge tDQSQb - 1.2	tDQSQb	MAX		1.2							nS
Data Hold Skew Factor	tQHSb	MAX		1.2							nS
Mode Register Parameters											
MODE REGISTER Write command period	tMRW	MIN	5	5							tCK(avg)
Mode Register Read command period	tMRR	MIN	2	2							tCK(avg)
LPDDR2 SDRAM Core Parameters^{*9}											
Read Latency	RL	MIN	3	8	7	6	5	4	3	3	tCK(avg)
Write Latency	WL	MIN	1	4	4	3	2	2	1	1	tCK(avg)
ACTIVE to ACTIVE command period	tRC	MIN		tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)							nS
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	MIN	3	15							nS
Self refresh exit to next valid command delay	tXSR	MIN	2	tRFCab + 10							nS
Exit power down to next valid command delay	tXP	MIN	2	7.5							nS
CAS to CAS delay	tCCD	MIN	2	2							tCK(avg)
Internal Read to Precharge command delay	tRTP	MIN	2	7.5							nS
RAS to CAS Delay	tRCD	Fast	3	15							nS
Row Precharge Time (single bank)	tRPpb	Fast	3	15							nS
Row Precharge Time (all banks)	tRPab 4-bank	Fast	3	15							nS
Row Active Time	tRAS	MIN	3	42							nS
		MAX	-	70							μS
Write Recovery Time	tWR	MIN	3	15							nS
Internal Write to Read Command Delay	tWTR	MIN	2	7.5					10		nS
Active bank A to Active bank B	tRRD	MIN	2	10							nS
Four Bank Activate Window	tFAW	MIN	8	50					60		nS
Minimum Deep Power Down Time	tDPD	MIN		500							μS

Parameter	Symbol	min / max	min tCK	Data Rate						Unit
				1066	933	800	667	533	400	
LPDDR2 Temperature De-Rating										
tDQSCK De-Rating	tDQSCK (Derated)	MAX		5620	6000					pS
Core Timings Temperature De-Rating	tRCD (Derated)	MIN		tRCD + 1.875					nS	
	tRC (Derated)	MIN		tRC + 1.875					nS	
	tRAS (Derated)	MIN		tRAS + 1.875					nS	
	tRP (Derated)	MIN		tRP + 1.875					nS	
	tRRD (Derated)	MIN		tRRD + 1.875					nS	

Note 1: Input set-up/hold time for signal (CA[0:n], CS_n).

Note 2: CKE input setup time is measured from CKE reaching high/low voltage level to CK_t/CK_c crossing.

Note 3: CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching high/low voltage level.

Note 4: Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.

Note 5: To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.

Note 6: Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.

Note 7: The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition".

Note 8: The output skew parameters are measured with Ron default settings into the reference load.

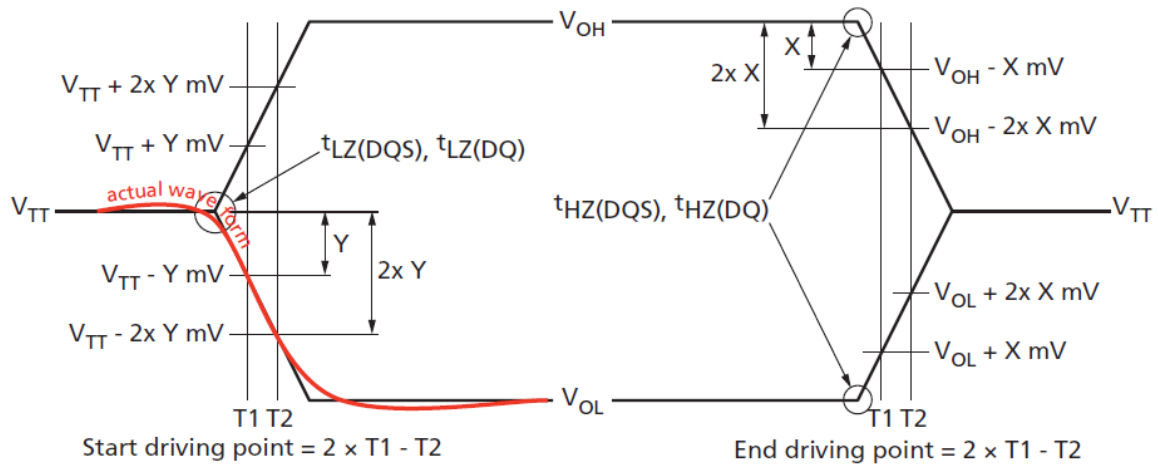
Note 9: The min tCK column applies only when tCK is greater than 6nS for LPDDR2-S4 devices.

Note 10: All AC timings assume an input slew rate of 1V/nS.

Note 11: Read, Write, and Input Setup and Hold values are referenced to Vref.

Note 12: For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Below "HSUL_12 Driver Output Reference Load for Timing and Slew Rate" figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

Output Transition Timing



Note 13: Measured from the start driving of DQS_t - DQS_c to the start driving the first rising strobe edge.

















Note 14: Measured from the from start driving the last falling strobe edge to the stop driving DQS_t, DQS_c.

Note 15: tDQCKDS is the absolute value of the difference between any two tDQCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

Note 16: tDQCKDM is the absolute value of the difference between any two tDQCK measurements (within a byte lane) within a 1.6µs rolling window. tDQCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

Note 17: tDQCKDL is the absolute value of the difference between any two tDQCK measurements (within a byte lane) within a 32ms rolling window. tDQCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

Command Truth Table

Command	Command Pins		DDR CA Pins (10)											CK_t EDGE
	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	X								
Refresh (all bank)	H	H	L	L	L	H	H	X						
			X	X										
Enter Self Refresh	H	L	L	L	L	H	X							
	X		X											
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	X	
			X	R0	R1	R2	R3	R4	R5	R6	R7	X	X	
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	X	
			X	AP ^{*3,4}	C3	C4	C5	C6	C7	C8	X	X	X	
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	X	
			X	AP ^{*3,4}	C3	C4	C5	C6	C7	C8	X	X	X	
Precharge (per bank, all bank)	H	H	L	H	H	L	H	AB ^{*12}	X	X	BA0	BA1	X	
			X	X										
BST	H	H	L	H	H	L	L	X						
			X	X										
Enter Deep Power Down	H	L	L	H	H	L	X							
	X		X											
NOP	H	H	L	H	H	H	X							
			X	X										
Maintain PD,SREF,DPD (NOP)	L	L	L	H	H	H	X							
			X	X										
NOP	H	H	H	X										
			X	X										
Maintain PD,SREF,DPD (NOP)	L	L	H	X										
			X	X										
Enter Power Down	H	L	H	X										
	X		X											
Exit PD, SREF,DPD	L	H	H	X										
	X		X											

Note 1: All commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.

Note 2: For LPDDR2 SDRAM, Bank addresses BA0 and BA1 (BA) determine which bank is to be operated upon.

Note 3: AP is significant only to SDRAM.

Note 4: AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

Note 5: “X” means “H or L (but a defined logic level)”.

Note 6: Self refresh exit and Deep Power Down exit are asynchronous.

Note 7: VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.

Note 8: CAxr refers to command/address bit “x” on the rising edge of clock.

Note 9: CAxf refers to command/address bit “x” on the falling edge of clock.

Note 10: CS_n and CKE are sampled at the rising edge of clock.

Note 11: The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

Note 12: AB “high” during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

CKE Truth Table

Device Current State ³	CKEn-1 ¹	CKEn ¹	CS_n ²	Command n ⁴	Operation n ⁴	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Dow	
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Others states	H	H	Refer to the Command Truth Table				

Note 1: “CKEn” is the logic state of CKE at clock rising edge n; “CKEn-1” was the state of CKE at the previous clock edge.

Note 2: “CS_n” is the logic state of CS_n at the clock rising edge n;.

Note 3: “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.

Note 4: “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.

Note 5: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note 6: Power Down exit time (tXP) should elapse before a command other than NOP is issued.

Note 7: Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.

Note 8: The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.

Note 9: The clock must toggle at least once during the tXP period.

Note 10: The clock must toggle at least once during the tXSR time.

Note 11: X' means 'Don't care'.

Note 12: Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

Current State Bank n – Command to Bank n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	6
	MRW	Load value to Mode Register	MR Writing	6
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6, 7
Row Active	Precharge	Deactivate row in bank or banks	Precharging	8, 14
	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
Reading	Precharge	Deactivate row in bank or banks	Precharging	8
	Read	Select column, and start new read burst	Reading	9, 10
	Write	Select column, and start write burst	Writing	9, 10, 11
Writing	BST	Read burst terminate	Active	12
	Write	Select column, and start new write burst	Writing	9, 10
	Read	Select column, and start read burst	Reading	9, 10, 13
Power On	Reset	Begin Device Auto-Initialization	Resetting	6, 8
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note 1: Values in this table apply when both CKEn -1 and CKEn are HIGH, and after tXSR or tXP has been met, if the previous state was power-down.

Note 2: All states and sequences not shown are illegal or reserved.

Note 3: Current state definitions:

State	Definition
Idle	The bank or banks have been precharged, and tRP has been met.
Active	A row in the bank has been activated, and tRCD has been met. No data bursts or accesses, and no register accesses, are in progress.
Reading	A READ burst has been initiated with auto precharge disabled, and has not yet terminated.
Writing	A WRITE burst has been initiated with auto precharge disabled, and has not yet terminated.

Note 4: The states listed below must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in the table: Current State Bank n to Command to Bank m..

State	Starts With...	Ends When..	Notes
Precharging	Registration of a PRECHARGE command	tRP is met	After tRP is met, the bank is in the idle state.

State	Starts With...	Ends When..	Notes
Row activating	Registration of an ACTIVATE command	tRCD is met	After tRCD is met, the bank is in the active state.
READ with AP enabled	Registration of a READ command with auto precharge enabled	tRP is met	After tRP is met, the bank is in the idle state.
WRITE with AP enabled	Registration of a WRITE command with auto precharge enabled	tRP is met	After tRP is met, the bank is in the idle state.

Note 5: The states listed below must not be interrupted by any executable command. NOP commands must be applied to each positive clock edge during these states.

State	Starts With...	Ends When..	Notes
Refreshing (all banks)	Registration of a REFRESH (all banks) command	tRFCab is met	After tRFCab is met, the device is in the all banks idle state.
Idle MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks idle state.
Resetting MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks idle state.
Active MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	tMRW is met	After tMRW is met, the device is in the all banks idle state.
Precharging all	Registration of a PRECHARGE ALL command	tRP is met	After tRP is met, the device is in the all banks idle state.

Note 6: Not bank-specific; requires that all banks are idle and no bursts are in progress.

Note 7: Not bank-specific reset command is achieved through Mode Register Write command.

Note 8: This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre-charging.

Note 9: A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

Note 10: The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.

Note 11: A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.

Note 12: Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.

Note 13: A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.

Note 14: If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

Current State Bank n – Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note 1: This table applies when:

- The previous state was self refresh or power-down;
- After tXSR or tXP has been met; and when both CKEn -1 and CKEn are HIGH.

Note 2: All states and sequences not shown are illegal or reserved..

Note 3: Current state definitions:

State	Condition	And...	And...
Idle	The bank has been precharged	tRP is met	
Active	A row in the bank has been activated	tRCD is met	No data bursts/accesses and no register accesses are in progress.
Reading	A READ burst has been initiated with auto precharge disabled	The READ has not yet terminated	
Writing	A WRITE burst has been initiated with auto precharge disabled	The WRITE has not yet terminated	

Note 4: Refresh, self refresh, and MRW commands can only be issued when all banks are idle.

Note 5: A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.

Note 6: The states listed below must not be interrupted by any executable command. NOP commands must be

applied during each clock cycle while in these states:

State	Starts With...	Ends When..	Notes
Idle MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks idle state.
Resetting MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the device is in the all banks reset state.
Active MR reading	Registration of the MRR command	tMRR is met	After tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	tMRW is met	After tMRW is met, the device is in the all banks idle state.

Note 7: tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.

Note 8: Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.

Note 9: This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre-charging.

Note 10: MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met).

Note 11: MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met).

Note 12: Not bank-specific; requires that all banks are idle and no bursts are in progress.

Note 13: The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.

Note 14: A Write command may be applied after the completion of the Read burst; otherwise a BST must be issued to end the Read prior to asserting a Write command.

Note 15: Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks.

Note 16: A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.

Note 17: Reset command is achieved through Mode Register Write command

Note 18: BST is allowed only if a Read or Write burst is ongoing.

IDD Measurement Conditions

Switching for CA Input Signals

	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)	CK _t (Rising) /CK _c (Falling)	CK _t (Falling) /CK _c (Rising)
Cycle	N		N+1		N+2		N+3	
/CS	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes 1: CS_n must always be driven HIGH.

Notes 2: For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.

Notes 3: The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Switching for IDD4R

Clock	CKE	CS _n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes 1: Data strobe (DQS_t) is changing between HIGH and LOW with every clock cycle.

Notes 2: The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

Power-up, Initialization, and Power-Off

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure are mandatory.

Power Ramp

While applying power (after Ta), CKE must be held LOW ($\leq 0.2 \times VDDCA$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Table below..

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2 - 200mV
	VDD1 and VDD2 must be greater than VDDCA - 200mV
	VDD1 and VDD2 must be greater than VDDQ - 200mV
	VREF must always be less than all other supply voltages

Notes 1: Ta is the point when any power supply first reaches 300mV.

Notes 2: The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.

Notes 3: The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 mS.

CKE and clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100 nS, after which it may be asserted high. Clock must be stable at least tINIT2 = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for tCKb (18 nS to 100 nS), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. tDQSCK) may have relaxed timings (e.g. tDQSCKb) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least tINIT3 = 200 μ S. (Td).

Reset command

After tINIT3 is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least tINIT4 = 1 μ S while keeping CKE asserted and issuing NOP commands.

Mode Registers Reads and Device Auto-Initialization (DAI) polling

After t_{INIT4} is satisfied (T_e) only MRR commands and power-down entry/exit commands are allowed. Therefore, after T_e , CKE may go low in accordance to Power-Down entry and exit specification. The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of t_{INIT5} before proceeding. As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured. After the DAI-bit (MR#0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (T_f). The state of the DAI status bit can be determined by an MRR command to MR#0. The LPDDR2 SDRAM device will set the DAI-bit no later than t_{INIT5} (10 μ S) after the Reset command. The memory controller shall wait a minimum of t_{INIT5} or until the DAI-bit is set before proceeding. After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).

ZQ Calibration

After t_{INIT5} (T_f), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after t_{ZQINIT} .

Normal Operation

After t_{ZQINIT} (T_g), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration. The LPDDR2 device will now be in IDLE state and ready for any valid command. After T_g , the clock frequency may be changed according to the clock frequency change procedure

Mode Register Definition

For LPDDR2, a set of mode registers is used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment and Definition

Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register

Mode Register Assignments

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00H	Device Info.	R	(RFU)			RZQI	DNVI	DI	DAI	
1	01H	Device Feature 1	W	nWR (for AP)		WC	BT	BL			
2	02H	Device Feature 2	W	(RFU)			RL & WL				
3	03H	I/O Config-1	W	(RFU)			DS				
4	04H	Refresh Rate	R	TUF	(RFU)			Refresh Rate			
5	05H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06H	Basic Config-2	R	Revision ID1							
7	07H	Basic Config-3	R	Revision ID2							
8	08H	Basic Config-4	R	I/O width		Density			Type		
9	09H	Test Mode	W	Vendor-Specific Test Mode							
10	0AH	I/O Calibration	W	Calibration Code							
11-15	0BH~0FH	(reserved)	-	(RFU)							
16	10H	PASR_Bank	W	Bank Mask							
17	11H	(Reserved)	W	(RFU)							
18-19	12H~13H	(Reserved)	-	(RFU)							
20-31	14h - 1Fh	Reserved for NVM									
32	20H	DQ Calibration Pattern A	R	See 7.4.20.2 "DQ Calibration"							
33-39	21H~27H	(Do Not Use)	-								
40	28H	DQ Calibration Pattern B	R	See 7.4.20.2 "DQ Calibration"							
41-47	29H~2FH	(Do Not Use)	-								
48-62	30H~3EH	(Reserved)	-	(RFU)							
63	3FH	Reset	W	X							
64-126	40H~7EH	(Reserved)	-	(RFU)							
127	7FH	(Do Not Use)	-								
128-190	80H~BEH	(Reserved for Vendor Use)	-	(RFU)							
191	BFH	(Do Not Use)	-								
192-254	C0H~FEH	(Reserved for Vendor Use)	-	(RFU)							
255	FFH	(Do Not Use)	-								

Notes 1: RFU bits must be set to "0" during Mode Register writes.

Notes 2: RFU bits must be read as "0" during Mode Register reads.

Notes 3: All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.

Notes 4: All mode registers that are specified as RFU shall not be written.

Notes 5: Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA[7:0] = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0b: DAI complete 1b: DAI still in progress
DI (Device Information)	Read-only	OP1	0b: S4 SDRAM
DNVI (Data Not Valid Information)	Read-only	OP2	0b: LPDDR2 SDRAM will not implement DNV functionality
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	00b: RZQ self test not executed. 01b: ZQ-pin may connect to VDDCA or float 10b: ZQ-pin may short to GND 11b: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

Notes 1: RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.

Notes 2: If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

Notes 3: In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 as defined above), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

Notes 4: In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240 Ohm \pm 1%).

MR1_Device Feature 1 (MA[7:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP[2:0]	010b: BL4 (default) 011b: BL8 100b: BL16 All others: Reserved
BT	Write-only	OP3	0b: Sequential (default) 1b: Interleaved
WC	Write-only	OP4	0b: Wrap (default) 1b: No wrap (allowed for SDRAM BL4 only)
nWR	Write-only	OP[7:5]	001b: nWR=3 (default) 010b: nWR=4 011b: nWR=5 100b: nWR=6 101b: nWR=7 110b: nWR=8 All others: Reserved

Notes 1: Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by $RU(tWR/tCK)$.

MR2_Device Feature 2 (MA[7:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			
RL & WL	Write-only	OP[3:0]	0001b: RL = 3 / WL = 1 (default) 0010b: RL = 4 / WL = 2 0011b: RL = 5 / WL = 2 0100b: RL = 6 / WL = 3 0101b: RL = 7 / WL = 4 0110b: RL = 8 / WL = 4 All others: Reserved				

MR3_I/O Configuration 1 (MA[7:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			
DS	Write-only	OP[3:0]	0000b: Reserved 0001b: 34.3-ohm typical 0010b: 40-ohm typical (default) 0011b: 48-ohm typical 0100b: 60-ohm typical 0101b: Reserved for 68.6-ohm typical 0110b: 80-ohm typical 0111b: 120-ohm typical All others: Reserved				

MR4_Device Temperature (MA[7:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		
SDRAM Refresh Rate	Read-only	OP[2:0]	000b: SDRAM Low temperature operating limit exceeded 001b: 4x tREFI, 4x tREFW 010b: 2x tREFI, 2x tREFW 011b: 1x tREFI, 1x tREFW ($\leq 85^{\circ}\text{C}$) 100b: Reserved 101b: 0.25x tREFI, 0.25x tREFW, do not de-rate SDRAM AC timing 110b: 0.25x tREFI, 0.25x tREFW, de-rate SDRAM AC timing 111b: SDRAM High temperature operating limit exceeded				
Temperature Update Flag (TUF)	Read-only	OP7	0b: OP[2:0] value has not changed since last read of MR4. 1b: OP[2:0] value has changed since last read of MR4.				

Notes 1: A Mode Register Read from MR4 will reset OP7 to '0'.

Notes 2: OP7 is reset to '0' at power-up.

Notes 3: If OP2 equals '1', the device temperature is greater than 85°C.

Notes 4: OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.

Notes 5: LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.

Notes 6: For specified operating temperature range and maximum operating temperature, refer to "Operating Temperature Conditions" table.

Notes 7: LPDDR2 devices must be derated by adding 1.875 nS to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in "LPDDR2 AC Timing" table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

MR5_Basic Configuration 1 (MA[7:0] = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							
LPDDR2 Manufacturer ID		Read-only	OP[7:0]		0000 1000b:		

MR8_Basic Configuration 4 (MA[7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	
Type	Read-only	OP[1:0]		00 _b : S4 SDRAM			
Density	Read-only	OP[5:2]		0010 _b : 256Mb			
I/O width	Read-only	OP[7:6]		00 _b : x32 01 _b : x16			

MR10_Calibration (MA[7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							
Calibration Code	Write-only		OP[7:0]		0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved		

Notes 1: Host processor shall not write MR10 with “Reserved” values.

Notes 2: LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.

Notes 3: See AC timing table for the calibration latency.

Notes 4: If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see section 7.4.23 “Mode Register Write ZQ Calibration Command”) or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

Notes 5: Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR16_PASR_Bank Mask (MA[7:0] = 10H)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 SDRAM	Reserved				Bank Mask			

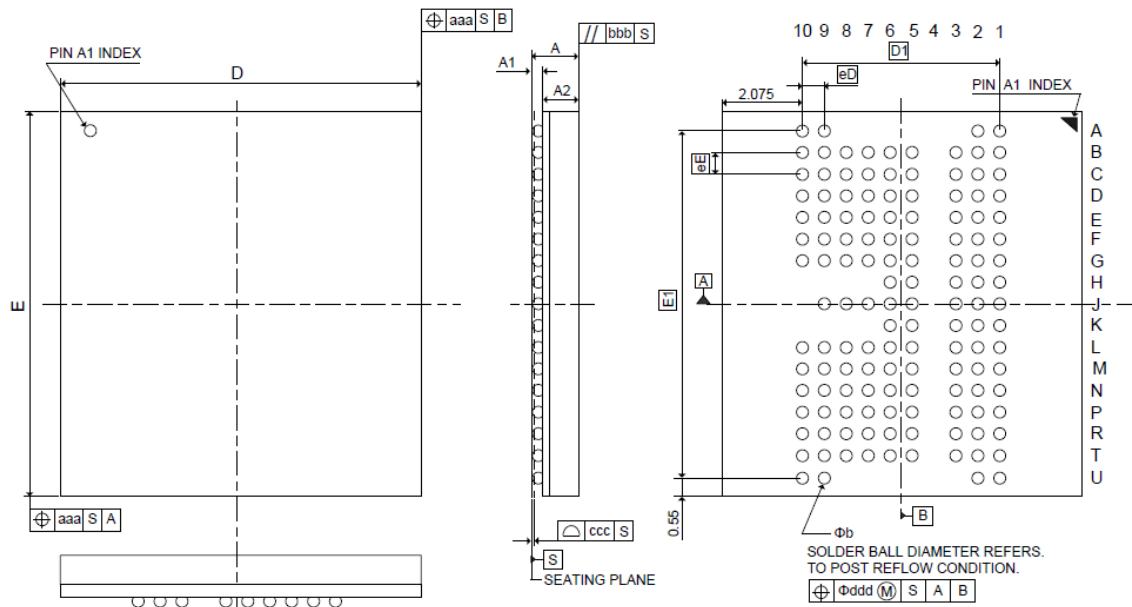
Bank [3:0] Mask	Write-only	OP[3:0]	0b: self-refresh enable to the bank (=unmasked, default) 1b: self-refresh blocked (=masked) OP0: bank 0 OP1: bank 1 OP2: bank 2 OP3: bank 3
Reserved	Write-only	OP[7:4]	Reserved. Any value written to OP[7:4] are ignored by LPDDR2.

Notes: The MR16 is used to control which bank or banks are to be masked or unmasked in self-refresh mode. It has no effect in autorefresh mode because LPDDR2 256Mb device does not support per-bank refresh in auto-refresh mode.

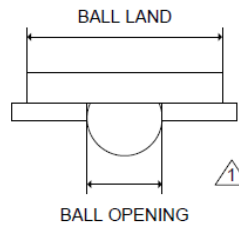
OP	Bank Mask	4-Bank S4 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	-	-
5	-	-
6	-	-
7	-	-

Package Description

134-ball FBGA



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.27	0.32	0.37
A2	0.53	0.58	0.63
b	0.35	0.40	0.45
D	9.90	10.00	10.10
E	11.40	11.50	11.60
D1	5.85 BSC.		
E1	10.40 BSC.		
eD	0.65 BSC.		
eE	0.65 BSC.		
aaa	0.15		
bbb	---	---	0.10
ccc	---	---	0.08
ddd	---	---	0.08



- Note:**
1. Ball land: 0.45mm, Ball opening: 0.35mm.
 2. PCB Ball land suggested ≤ 0.35 mm.

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	June. 2022	Rico Yang	N/A
1.0	First SPEC. release.	July. 2022	Rico Yang	N/A