

4Gb (16Mx8Banksx32) Low Power DDR4 SDRAM

Descriptions

H2AB04G32D6B uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. To achieve high-speed operation, our H2AB04G32D6B SDRAM adopt 16n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the H2AB04G32D6B effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal SDRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the H2AB04G32D6B are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For H2AB04G32D6B devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Features

- Frequency to 2133MHz (data rate: 4266Mbps/pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Data width: x32
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable Burst Lengths: 16,32
- Interface: LVSTL_11
- Burst type: Sequential
- Programmable Driver strength
- Support write mask and data bus inversion (DBI)
- On-die termination (ODT)
- Auto Refresh and Self Refresh Modes
- Input clock stop and frequency change
- Write leveling support
- DQ-DQS training
- Target Row Refresh Mode
- CA training support
- FBGA “green” package - 200-ball FBGA
- Operating temperature range :
Commercial : 0°C to 85°C
- Double data rate architecture on the DQ pins
- VDD1/VDD2/VDDQ= 1.8V/1.1V/1.1V

Ordering Information

| Part No | Organization | Max. Data Rate | Package | Grade |
|-------------------|--------------|----------------|--------------------------|------------|
| H2AB04G32D6BKAAC | 128M X 32 | LP DDR4-3200 | 200Ball BGA,10x14.5mm | Commercial |
| H2AB04G32D6BPAAAC | 128M X 32 | LP DDR4-3733 | | Commercial |
| H2AB04G32D6BQAAC | 128M X 32 | LP DDR4-4266 | | Commercial |

Pin Assignment

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|-------|----------|----------|--------|------|---|---|--------|--------|----------|---------|-------|
| A | DNU | DNU | VSS | VDD2 | ZQ0 | | | NC | VDD2 | VSS | DNU | DNU |
| B | SEN_A | DQ0_A | VDDQ | DQ7_A | VDDQ | | | VDDQ | DQ15_A | VDDQ | DQ8_A | DNU |
| C | VSS | DQ1_A | DMI0_A | DQ6_A | VSS | | | VSS | DQ14_A | DMI1_A | DQ9_A | VSS |
| D | VDDQ | VSS | DQS0_t_A | VSS | VDDQ | | | VDDQ | VSS | DQS1_t_A | VSS | VDDQ |
| E | VSS | DQ2_A | DQS0_e_A | DQ5_A | VSS | | | VSS | DQ13_A | DQS1_e_A | DQ10_A | VSS |
| F | VDD1 | DQ3_A | VDDQ | DQ4_A | VDD2 | | | VDD2 | DQ12_A | VDDQ | DQ11_A | VDD1 |
| G | VSS | ODT_CA_A | VSS | VDD1 | VSS | | | VSS | VDD1 | VSS | NC | VSS |
| H | VDD2 | CA0_A | NC | CS0_A | VDD2 | | | VDD2 | CA2_A | CA3_A | CA4_A | VDD2 |
| J | VSS | CA1_A | VSS | CKE0_A | NC | | | CK_t_A | CK_e_A | VSS | CA5_A | VSS |
| K | VDD2 | VSS | VDD2 | VSS | NC | | | NC | VSS | VDD2 | VSS | VDD2 |
| L | | | | | | | | | | | | |
| M | | | | | | | | | | | | |
| N | VDD2 | VSS | VDD2 | VSS | NC | | | NC | VSS | VDD2 | VSS | VDD2 |
| P | VSS | CA1_B | VSS | CKE0_B | NC | | | CK_t_B | CK_e_B | VSS | CA5_B | VSS |
| R | VDD2 | CA0_B | NC | CS0_B | VDD2 | | | VDD2 | CA2_B | CA3_B | CA4_B | VDD2 |
| T | VSS | ODT_CA_B | VSS | VDD1 | VSS | | | VSS | VDD1 | VSS | RESET_n | VSS |
| U | VDD1 | DQ3_B | VDDQ | DQ4_B | VDD2 | | | VDD2 | DQ12_B | VDDQ | DQ11_B | VDD1 |
| V | VSS | DQ2_B | DQS0_e_B | DQ5_B | VSS | | | VSS | DQ13_B | DQS1_e_B | DQ10_B | VSS |
| W | VDDQ | VSS | DQS0_t_B | VSS | VDDQ | | | VDDQ | VSS | DQS1_t_B | VSS | VDDQ |
| Y | VSS | DQ1_B | DMI0_B | DQ6_B | VSS | | | VSS | DQ14_B | DMI1_B | DQ9_B | VSS |
| AA | DNU | DQ0_B | VDDQ | DQ7_B | VDDQ | | | VDDQ | DQ15_B | VDDQ | DQ8_B | SEN_B |
| AB | DNU | DNU | VSS | VDD2 | VSS | | | VSS | VDD2 | VSS | DNU | DNU |

200-Ball FBGA

Pin Description (Simplified)

| Symbol | Type | Description |
|---|-----------|---|
| CK_t_A, CK_c_A, CK_t_B, CK_c_B | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair. |
| CKE_A, CKE_B | Input | Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. Each channel (A & B) has its own CKE signal. |
| CS_A, CS_B | Input | Chip select: CS is part of the command code. Each channel (A & B) has its own CS signal |
| CA[5:0]_A, CA[5:0]_B | Input | Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals. |
| ODT_CA_A, ODT_CA_B | Input | CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. |
| DQ[15:0]_A, DQ[15:0]_B | I/O | Data input/output: Bidirectional data bus. |
| DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B | I/O | Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes. |
| DMI[1:0]_A, DMI[1:0]_B | I/O | Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals. |
| ZQ0 | Reference | ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. The ZQ0 pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor. |
| VDDQ, VDD1, VDD2 | Supply | Power supplies: Isolated on the die for improved noise immunity. |
| VSS, VSSQ | Supply | Ground Reference: Power supply ground reference. |
| RESET_n | Input | RESET: When asserted LOW, the RESET pin resets both channels of the die. |
| SEN | Input | Scan Enable: SEN must be asserted HIGH for enabling boundary scan function. Must be tied to Ground or NC (No Connection) when not in use. |
| DNU | | Do not use: Must be grounded or left floating. |
| NC | | No connect: Not internally connected. |

Absolute Maximum Rating

| Symbol | Item | Rating | Units |
|------------------------------------|-------------------------------------|------------|-------|
| V _{IN} , V _{OUT} | Voltage on any ball relative to VSS | -0.4 ~ 1.5 | V |
| V _{DD1} | VDD1 supply voltage relative to VSS | -0.4 ~ 2.1 | V |
| V _{DD2} | VDD2 supply voltage relative to VSS | -0.4 ~ 1.5 | V |
| V _{DDQ} | VDDQ supply voltage relative to VSS | -0.4 ~ 1.5 | V |
| T _{STG} | Storage Temperature (plastic) | -55 ~ 125 | °C |

Note 1: For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.

Note 2: Storage temperature is the case surface temperature on the center/top side of the device.
For measurement conditions, refer to the JESD51-2 standard.

Input / Output Capacitance

| Symbol | Parameter | Min. | Max. | Units |
|-------------------|--|------|------|-------|
| C _{CK} | Input capacitance, CK _t and CK _c | 0.5 | 0.9 | pF |
| C _{DCK} | Input capacitance delta, CK _t and CK _c | 0 | 0.09 | pF |
| C _I | I Input capacitance, all other input-only pins | 0.5 | 0.9 | pF |
| C _{DI} | Input capacitance delta, all other input-only pins | -0.1 | 0.1 | pF |
| C _{IO} | Input/output capacitance, DQ, DMI, DQS _t , DQS _c | 0.7 | 1.3 | pF |
| C _{DDQS} | Input/output capacitance delta, DQS _t , DQS _c | 0 | 0.1 | pF |
| C _{DIO} | Input/output capacitance delta, DQ, DMI | -0.1 | 0.1 | pF |
| C _{ZQ} | Input/output capacitance, ZQ pin | 0 | 5.0 | pF |

Note 1: This parameter is not subject to production testing. It is verified by design and characterization.

Note 2: Absolute value of CCK_t – CCK_c

Note 3: C_I applies to CS, CKE and CA[5:0].

Note 4: C_{DI} = C_I – 0.5 × (CCK_t + CCK_c); it does not apply to CKE.

Note 5: DMI loading matches DQ and DQS.

Note 6: Absolute value of CDQS_t and CDQS_c.

Note 7: This parameter applies to LPDDR4 die only (does not include package capacitance).

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|------------------|-----------------------|------|------|------|-------|
| V _{DD1} | Core Supply voltage 1 | 1.70 | 1.80 | 1.95 | V |
| V _{DD2} | Core Supply voltage 2 | 1.06 | 1.10 | 1.17 | V |
| V _{DDQ} | I/O buffer power | 1.06 | 1.10 | 1.17 | V |

Notes: 1. VDD1 uses significantly less power than VDD2.

Notes: 2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

Notes: 3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

DC Characteristics

(IDD Specifications; VDD2, VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V)

| Symbol | | Supply | Speed Grade | | Unit |
|--------|---------|--------|-------------|------|------|
| | | | 3733 | 4266 | |
| IDD0 | IDD01 | VDD1 | 9.7 | 9.7 | mA |
| | IDD02 | VDD2 | 47 | 47 | |
| | IDD0Q | VDDQ | 0.2 | 0.2 | |
| IDD2P | IDD2P1 | VDD1 | 0.21 | 0.21 | mA |
| | IDD2P2 | VDD2 | 6 | 6 | |
| | IDD2PQ | VDDQ | 0.2 | 0.2 | |
| IDD2PS | IDD2PS1 | VDD1 | 0.24 | 0.24 | mA |
| | IDD2PS2 | VDD2 | 6 | 6 | |
| | IDD2PSQ | VDDQ | 0.2 | 0.2 | |
| IDD2N | IDD2N1 | VDD1 | 0.21 | 0.21 | mA |
| | IDD2N2 | VDD2 | 29 | 29 | |
| | IDD2NQ | VDDQ | 0.2 | 0.2 | |
| IDD2NS | IDD2NS1 | VDD1 | 0.24 | 0.24 | mA |
| | IDD2NS2 | VDD2 | 22 | 22 | |
| | IDD2NSQ | VDDQ | 0.2 | 0.2 | |
| IDD3P | IDD3P1 | VDD1 | 1.08 | 1.08 | mA |
| | IDD3P2 | VDD2 | 8 | 8 | |
| | IDD3PQ | VDDQ | 0.2 | 0.2 | |
| IDD3PS | IDD3PS1 | VDD1 | 1.07 | 1.07 | mA |
| | IDD3PS2 | VDD2 | 8 | 8 | |
| | IDD3PSQ | VDDQ | 0.2 | 0.2 | |
| IDD3N | IDD3N1 | VDD1 | 1.18 | 1.18 | mA |
| | IDD3N2 | VDD2 | 31 | 31 | |
| | IDD3NQ | VDDQ | 0.2 | 0.2 | |
| IDD3NS | IDD3NS1 | VDD1 | 1.18 | 1.18 | mA |
| | IDD3NS2 | VDD2 | 24 | 24 | |
| | IDD3NSQ | VDDQ | 0.2 | 0.2 | |
| IDD4R | IDD4R1 | VDD1 | 2.96 | 2.96 | mA |
| | IDD4R2 | VDD2 | 330 | 360 | |
| | IDD4RQ | VDDQ | 110 | 110 | |
| IDD4W | IDD4W1 | VDD1 | 2.24 | 2.24 | mA |
| | IDD4W2 | VDD2 | 290 | 320 | |
| | IDD4WQ | VDDQ | 0.5 | 0.5 | |

DC Characteristics(Continued)

(IDD Specifications; VDD2, VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V)

| Symbol | | Supply | Speed | | Unit |
|--------|---------|--------|-------|------|------|
| | | | 3733 | 4266 | |
| IDD5 | IDD51 | VDD1 | 12.4 | 12.4 | mA |
| | IDD52 | VDD2 | 48 | 48 | |
| | IDD5Q | VDDQ | 0.02 | 0.02 | |
| IDD5AB | IDD5AB1 | VDD1 | 0.6 | 0.6 | mA |
| | IDD5AB2 | VDD2 | 29 | 29 | |
| | IDD5ABQ | VDDQ | 0.02 | 0.02 | |
| IDD5PB | IDD5PB1 | VDD1 | 2.68 | 2.68 | mA |
| | IDD5PB2 | VDD2 | 30 | 30 | |
| | IDD5PBQ | VDDQ | 0.2 | 0.2 | |

Notes: 1. ODT disabled: MR11 OP[2:0] = 000b

Notes: 2. Guaranteed by design with output load = 5pF and RON = 40Ω.

Notes: 3. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.

IDD6 Partial Array Self-refresh current; VDD2,VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V

| PASR | Supply | Temp. | | Unit |
|------------|--------|-------|------|------|
| | | 85°C | 95°C | |
| Full Array | VDD1 | 0.43 | 1.3 | mA |
| | VDD2 | 1.85 | 8 | |
| | VDDQ | 0.01 | 0.04 | |

Notes: 1. IDD values reflect dual-channel operation with the same pattern for each channel.

Notes: 2. IDD6 typical value of 85°C. IDD6 85°C is typical of the distribution of the arithmetic mean.

Input Levels for ODT_CA

| Parameter | Symbol | Min. | Max. | Unit |
|----------------------|--------|-------------|-------------|------|
| ODT input HIGH level | VIHODT | 0.75 x VDD2 | VDD2 + 0.2 | V |
| ODT input LOW level | VILODT | -0.2 | 0.25 x VDD2 | V |

Single-Ended Output Slew Rate

| Parameter | Symbol | Value | | Unit |
|---|--------|-------|------|------|
| | | Min. | Max. | |
| Single-ended output slew rate ($V_{OH} = V_{DDQ} \times 0.5$) | SRQse | 3.5 | 9.0 | V/ns |
| Output slew rate matching ratio (rise to fall) | - | 0.8 | 1.2 | - |

Note 1: SR = Slew rate; Q = Query output; se = Single-ended signal.

Note 2: Measured with output reference load.

Note 3: The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Note 4: The output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC) = 0.2 \times V_{OH}(DC)$ and $V_{OH}(AC) = 0.8 \times V_{OH}(DC)$.

Note 5: Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.

Differential Output Slew Rate

| Parameter | Symbol | Value | | Unit |
|---|---------|-------|------|------|
| | | Min. | Max. | |
| Differential output slew rate ($V_{OH} = V_{DDQ} \times 0.5$) | SRQdiff | 7 | 18 | V/ns |

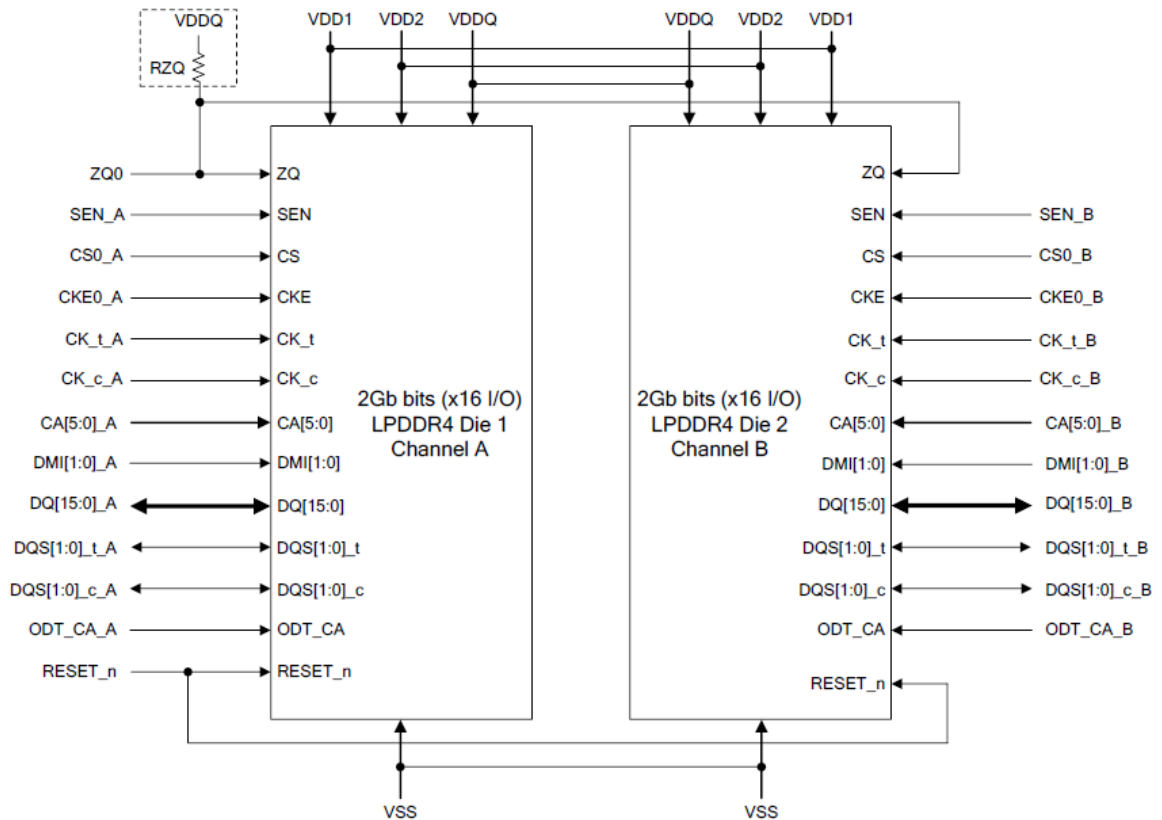
Note 1: SR = Slew rate; Q = Query output; se = Differential signal

Note 2: Measured with output reference load.

Note 3: The output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC) = -0.8 \times V_{OH}(DC)$ and $V_{OH}(AC) = 0.8 \times V_{OH}(DC)$.

Note 4: Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte Switching.

Block Diagram



Note: In dash line block RZQ and VDDQ are external component.

AC Characteristics

($V_{DD2}, V_{DDQ}, V_{DDCA}=1.06\sim 1.17V, V_{DD1}=1.70\sim 1.95V$)

| Symbol | Parameter | Min/Max | Data Rate | | Unit |
|---------------------|--|---------|------------------------------|------|----------|
| | | | 3733 | 4266 | |
| Clock Timing | | | | | |
| tCK(avg) | Average clock period | Min | 535 | 468 | ps |
| | | Max | 100 | 100 | ns |
| tCH(avg) | Average HIGH pulse width | Min | 0.46 | 0.46 | tCK(avg) |
| | | Max | 0.54 | 0.54 | tCK(avg) |
| tCL(avg) | Average LOW pulse width | Min | 0.46 | 0.46 | tCK(avg) |
| | | Max | 0.54 | 0.54 | tCK(avg) |
| tCK(abs) | Absolute clock period | Min | tCK(avg) MIN + tJIT(per) MIN | | ps |
| tCH(abs) | Absolute clock HIGH pulse width | Min | 0.43 | 0.43 | tCK(avg) |
| | | Max | 0.57 | 0.57 | tCK(avg) |
| tCL(abs) | Absolute clock LOW pulse width | Min | 0.43 | 0.43 | tCK(avg) |
| | | Max | 0.57 | 0.57 | tCK(avg) |
| tJIT(per), allowed | Clock period jitter | Min | -34 | -30 | ps |
| | | Max | 34 | 30 | ps |
| tJIT(cc), allowed | Maximum clock jitter between two consecutive clock cycles (with clock period jitter) | Max | 68 | 60 | ps |

AC Characteristics (Continued)
 $(V_{DD2}, V_{DDQ}, V_{DDCA}=1.06\sim 1.17V, V_{DD1}=1.70\sim 1.95V)$

| Symbol | Parameter | Min/ Max | Data Rate | | Unit |
|----------------------------------|---|-------------|--|------|----------|
| | | | 3733 | 4266 | |
| ZQ Calibration Parameters | | | | | |
| tZQCAL | ZQCAL START to ZQCAL LATCH command interval | Min | 1 | | us |
| tZQLAT | ZQCAL LATCH to next valid command interval | Min | MAX(30ns, 8nCK) | | ns |
| tZQRESET | ZQCAL RESET to next valid command interval | Min | MAX(50ns, 3nCK) | | ns |
| READ Parameters | | | | | |
| tDQSCK | DQS output access time from CK | Min | 1500 | | ps |
| | | Max | 3500 | | ps |
| tDQSCK_VOLT | DQS output access time from CK_t/CK_c – voltage variation | Max | 7 | | ps/mV |
| tDQSCK_TEMP | DQS output access time from CK_t/CK_c – temperature variation | Max | 4 | | ps/°C |
| tDQSCK_rank2rank | CK to DQS rank to rank variation | Max | 1.0 | | ns |
| tDQSQ | DQS-DQ skew | Max | 0.18 | | UI |
| tQH | DQ output hold time total from DQS_t, DQS_c | Min | Min (tQSH, tQSL) | | ps |
| tRPRE | READ preamble | Min | 1.8 | | tCK(avg) |
| tRPST | 0.5 tck READ postamble | Min | 0.4 | | tCK(avg) |
| tLZ(DQS) | DQS Low-Z from clock | Min | $(RL \times tCK) + tDQSCK(\text{Min}) - (tRPRE(\text{Max}) \times tCK) - 200\text{ps}$ | | ps |
| tLZ(DQ) | DQ Low-Z from clock | Min | $(RL \times tCK) + tDQSCK(\text{Min}) - 200\text{ps}$ | | ps |
| tHZ(DQS) | DQS High-Z from clock | Min | $(RL \times tCK) + tDQSCK(\text{Max}) + (BL/2 \times tCK) + (tRPST(\text{Max}) \times tCK) - 100\text{ps}$ | | ps |
| tHZ(DQ) | DQ High-Z from clock | Max | $t(RL \times tCK) + tDQSCK(\text{Max}) + tDQSQ(\text{Max}) + (BL/2 \times tCK) - 100\text{ps}$ | | ps |
| tQW_total | Data output valid window time total, per pin | Min | 0.70 | 0.70 | UI |
| tDQSQ_DBI | DQS_t, DQS_c to DQ skew total, per group, per access | Max | 0.18 | | UI |
| tQH_DBI | DQ output hold time total from DQS_t, DQS_c | Min | MIN(tQSH_DBI, tQSL_DBI) | | ps |
| tQW_total_DBI | Data output valid window time total, per pin | Min | 0.70 | 0.70 | UI |
| tQSL | DQS_t, DQS_c differential output LOW time | Min | tCL(abs) – 0.05 | | tCK(avg) |
| tQSH | DQS_t, DQS_c differential output HIGH time | Min | tCH(abs) – 0.05 | | tCK(avg) |
| tQSL-DBI | DQS_t, DQS_c differential output LOW time | Min | tCL(abs) – 0.045 | | tCK(avg) |
| tQSH-DBI | DQS_t, DQS_c differential output HIGH time | Min | tCH(abs) – 0.045 | | tCK(avg) |

AC Characteristics (Continued)
 $(V_{DD2}, V_{DDQ}, V_{DDCA}=1.06\sim 1.17V, V_{DD1}=1.70\sim 1.95V)$

| Symbol | Parameter | Min/ Max | Data Rate | | Unit |
|---|---|-------------|-------------------------------|------|-----------------------|
| | | | 3733 | 4266 | |
| CKE Input Parameters | | | | | |
| t _{CKE} | CKE minimum pulse width(HIGH and LOW pulse width) | Min | Max(7.5ns, 4nCK) | | ns |
| t _{CMDCKE} | Delay from valid command to CKE input LOW | Min | Max(1.75ns, 3nCK) | | ns |
| t _{CKELCK} | Valid clock requirement after CKE input LOW | Min | MAX(5ns, 5nCK) | | ns |
| t _{CSCKE} | Valid CS requirement before CKE input LOW | Min | 1.75 | | ns |
| t _{CKELCS} | Valid CS requirement after CKE input LOW | Min | MAX(5ns, 5nCK) | | ns |
| t _{CKCKEH} | Valid Clock requirement before CKE Input HIGH | Min | MAX(1.75ns, 3nCK) | | ns |
| t _{XP} | Exit power-down to next valid command delay | Min | MAX(7.5ns, 5nCK) | | ns |
| t _{CSCKEH} | Valid CS requirement before CKE input HIGH | Min | 1.75 | | ns |
| t _{CKEHCS} | Valid CS requirement after CKE input HIGH | Min | MAX(7.5ns, 5nCK) | | ns |
| t _{MRWCKEL} | Valid clock and CS requirement after CKE input LOW after MRW command | Min | MAX(14ns, 10nCK) | | ns |
| t _{ZQCKE} | Valid clock and CS requirement after CKE input LOW after ZQ calibration start command | Min | MAX(1.75ns, 3nCK) | | ns |
| Command Address Input Parameters | | | | | |
| t _{clVW} | Command/address valid window | Min | 0.3 | | t _{CK} (avg) |
| t _{clPW} | Address and control input pulse width | Min | 0.6 | | t _{CK} (avg) |
| Boot Parameters (10–55 MHz) | | | | | |
| t _{CKb} | Clock cycle time | Max | - | | ns |
| | | Min | 18 | | ns |
| t _{DQSCKb} | DQS output data access time from CK | Min | TBD | | ns |
| | | Max | TBD | | ns |
| t _{DQSQb} | Data strobe edge to output data edge | Max | TBD | | ns |
| Mode Register Parameters | | | | | |
| t _{MRW} | MODE REGISTER WRITE command period | Min | MAX(10ns, 10nCK) | | ns |
| t _{MRD} | MODE REGISTER SET command delay | Min | MAX(14ns, 10nCK) | | ns |
| t _{MRR} | MODE REGISTER READ command period | Min | 8 | | t _{CK} (avg) |
| t _{MRRl} | Additional time after t _{XP} has expired until MRR command may be issued | Min | t _{RCD} (min) + 3nCK | | ns |
| t _{SDO} | Delay from MRW command to DQS driven out | Max | MAX(12nCK, 20ns) | | ns |

AC Characteristics (Continued)
 $(V_{DD2}, V_{DDQ}, V_{DDCA}=1.06\sim 1.17V, V_{DD1}=1.70\sim 1.95V)$

| Symbol | Parameter | Min/Max | Data Rate | | Unit |
|------------------------|---|---------|--|-------------------|----------|
| | | | 3733 | 4266 | |
| Core Parameters | | | | | |
| RL-A | READ latency (DBI disabled) | Min | 32 | 36 | tCK(avg) |
| RL-B | READ latency (DBI enabled) | Min | 36 | 40 | tCK(avg) |
| WL-A | WRITE latency (Set A) | Min | 16 | 18 | tCK(avg) |
| WL-B | WRITE latency (Set B) | Min | 30 | 34 | tCK(avg) |
| tRC | ACTIVATE-to-ACTIVATE command period | Min | tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge) | | ns |
| tSR | Minimum self refresh time (entry to exit) | Min | MAX(15ns, 3nCK) | | ns |
| tXSR | Self refresh exit to next valid command delay | Min | MAX(tRFCab + 7.5ns, 2nCK) | | ns |
| tCCD | CAS-to-CAS delay | Min | 8 | | tCK(avg) |
| tCCDMW | CAS-to-CAS delay masked write | Min | 32 | | tCK(avg) |
| tRTP | Internal READ to PRECHARGE command delay | Min | Max (7.5ns, 8nCK) | | ns |
| tRCD | RAS-to-CAS delay | Min | Max (18ns, 4nCK) | | ns |
| tRPpb | Row precharge time (single bank) | Min | Max (18ns, 4nCK) | | ns |
| tRPpab | Row precharge time (all banks) | Min | Max (21ns, 4nCK) | | ns |
| tRAS | Row active time | Min | Max (42ns, 3nCK) | | ns |
| | | Max | MIN(9 × tREFI × Refresh Rate, 70.2) | | us |
| tWR | WRITE recovery time | Min | Max (18ns, 6nCK) | | ns |
| tWTR | WRITE-to- READ command delay | Min | Max (10ns, 8nCK) | | ns |
| tRRD | Active bank A to active bank B | Min | Max (10ns, 4nCK) | Max (7.5ns, 4nCK) | ns |
| tPPD | Precharge-to-precharge delay | Min | 4 | | tCK(avg) |
| tFAW | Four-bank activate window | Min | 40 | 30 | ns |
| tESCKE | Delay from SRE command to CKE input LOW | Min | MAX(1.75ns, 3nCK) | | - |

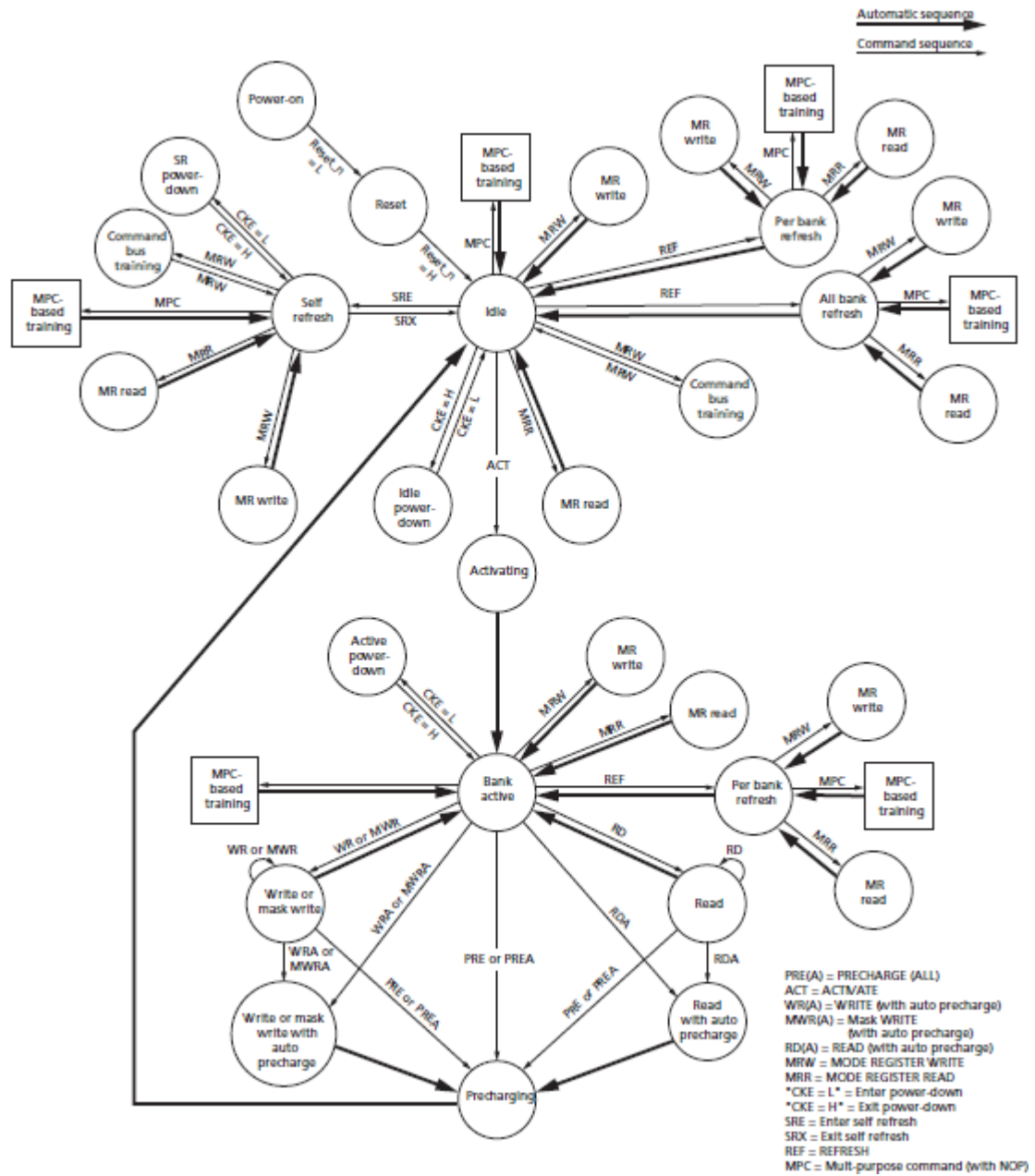
AC Characteristics (Continued)

(V_{DD2} , V_{DDQ} , V_{DDCA} = 1.06~1.17V, V_{DD1} = 1.70~1.95V)

| Symbol | Parameter | Min/Max | Data Rate | | Unit |
|-----------------------------------|---|---------|------------------|------|------|
| | | | 3733 | 4266 | |
| CA Bus Training Parameters | | | | | |
| tCKELCK | Valid clock requirement after CKE Input LOW | Min | MAX(5ns, 5nCK) | | tCK |
| tDStrain | Data setup for VREF training mode | Min | 2 | | ns |
| tDHtrain | Data hold for VREF training mode | Min | 2 | | ns |
| tADR | Asynchronous data ready | Max | 20 | | ns |
| tCACD | CA BUS TRAINING command- to-command delay | Min | RU(tADR/tCK) | | tCK |
| tDQSCKE | Valid strobe requirement before CKE LOW | Max | 10 | | ns |
| tCAENT | First CA BUS TRAINING command following CKE LOW | Min | 250 | | ns |
| tVREFca_LONG | VREF step time – multiple steps | Max | 250 | | ns |
| tVREFca_SHORT | VREF step time – one step | Max | 80 | | ns |
| tCKPRECS | Valid clock requirement before CS HIGH | Min | 2tCK + tXP | | - |
| tCKPSTCS | Valid clock requirement after CS HIGH | Min | MAX(7.5ns, 5nCK) | | - |
| tCS_VREF | Minimum delay from CS to DQS toggle in command bus training | Min | 2 | | tCK |
| tCKEHDQS | Minimum delay from CKE HIGH to strobe High-Z | Min | 10 | | ns |
| tMRZ | CA bus training CKE HIGH to DQ tri-state | Min | 1.5 | | ns |
| tCKELODton | ODT turn-on latency from CKE | Min | 20 | | ns |
| tCKEHODTof | ODT turn-off latency from CKE | Min | 20 | | ns |
| tXCBT_Short | Exit command bus training mode to next valid command delay | Min | MAX(200ns, 5nCK) | | - |
| tXCBT_Middle | | Min | MAX(200ns, 5nCK) | | - |
| tXCBT_Long | | Min | MAX(250ns, 5nCK) | | - |

| Write Voltage and Timing | | | | | |
|--|--|-----|---|------|----------|
| TdIVW_total | Rx timing window total at VdIVW voltage levels | Max | 0.25 | 0.25 | UI |
| TdIVW_1-bit | Rx timing window 1-bit toggle (at VdIVW voltage levels) | Max | TBD | | UI |
| TdIPW | DQ and DMI input pulse width (at VCENT_DQ) | Min | 0.45 | | UI |
| tDQS2DQ | DQ-to-DQS offset | Min | 200 | | ps |
| | | Max | 800 | | |
| tDQDQ | DQ-to-DQ offset | Max | 30 | | ps |
| tDQS2DQ_tem | DQ-to-DQS offset temperature variation | Max | 0.6 | | ps/°C |
| tDQS2DQ_volt | DQ-to-DQS offset voltage variation | Max | 33 | | ps/50mV |
| tDQSS | WRITE command to first DQS transition | Min | 0.75 | | tCK(avg) |
| | | Max | 1.25 | | |
| tDQSH | DQS input HIGH-level width | - | 0.4 | | tCK(avg) |
| tDQSL | DQS input LOW-level width | Min | 0.4 | | tCK(avg) |
| tDSS | DQS falling edge to CK setup time | Min | 0.2 | | tCK(avg) |
| tDSH | DQS falling edge from CK hold time | Min | 0.2 | | tCK(avg) |
| tWPST | Write postamble | Min | 0.4 (or 1.4 if extra postamble is programmed in MR) | | tCK(avg) |
| tWPRE | Write preamble | Min | 1.8 | | tCK(avg) |
| Temperature Derating Parameters | | | | | |
| tDQCKd | DQS output access time from CK_t/CK_c (derated) | Max | 3600 | | ps |
| tRCDd | RAS-to-CAS delay (derated) | Min | tRCD + 1.875 | | ns |
| tRCd | ACTIVATE-to-ACTIVATE command period (same bank, derated) | Min | tRC + 3.75 | | ns |
| tRASd | Row active time (derated) | Min | tRAS + 1.875 | | ns |
| tRPd | Row precharge time (derated) | Min | tRP + 1.875 | | ns |
| tRRD | Active bank A to active bank B (derated) | Min | tRRD + 1.875 | | ns |

Simplified State Diagram



Command Truth Table

Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data.

| SDRAM Command | SDR Command Pins | SDR CA Pins (6) | | | | | | CK_t edge | Notes |
|--|------------------|-----------------|-----|-----|-----|-----|-----|-----------|-------------|
| | CS | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| Deselect (DES) | L | X | | | | | | R1 | 1,2 |
| Multi-Purpose Command (MPC) | H | L | L | L | L | L | OP6 | R1 | 1,9 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |
| Precharge (PRE) (Per Bank, All Bank) | H | L | L | L | L | H | AB | R1 | 1,2,3,4 |
| | L | BA0 | BA1 | BA2 | V | V | V | R2 | |
| Refresh (REF) (Per Bank, All Bank) | H | L | L | L | H | L | AB | R1 | 1,2,3,4 |
| | L | BA0 | BA1 | BA2 | V | V | V | R2 | |
| Self Refresh Entry (SRE) | H | L | L | L | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Write -1 (WR-1) | H | L | L | H | L | L | BL | R1 | 1,2,3,6,7,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| Self Refresh Exit (SRX) | H | L | L | H | L | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Mask Write -1 (MWR-1) | H | L | L | H | H | L | L | R1 | 1,2,3,5,6,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| RFU | H | L | L | H | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Read -1 (RD-1) | H | L | H | L | L | L | BL | R1 | 1,2,3,6,7,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| CAS-2 (Write-2, Mask Write -2, Read-2, MRR-2, MPC) | H | L | H | L | L | H | C8 | R1 | 1,8,9 |
| | L | C2 | C3 | C4 | C5 | C6 | C7 | R2 | |
| RFU | H | L | H | L | H | L | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| RFU | H | L | H | L | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Mode Register Write-1 (MRW-1) | H | L | H | H | L | L | OP7 | R1 | 1,11 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | R2 | |
| Mode Register Write-2 (MRW-2) | H | L | H | H | L | H | OP6 | R1 | 1,11 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |
| Mode Register Read-1 (MRR-1) | H | L | H | H | H | L | V | R1 | 1,2,12 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | R2 | |
| RFU | H | L | H | H | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Activate-1 (ACT-1) | H | H | L | R12 | R13 | X | X | R1 | 1,2,3,10 |
| | L | BA0 | BA1 | BA2 | X | R10 | R11 | R2 | |
| Activate-2 (ACT-2) | H | H | H | R6 | R7 | R8 | R9 | R1 | 1,10 |
| | L | R0 | R1 | R2 | R3 | R4 | R5 | R2 | |

- Note 1:** All commands except for DESELECT are two clock cycles and are defined by the current state of CS and CA[5:0] at the rising edge of the clock. DESELECT command is one clock cycle and is not latched by the device.
- Note 2:** V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, and CA[5:0] can be floated.
- Note 3:** Bank addresses BA[2:0] determine which bank is to be operated upon.
- Note 4:** AB HIGH during PRECHARGE or REFRESH commands indicate the command must be applied to all banks, and the bank addresses are "Don't Care."
- Note 5:** MASK WRITE-1 command only supports BL16. For MASK WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).
- Note 6:** AP HIGH during a WRITE-1, MASK WRITE-1, or READ-1 command indicates that an auto precharge will occur to the bank the command is operating on. AP LOW indicates that no auto precharge will occur and the bank will remain open upon completion of the command.
- Note 7:** When enabled in the mode register, BL HIGH during a WRITE-1, MASK-WRITE-1, or READ-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOW during one of these commands indicates the burst length should be set on-the-fly to BL = 16. If on-the-fly burst length is not enabled in the mode register, this bit should be driven to a valid level and is ignored by the device.
- Note 8:** For CAS-2 commands (WRITE-2, MASK WRITE-2, READ-2, MRR-2, or MPC (only write FIFO, read FIFO and read DQ calibration), C[1:0] are not transmitted on the CA [5:0] bus and are assumed to be zero. Note that for CAS-2 WRITE-2 or CAS-2 MASK WRITE-2 command, C[3:2] must be driven LOW.
- Note 9:** WRITE-1, MASK-WRITE-1, READ-1, MODE REGISTER READ-1, or MPC (only write FIFO, read FIFO, and read DQ calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. WRITE-1, MASK WRITE-1, READ-1, MRR-1, or MPC (only write FIFO, read FIFO, and read DQ calibration) command must be issued first before issuing CAS-2 command. MPC (only Start and Stop DQS Oscillator, Start and Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
- Note 10:** The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutively without any other command between them. The ACTIVATE-1 command must be issued prior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
- Note 11:** The MRW-1 command must be followed by the MRW-2 command consecutively without any other command between them. The MRW-1 command must be issued prior to the MRW-2 command.
- Note 12:** The MRR-1 command must be followed by the CAS-2 command consecutively without any other commands between them. The MRR-1 command must be issued prior to the CAS-2 command.

IDD Measurement Conditions

Definition of Switching for CA Input Signals

| CK_t edge | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 |
|-----------|----|----|----|----|----|----|----|----|
| CKE | H | H | H | H | H | H | H | H |
| CS | L | L | L | L | L | L | L | L |
| CA0 | H | L | L | L | L | H | H | H |
| CA1 | H | H | H | L | L | L | L | H |
| CA2 | H | L | L | L | L | H | H | H |
| CA3 | H | H | H | L | L | L | L | H |
| CA4 | H | L | L | L | L | H | H | H |
| CA5 | H | H | H | L | L | L | L | H |

Notes 1: LOW = $V_{IN} \leq V_{IL(DC) MAX}$, HIGH = $V_{IN} \geq V_{IH(DC) MIN}$, STABLE = Inputs are stable at a HIGH or LOW level

Notes 2: CS must always be driven LOW.

Notes 3: 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

Notes 4: The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

CA Pattern for IDD4R for BL=16

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | H | H | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

Notes 1: BA[2:0] = 010; CA[9:4] = 000000 OR 111111; Burst order CA[3:2] = 00 or 11.

Notes 2: CA pins are kept LOW with DES CMD to reduce ODT current.

CA Pattern for IDD4W for BL=16

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | L | L | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

Notes 1: BA[2:0] = 010; CA[9:4] = 000000 or 111111

Notes 2: No burst ordering

Notes 3: CA pins are kept LOW with DES CMD to reduce ODT current

Data Pattern for IDD4W(DBI off) for BL=16

| DBI Off Case | | | | | | | | | | |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 | DBI | # of 1s |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

| | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|---|---|
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

Notes 1: Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming.

Data Pattern for IDD4R(DBI off) for BL=16

| DBI Off Case | | | | | | | | | | |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 | DBI | # of 1s |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

| | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|---|---|
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| # of 1s | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

Notes 1: Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming.

Data Pattern for IDD4W(DBI On) for BL=16

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |

Notes 1: DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, and BL28.

Data Pattern for IDD4R(DBI On) for BL=16

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| # of 1s | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |

Notes 1: DBI enabled burst: BL0, BL6, BL8, BL14, BL20, BL26, and BL30.

CA Pattern for IDD4R for BL = 32

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | READ-1 | L | H | L | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+9 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+10 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+11 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+16 | HIGH | HIGH | READ-1 | L | H | L | L | L | L |
| N+17 | HIGH | LOW | | L | H | L | L | H | L |
| N+18 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+19 | HIGH | LOW | | H | H | L | H | H | H |
| N+20 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+21 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+22 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+23 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+24 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+25 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+26 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+27 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+28 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+29 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+30 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+31 | HIGH | LOW | DES | L | L | L | L | L | L |

Notes 1: BA[2:0] = 010, C[9:5] = 00000 or 11111, Burst order C[4:2] = 000 or 111.

CA Pattern for IDD4W for BL = 32

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | WRITE-1 | L | L | H | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+9 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+10 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+11 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+16 | HIGH | HIGH | WRITE-1 | L | L | H | L | L | L |
| N+17 | HIGH | LOW | | L | H | L | L | H | L |
| N+18 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+19 | HIGH | LOW | | L | L | L | H | H | H |
| N+20 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+21 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+22 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+23 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+24 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+25 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+26 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+27 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+28 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+29 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+30 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+31 | HIGH | LOW | DES | L | L | L | L | L | L |

Notes 1: BA[2:0] = 010, C[9:5] = 00000 or 11111.

Data Pattern for IDD4W (DBI Off) for BL = 32

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL32 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL33 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL35 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |

Data Pattern for IDD4W (DBI Off) for BL = 32(continue)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL37 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL38 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL39 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL40 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL41 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL43 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL45 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL46 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL47 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL48 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL53 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL54 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL55 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL61 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL63 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | | |

Notes 1: Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming

Data Pattern for IDD4R (DBI Off) for BL = 32

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

Data Pattern for IDD4R (DBI Off) for BL = 32(Continue)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL32 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL33 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL34 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL35 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL36 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL37 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL38 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Data Pattern for IDD4R (DBI Off) for BL = 32(Continue)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL39 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL40 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL41 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL42 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL43 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL44 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL45 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL46 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL47 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL48 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL53 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL54 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL55 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL61 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL62 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL63 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| # of 1s | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | | |

Notes 1: Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W/R pattern programming.

Data Pattern for IDD4W (DBI On) for BL = 32

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |

Data Pattern for IDD4W (DBI On) for BL = 32(Continue)

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL32 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL33 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL35 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL37 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL38 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL39 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL40 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

Data Pattern for IDD4W (DBI On) for BL = 32(Continue)

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL41 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL43 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL45 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL46 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL47 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL48 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL53 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL54 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL55 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL61 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL63 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 16 | 16 | 16 | 16 | 16 | 16 | 32 | 32 | 16 | |

Notes 1: DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL32, BL38, BL40, BL46, BL48, BL54, BL58, and BL60.

Data Pattern for IDD4R (DBI On) for BL = 32

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |

Data Pattern for IDD4R (DBI On) for BL = 32(continue)

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL32 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL33 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL35 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL37 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL38 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL39 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL40 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL41 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |

Data Pattern for IDD4R (DBI On) for BL = 32(continue)

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL43 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL45 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL46 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL47 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL48 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL53 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL54 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL55 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL61 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL62 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL63 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| # of 1s | 16 | 16 | 16 | 16 | 16 | 16 | 32 | 32 | 16 | |

Notes 1: DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL34, BL36, BL42, BL44, BL48, BL52, BL58, and BL62.

Power-up, initialization

To ensure proper functionality for power-up and reset initialization, default values for the MR settings are provided in the table below.

| Item | Mode Register Setting | Default Setting | Description |
|------------------------------|-----------------------|-----------------|--|
| FSP-OP/WR | MR13 OP[7:6] | 00b | FSP-OP/WR[0] are enabled |
| WLS | MR2 OP[6] | 0b | WRITE latency set A is selected |
| WL | MR2 OP[5:3] | 000b | WL = 4 |
| RL | MR2 OP[2:0] | 000b | RL = 6, nRTP = 8 |
| nWR | MR1 OP[6:4] | 000b | nWR = 6 |
| DBI-WR/RD | MR3 OP[7:6] | 00b | Write and read DBI are disabled |
| CA ODT | MR11 OP[6:4] | 000b | CA ODT is disabled |
| DQ ODT | MR11 OP[2:0] | 000b | DQ ODT is disabled |
| V _{REF(CA)} setting | MR12 OP[6] | 1b | V _{REF(CA)} range[1] is enabled |
| V _{REF(CA)} value | MR12 OP[5:0] | 001101b | Range1: 27.2% of V _{DD2} |
| V _{REF(DQ)} setting | MR14 OP[6] | 1b | V _{REF(DQ)} range[1] enabled |
| V _{REF(DQ)} value | MR14 OP[5:0] | 001101b | Range1: 27.2% of V _{DDQ} |

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

Voltage Ramp

1. While applying power (after T_a), RESET_n should be held LOW ($\leq 0.2 \times VDD2$), and all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the table below. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

| After | Applicable Conditions |
|---------------|--|
| Ta is reached | VDD1 must be greater than VDD2 |
| | VDD2 must be greater than VDDQ - 200mV |

Notes 1: T_a is the point when any power supply first reaches 300mV.

Notes 2: Noted conditions apply between T_a and power-down (controlled or uncontrolled).

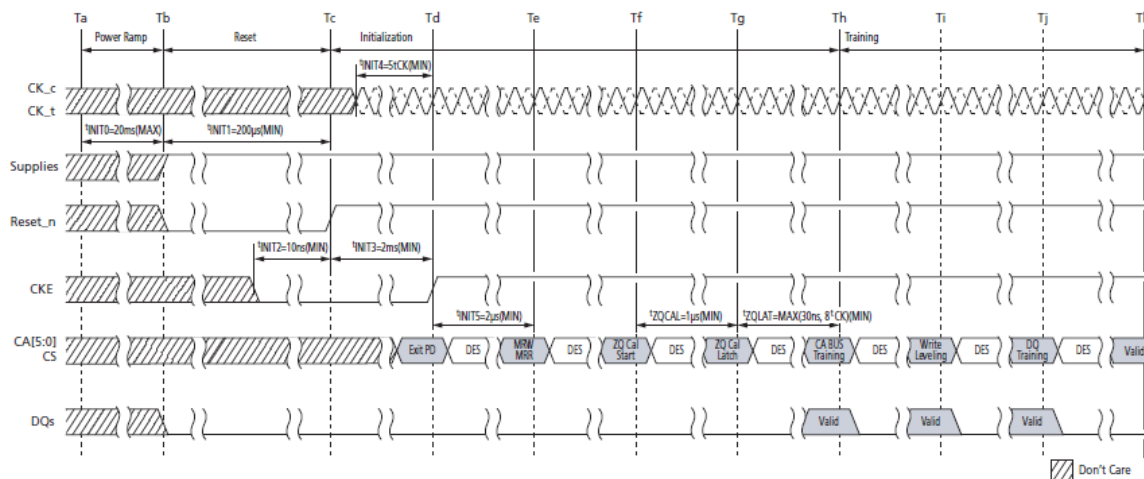
Notes 3: T_b is the point at which all supply and reference voltages are within their defined operating ranges.

Notes 4: Power ramp duration t_{INIT0} ($T_b - T_a$) must not exceed 20ms.

Notes 5: The voltage difference between any VSS and VSSQ must not exceed 100mV

2. Following completion of the of the voltage ramp (T_b), RESET_n must be held LOW for t_{INIT1} . DQ, DMI, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at T_b , RESET_n must remain LOW for at least t_{INIT1} (T_c), after which RESET_n can be de-asserted to HIGH (T_c). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care."



Notes 1: Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

- After RESET_n is de-asserted (T_c), wait at least t_{INIT3} before activating CKE. CK_t, CK_c must be started and stabilized for t_{INIT4} before CKE goes active (T_d). CS must remain LOW when the controller activates CKE.
- After CKE is set to HIGH, wait a minimum of t_{INIT5} to issue any MRR or MRW commands (T_e). For MRR and MRW commands, the clock frequency must be within the range defined for tCK_b . Some AC parameters (for example, $tDQSCK$) could have relaxed timings (such as $tDQSCK_b$) before the system is appropriately configured.
- After completing all MRW commands to set the pull-up, pull-down, and Rx termination values, the controller can issue the ZQCAL START command to the memory (T_f). This command is used to calibrate the VOH level and the output impedance over process, voltage, and temperature. In systems where more than one device share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each device. The ZQ calibration sequence is completed after $tZQCAL$ (T_g). The ZQCAL LATCH command must be issued to update the DQ drivers and DQ + CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th), the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (command bus training mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The device will power-up with receivers configured for low-speed operations and with VREF(CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training is complete. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and it outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.
8. After command bus training, the controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is HIGH(Ti). See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the controller adjusts write DQS timing to the point where the device recognizes the start of write DQ data burst with desired WRITE latency.
9. After write leveling, the DQ bus (internal VREF(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC TRAINING commands and by issuing MRW commands to adjust VREF(DQ). The device will power-up with receivers configured for low-speed operations and with VREF(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ bus training is complete. The MPC[READ DQ CALIBRATION] command is used together with MPC[READ-FIFO] or MPC[WRITE-FIFO] commands to train the DQ bus without disturbing the memory array contents.
10. At Tk, the device is ready for normal operation and is ready to accept any valid command. Any mode registers that have not previously been configured for normal operation should be written at this time.

Mode Registers

Mode Register Assignment and Definition

The table listed below shows the mode registers for LPDDR4 SDRAM. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Mode Register Assignments(continued)

| MR# | OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----|---|----------------|----------|---------|---------------|--------------|---------|----------|
| 0 | CATR | RFU | RFU | RZQI | | RFU | Latency | Refresh |
| 1 | RPST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | |
| 2 | WR Lev | WLS | WL | | | RL | | |
| 3 | DBI-WR | DBI-RD | PDDS | | | PPRP | WR PST | PU-CAL |
| 4 | TUF | Thermal Offset | | PPRE | SR Abort | Refresh Rate | | |
| 5 | LPDDR4 Manufacturer ID | | | | | | | |
| 6 | Revision ID-1 | | | | | | | |
| 7 | Revision ID-2 | | | | | | | |
| 8 | IO Width | | Density | | | Type | | |
| 9 | Vendor Specific Test Register | | | | | | | |
| 10 | RFU | | | | | | | ZQ-Reset |
| 11 | RFU | CA ODT | | | RFU | DQ ODT | | |
| 12 | RFU | VR-CA | VREF(CA) | | | | | |
| 13 | FSP-OP | FSP-WR | DMD | RRO | VRCG | VRO | RPT | CBT |
| 14 | RFU | VR(dq) | VREF(DQ) | | | | | |
| 15 | Lower-Byte Invert Register for Calibration | | | | | | | |
| 16 | PASR Bank Mask | | | | | | | |
| 17 | PASR Segment Mask | | | | | | | |
| 18 | DQS Oscillator Count - LSB | | | | | | | |
| 19 | DQS Oscillator Count - MSB | | | | | | | |
| 20 | Upper-Byte Invert Register for DQ Calibration | | | | | | | |
| 21 | RFU | | | | | | | |
| 22 | RFU | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT | | | |
| 23 | DQS interval timer run time setting | | | | | | | |
| 24 | TRR Mode | TRR Mode BAn | | | Unlimited MAC | MAC Value | | |
| 25 | PPR Resource | | | | | | | |
| 26 | RFU | | | | | | | |
| 27 | RFU | | | | | | | |
| 28 | RFU | | | | | | | |
| 29 | RFU | | | | | | | |
| 30 | Reserved for testing – SDRAM will ignore | | | | | | | |
| 31 | RFU | | | | | | | |
| 32 | DQ Calibration Pattern "A" (default = 5A _H) | | | | | | | |
| 33 | RFU | | | | | | | |
| 34 | RFU | | | | | | | |
| 35 | RFU | | | | | | | |
| 36 | RFU | | | | | | | |
| 37 | RFU | | | | | | | |
| 38 | RFU | | | | | | | |
| 39 | Reserved for testing – SDRAM will ignore | | | | | | | |
| 40 | DQ Calibration Pattern "B" (default = 3C _H) | | | | | | | |

MR0 Device Feature 0 (MA[5:0] = 00h)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|-------|-------|-------|-------|--------------|--------------|
| CATR | RFU | RFU | RZQI | | RFU | Latency Mode | Refresh Mode |

| Function | Type | Operand | Data | Notes |
|--------------------------------------|-----------|---------|---|------------|
| Refresh Mode | Read-only | OP[0] | 0b: Both legacy and modified refresh mode supported (default) 1b: Only modified refresh mode supported | |
| Latency Mode | | OP[1] | 0b: Device supports normal latency 1b: Reserved | 6 |
| RZQI (Built-in Self-Test for RZQ) | | OP[4:3] | 00b: RZQ Self-Test not support. 01b: ZQ-pin may connect to VSSQ or float 10b: ZQ-pin may short to VDDQ 11b: ZQ-pin Self-Test completed, no error condition detected (ZQ-pin may not connect to VSSQ or float ,nor short to VDDQ) | 1, 2, 3, 4 |
| CATR (CA Terminating Rank) | | OP[7] | 0b: CA for this rank is not terminated 1b: CA for this rank is terminated | 5 |

Notes 1: RZQI MR value, if supported, will be valid after the following sequence:

- Completion of MPC[ZQCAL START] command to either channel
- Completion of MPC[ZQCAL LATCH] command to either channel then tZQLAT is satisfied
RZQI value will be lost after reset

Notes 2: If ZQ is connected to VSSQ to set default calibration, OP[4:3] must be set to 01b. If ZQ is not connected to VSSQ, either OP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assembly error. It is recommended that the assembly error be corrected..

Notes 3: In the case of possible assembly error, the device will default to factory trim settings for RON, and will ignore ZQ CALIBRATION commands. In either case, the device may not function as intended.

Notes 4: If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor meets the specified limits (that is, 240Ω ±1%).

Notes 5: CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated.

Notes 6: Byte mode is not supported.

MR1 Device Feature 1 (MA[5:0] = 01h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------------|-----|-----|--------|--------|-----|-----|
| RD-PST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | |

MR1 Op-Code Bit Definitions

| Feature | Type | OP | Definition | Notes |
|---------------------------------|------------|---------|---|---------|
| BL Burst length | Write-only | OP[1:0] | 00b: BL = 16 sequential (default) 01b: BL = 32 sequential 10b: BL = 16 or 32 sequential (on-the-fly) 11b: Reserved | 1 |
| WR-PRE Write preamble length | Write-only | OP[2] | 0b: Reserved 1b: WR preamble = $2 \times t_{CK}$ | 5, 6 |
| RD-PRE Read preamble type | Write-only | OP[3] | 0b: RD preamble = Static (default) 1b: RD preamble = Toggle | 3, 5, 6 |

| Feature | Type | OP | Definition | Notes |
|---|------------|---------|---|---------|
| nWR Write-recovery for AUTO PRECHARGE command | Write-only | OP[6:4] | 000b: nWR = 6 (default) 001b: nWR = 10 010b: nWR = 16 011b: nWR = 20 100b: nWR = 24 101b: nWR = 30 110b: nWR = 34 111b: nWR = 40 | 2, 5, 6 |
| RD-PST Read postamble length | Write-only | OP[7] | 0b: RD postamble = $0.5 \times t_{CK}$ (default) 1b: RD postamble = $1.5 \times t_{CK}$ | 4, 5, 6 |

Notes 1: Burst length on-the-fly can be set to either BL = 16 or BL = 32 by setting the BL bit in the command operands. See the Command Truth Table.

Notes 2: The programmed value of nWR is the number of clock cycles the device uses to determine the starting point of an internal precharge after a write burst with auto precharge (AP) enabled.

Notes 3: For READ operations, this bit must be set to select between a toggling preamble and a non-toggling preamble.

Notes 4: OP[7] provides an optional read postamble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.

Notes 5: There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.

Notes 6: There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

MR2 MR2 Device Feature (MA[5:0] = 02Ch)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|-----|-----|-----|-----|-----|-----|-----|
| WR Lev | WLS | | WL | | | RL | |

MR2 Op-Code Bit Definitions

| Feature | Type | OP | Definition | Notes |
|--------------------------|------------|---------|---|---------|
| RL READ latency | Write-only | OP[2:0] | RL and nRTP for DBI-RD disabled (MR3 OP[6] = 0b) 000b: RL = 6, nRTP = 8 (default) 001b: RL = 10, nRTP = 8 010b: RL = 14, nRTP = 8 011b: RL = 20, nRTP = 8 100b: RL = 24, nRTP = 10 101b: RL = 28, nRTP = 12 110b: RL = 32, nRTP = 14 111b: RL = 36, nRTP = 16 <hr/> RL and nRTP for DBI-RD enabled (MR3 OP[6] = 1b) 000b: RL = 6, nRTP = 8 001b: RL = 12, nRTP = 8 010b: RL = 16, nRTP = 8 011b: RL = 22, nRTP = 8 100b: RL = 28, nRTP = 10 101b: RL = 32, nRTP = 12 110b: RL = 36, nRTP = 14 111b: RL = 40, nRTP = 16 | 1, 3, 4 |
| WL WRITE latency | Write-only | OP[5:3] | WL set A (MR2 OP[6] = 0b) 000b: WL = 4 (default) 001b: WL = 6 010b: WL = 8 011b: WL = 10 100b: WL = 12 101b: WL = 14 110b: WL = 16 111b: WL = 18 <hr/> WL set B (MR2 OP[6] = 1b) 000b: WL = 4 001b: WL = 8 010b: WL = 12 011b: WL = 18 100b: WL = 22 101b: WL = 26 110b: WL = 30 111b: WL = 34 | 1, 3, 4 |
| WLS WRITE latency set | Write-only | OP[6] | 0b: Use WL set A (default) 1b: Use WL set B | 1, 3, 4 |
| WR Lev Write leveling | Write-only | OP[7] | 0b: Disable write leveling (default) 1b: Enable write leveling | 2 |

Notes 1: See Latency Code Frequency Table for allowable Frequency Ranges for RL/WL/nWR/nRTP.

Notes 2: After an MRW command to set the write leveling enable bit (OP[7] = 1b), the device remains in the MRW state until another MRW command clears the bit (OP[7] = 0b). No other commands are allowed until the write leveling enable bit is cleared.

Notes 3: There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address, or read from with an MRR command to this address.

Notes 4: There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Mode Register 14 (MA[5:0] = 0Eh)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|------------------|----------------------|-------|-------|-------|-------|-------|
| RFU | VR _{DQ} | V _{REF(DQ)} | | | | | |

MR14 Op-Code Bit Definition

| Feature | Type | OP | Definition | Notes |
|--|----------------|---------|--|-----------|
| V _{REF(DQ)} V _{REF(DQ)} setting | Read/ Write | OP[5:0] | 000000b–110010b: See V _{REF} Settings table All others: Reserved | 1–3, 5, 6 |
| VR _{DQ} V _{REF(DQ)} range | | OP[6] | 0b: V _{REF(DQ)} range[0] enabled 1b: V _{REF(DQ)} range[1] enabled (default) | 1, 2, 4–6 |

Notes 1: This register controls the VREF(DQ) levels for frequency set point[1:0]. Values from either VRDQ [vendor defined] or VRDQ [vendor defined] may be selected by setting OP[6] appropriately.

Notes 2: A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ will be set to 0.

Notes 3: write to OP[5:0] sets the internal VREF(DQ) level for FSP[0] when MR13 OP[6] = 0b, or sets FSP[1] when MR13 OP[6] = 1b. The time required for VREF(DQ) to reach the set level depends on the step size from the current level to the new level.

Notes 4: A write to OP[6] switches the device between two internal VREF(DQ) ranges. The range (range[0] or range[1]) must be selected when setting the VREF(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or reset event.

Notes 5: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

Notes 6: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, for example, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR22 Register Information (MA[5:0] = 16h)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|---------|---------|---------|---------|-------|-------|
| RFU | | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT | | |

MR22 Register Information

| Function | Type | Operand | Data | Notes |
|---|------------|---------|---|---------------|
| SoC ODT (Controller ODT Value for VOH calibration) | Write-only | OP[2:0] | 000_b : Disable (Default) 001_b : RZQ/1 010_b : RZQ/2 011_b : RZQ/3 100_b : RZQ/4 101_b : RZQ/5 110_b : RZQ/6 111_b : Reserved | 1, 2, 3 |
| ODTE-CK (CK ODT enabled for nonterminating rank) | | OP[3] | 0_b : ODT-CK Over-ride Disabled (Default) 1_b : ODT-CK Over-ride Enabled | 2, 3, 4, 6, 8 |
| ODTE-CS (CS ODT enable for nonterminating rank) | | OP[4] | 0_b : ODT-CS Over-ride Disabled (Default) 1_b : ODT-CS Over-ride Enabled | 2, 3, 5, 6, 8 |
| ODTD-CA (CA ODT termination disable) | | OP[5] | 0_b : ODT-CA Obeyes ODT_CA bond pad (default) 1_b : ODT-CA Disabled | 2, 3, 6, 7, 8 |

Notes 1: All values are typical.

Notes 2: There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command or read from with an MRR command to this address.

Notes 3: There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Notes 4: When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.

Notes 5: When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.

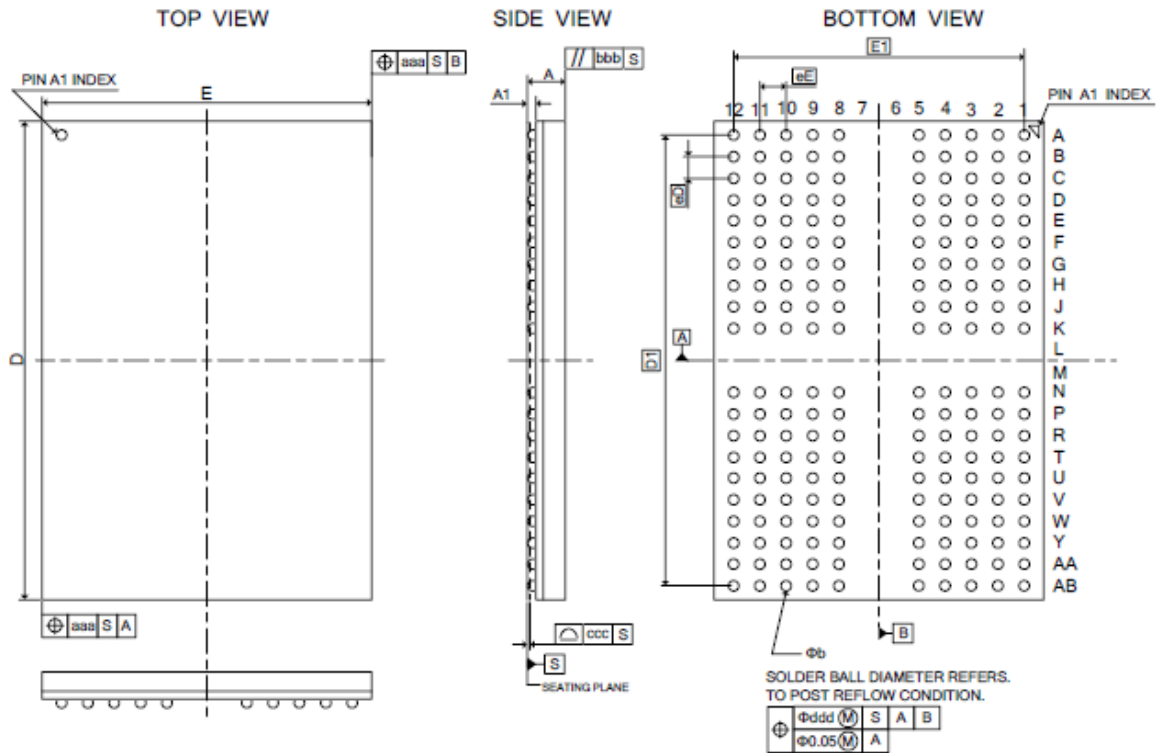
Notes 6: For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.

Notes 7: When OP[5]=0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT_CA bond pad or MR11-OP[6:4].

Notes 8: To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or ODT_CA pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self Refresh, Self Refresh Power-down, Active Power-down and Precharge Power-down.

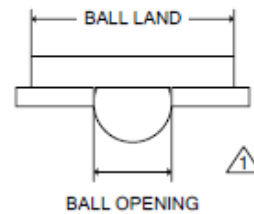
Package Description

200-ball FBGA 10x14.5mm



Controlling Dimension:
Millimeters

| SYMBOL | DIMENSION (MM) | | | DIMENSION (Inch) | | |
|--------|----------------|-------|-------|------------------|-------|--------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.60 | 0.70 | 0.80 | 0.021 | 0.026 | 0.031 |
| A1 | 0.177 | 0.227 | 0.277 | 0.007 | 0.009 | 0.011 |
| b | 0.313 | 0.363 | 0.413 | 0.012 | 0.014 | 0.016 |
| D | 14.40 | 14.50 | 14.60 | 0.566 | 0.570 | 0.574 |
| E | 9.90 | 10.00 | 10.10 | 0.389 | 0.393 | 0.397 |
| D1 | 13.65 BSC. | | | 0.537 BSC. | | |
| E1 | 8.80 BSC. | | | 0.346 BSC. | | |
| eD | 0.65 BSC. | | | 0.025 BSC. | | |
| eE | 0.80 BSC. | | | 0.031 BSC. | | |
| aaa | 0.15 BSC. | | | 0.0059 BSC. | | |
| bbb | --- | --- | 0.10 | --- | --- | 0.0039 |
| ccc | --- | --- | 0.10 | --- | --- | 0.0039 |
| ddd | --- | --- | 0.15 | --- | --- | 0.0059 |



Note:
1. Ball land: 0.41mm, Ball opening: 0.35mm

Revision History

| Revision No. | History | Draft Date | Editor | Remark |
|--------------|----------------------|------------|-----------|--------|
| 0.1 | Initial Release. | Dec. 2023 | Rico Yang | N/A |
| 1.0 | First SPEC. release. | May.. 2024 | Rico Yang | N/A |