16Gb (1Gb×16) DDR5 SDRAM

Descriptions

The 16Gb DDR5 SDRAM is organized as a 64Mbit x16 I/Os x 16banks device. This synchronous device achieves high speed double- data-rate transfer rates of up to 5600Mb/sec/pin (DDR5-5600) for general applications.

The chip is designed to comply with the following key DDR5 SDRAM features

such as posted CAS, Programmable CWL, Internal Calibration via MPC, On Die Termination via Mode Register setting and Asynchronous Reset.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion.

The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. The DDR5 device operates with 1.1V (1.067V~1.166V) and 1.8V (1.746V~1.908V) power supply.

The 16Gb DDR5 device is available in 106ball FBGAs(x16).

Features

- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%)).
- VPP = 1.8V(1.746V(-3%) ~ 1.908V(+6%)).
- Package : x16-16Banks(4 Bank Groups).
- JEDEC standard compliant.
- Programmable CAS Write Latency (CWL) = RL-2.
- 16-bit pre-fetch.
- Burst Length: 16 by default. 8 with tCCD=8, which does not allow. gapless READ or WRITE, where BC8 and BL32 refer to CA5BL*=L.
- Bi-directional Differential Data-Strobe.
- 2N mode
- On Die Termination (ODT) via Mode Register setting
- Average Refresh period 3.9us at lower than TCASE 85°C, 1.95us at 85°C < TCASE < 95 °C.
- Connectivity Test Mode (TEN) is supported.
- Asynchronous Reset.
- Package: 106 balls FBGA - x16.
- All of Lead-Free products are compliant for RoHS.
- All of products are Halogen-free.
- POD (Pseudo Open Drain) interface for data input/output,command and address input.
- sPPR and hPPR capability
- External VPP for DRAM activating power.
- JRefresh Management(RFM) is not required.
- CAI (Command Address Inversion).
- On-Die ECC is supported with ECC Transparency and ErrorCheck and Scrub(ECS).
- Command Address Inversion(CAI).

Ordering Information

Part No	Organization	Data Rate	Package	Grade
H2AD16G16F6SSAPC	1024M X 16	DDR5-4800 40-39-39	106 Ball BGA, 10x14.1mm	Commercial
H2AD16G16F6STAPC	1024M X 16	DDR5-5600 46-45-45	106 Ball BGA, 10x14.1mm	Commercial
H2AD16G16F6SSAPI	1024M X 16	DDR5-4800 40-39-39	106 Ball BGA, 10x14.1mm	Industrial
H2AD16G16F6STAPI	1024M X 16	DDR5-5600 46-45-45	106 Ball BGA, 10x14.1mm	Industrial

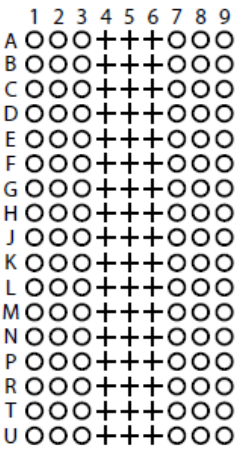
Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

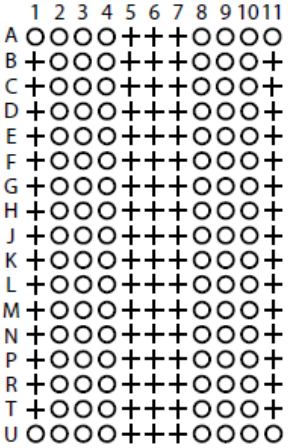
106-Ball FBGA – x16

AU	1	2	3	4	5	6	7	8	9	10	11
AT		1	2	3	4	5	6	7	8	9	
A	NC	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	NC
B		VDD	VDDQ	DQU2				DQU3	VDDQ	VDD	
C		VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS	
D		VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ	
E		VDD	DQU4	DQU6				DQU7	DQU5	VDD	
F		VDD	VDDQ	DQL2				DQL3	VDDQ	VDD	
G		VSS	DQL0	DQSL_t				DML_n	DQL1	VSS	
H		VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ	
J		VDD	DQL4	DQL6				DQL7	DQL5	VDD	
K		VSS	VDDQ	VSS				VSS	VDDQ	VSS	
L		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	
M		ALERT_n	VSS	CS_n				CK_c	VSS	VDD	
N		VDDQ	CA4	CA0				CA1	CA5	VDDQ	
P		VDD	CA6	CA2				CA3	CA7	VDD	
R		VDDQ	VSS	CA8				CA9	VSS	VDDQ	
T		CAI	CA10	CA12				CA13	CA11	RESET_n	
U	NC	VDD	VSS	VDD				VPP	VSS	VDD	NC

MO-210-AT (x16)



with support balls



O Populated ball
\+ Ball not populated

Note: 1. Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU (x16) with support balls are for mechanical support only, and should not be tied to either electrically high or low.

2. Some of the additional support balls can be selectively populated under the supplier's discretion.

106-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All command/address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides external Rank selection on systems with multiple Ranks. CS_n is considere part of the command code.CS_n is also used to enter and exit the parts fro power down modes.
DM_n, DMU_n, DML_n	Input	**Input Data Mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write acces DM_n is sampled on both edges of DQS. For x8 device, the function of DM is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA[13:0]	Input	**Command/Address Inputs:** CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operatio RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 2(of VDDQ,
DQ	Input/Output	**Data Input/Output:** Bidirectional data bus. If CRC is enabled via the mode register, CRC code is added at the end of a data burst.

106-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
DQS_t, DQS_c, DQSU_t,DQSU_c, DQSL_t, DQSL_c	Input/Output	**Data Strobe:** Output with read data, input with write data, edge-aligned with read data, centered in write data. For x16 devices, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. The device supports differential data strobe only, not single-ended.
TDQS_t, TDQS_c	Output	**Termination Data Strobe:** TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs mu disable the TDQS function via MR5:OP[4]=0.
ALERT_n	Input/Output	**Alert:** If there is an error in CRC, ALERT_n drives LOW for the period time Interval and returns HIGH. During the connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In cases where this pin is not connected, ALERT_n must be bonded to VDDQ on the system board.
TEN	Input	**Connectivity Test Mode Enable:** Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDDQ. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pulldown resistor to VSS.
MIR	Input	**Mirror:** Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected (strapped) to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSS if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected (Strapped) to VDDQ. No active signaling requirements defined
CAI	Input	**Command and Address Inversion:** With the CAI pin connected (strapped) to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSS if no CA inversion is required. No active signaling requirements defined.

106-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
CA_ODT	Input	**ODT for Command and Address:** Apply Group A settings if the pin is connected (strapped) to VSS and apply Group B settings if the pin is connected (strapped) to VDDQ. No active signalling requirements defined.
LBDQ	Ouput	**Loopback Data Output:** The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
LBDQS	Ouput	**Loopback Data Strobe Output:** A single-ended strobe with the rising edged aligned with loopback data edge, falling edge aligned with data center. When loopback is enabled, it is in driver mode using the default RON described in the Loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use.
NC		No Connect: No internal electrical connection is present.

106-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
VDDQ	Supply	DQ power supply; 1.1V nominal.
VDD	Supply	Power supply; 1.1V nominal.
VSS	Supply	Ground
VPP	Supply	Activating power supply; 1.8V nominal.
ZQ	Reference	Reference pin for ZQ calibration. This ball is tied to an external 240 ohm resistor (RZQ), which is tied to VSS.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.3 ~ +1.4		V
VDD	Power Supply Voltage	-0.3 ~ +1.4		V
VDDQ	Power Supply Voltage	-0.3 ~ +1.4		V
VPP	Power Supply Voltage	-0.3 ~ +2.1		V
TOP	Operating Temperature Range	Commercial	0 ~ +95	°C
		Industrial	-40~+95	°C
TSTG	Storage Temperature Range	-55 ~ +100		°C

Note: 1.Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

3. All operating temperature symbols, ranges, acronyms from JESD402-1.

DC Operating Conditions(Low Frequency Voltage)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	1.067	1.1	1.166	V
V_{DDQ}	Supply voltage for output	1.067	1.1	1.166	V
V_{PP}	Wordline supply voltage	1.746	1.8	1.908	V

Input/ Output Capacitance

Symbol	Parameters	Min.	Max.	Unit	Notes
CIO	Input capacitance	0.35	0.9	pF	1,2
CDIO	Input/output capacitance	-0.1	0.1	pF	1,2,8
CDDQS	Input/output capacitance	-	0.04	pF	1,2,4
CCK	Input capacitance delta	0.2	0.6	pF	1,2
CDCK	Input capacitance	-	0.05	pF	1,2,3
CI	Input capacitance	0.2	0.6	pF	1,2,5,12
CDI_CS	Input capacitance delta(CS_n pins only)	-0.1	0.1	pF	1,2,6
CDI_CA	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	pF	1,2,7
CALERT	Input/output capacitance	0.3	1.5	pF	1,2
CLoopback	Input/output pin capacitance, ZQ	0.3	1.0	pF	1,2
CTEN	Input capacitance of TEN	0.2	2.3	pF	1,2,9
CZQ	Input capacitance of ZQ	-	5	pF	1,2,11
CSTRAP	Input capacitance of MIR, CAI, CA_ODT pins	-	10	pF	1,2,10

Notes1: This parameter is not subject to production test.

Notes2: This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

Notes3: Absolute value CIO(CK_t) - CIO(CK_c)

Notes4: Absolute value of CIO(DQS_t) - CIO(DQS_c)

Notes5: CI applies to CS_n and CA[13:0]

Notes6: CDI_CS_n = CI(CS_n) - 0.5 × (CI(CLK_t) + CICLK_c))

Notes7: CDI_CA = CI(CA) - 0.5 x (CI(CLK_t) + CI(CLK_c)).

Notes8: CDIO = CIO(DQ,DM) - Avg(CIODQ,DM))

Notes9: TEN pin may be DRAM internally pulled LOW through a weak pull-down resistor to VSS. In this case, CTEN might not be valid and the system must verify TEN signal with vendor-specific information.

Notes10: MIR, CAI, and CA_ODT are strap pins used to configure module or point-to-point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.

Notes11: Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality/accuracy with the max capacitive load is characterized.

Notes12: CI options are incorporated VcIVW in the DRAM CA, CS Parametric Values.

DRAM Package Electrical Specifications

Parameters	Symbol	Min.	Max.	Unit	Notes
Input/output Zpkg	Zpkg_DQ	45	75	ohm	1,2,4,5,10
Input/output pkg delay	Tpkg_delay_DQ	10	40	ps	1,3,4,5
DQS_t, DQS_c Zpkg	Zpkg_DQS	45	75	ohm	1,2,5,10,12
DQS_t, DQS_c pkg delay	Tpkg_delay_DQS	10	40	ps	1,3,5,10,12
Delta Zpkg DQS_t, DQS_c	Zpkg_DQS	-	5	ohm	1,2,5,7,10
Delta delay DQS_t, DQS_c	Tpkg_delay_DQS	-	2	ps	1,3,5,7,10
Input-CTRL pins Zpkg	Zpkg_CTRL	45	75	ohm	1,2,5,9,10
Input-CTRL pins pkg delay	Tpkg_delay_CTRL	10	40	ps	1,3,5,9,10
Input-CMD ADD pins Zpkg	Zpkg_CA	45	75	ohm	1,2,5,8,10
Input-CMD ADD pins pkg delay	Tpkg_delay_CA	10	45	ps	1,3,5,8,10,13
CLK_t and CLK_c Zpkg	Zpkg_CLK	45	75	ohm	1,2,5,10
CLK_t and CLK_c pkg delay	Tpkg_delay_CLK	10	45	ps	1,3,5,10
Delta Zpkg CLK_t and CLK_c	DZpkg_delay_CLK	-	5	ohm	1,2,5,6,10
Delta delay CLK_t and CLK_c	DTpkg_delay_CLK	-	2	ps	1,3,5,6,10
ALERT Zpkg	Zpkg_ALERT	45	75	ohm	1,2,5,10
ALERT delay	Tpkg_delay_ALERT	10	60	ps	1,3,5,10
Loopback Zpkg	Zpkg_Loopback	45	75	ohm	1,2,5,10,11
Loopback delay	Tpkg_delay_Loopback	10	60	ps	1,3,5,10,11

Notes1: This parameter is not subject to production test.

Notes2: This parameter is measured by using vendor-specific measurement methodology

Notes3: This parameter is measured by using vendor-specific measurement methodology

Notes4: Zpkg_DQ and Tpkg_delay_DQ applies to DQ, DM, TDQS_t, and TDQS_c.

Notes5: This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

Notes6: Absolute value of Zpkg_CK_t - Zpkg_CK_c for impedance (Z) or absolute value of Tpkg_delay_CK_t - Tpkg_delay_CK_c for delay (Tpkg_delay).

Notes7: Absolute value of Zpkg(DQS_t) - Zpkg(DQS_c) for impedance (Z) or absolute value of

Tpkg_delay_DQS_t - Tpkg_delay_DQS_c for delay (Tpkg_delay)

Notes8: Zpkg_CA and Tpkg_delay_CA applies to CA[13:0].

Notes9: Zpkg_CTRL and Tpkg_delay_CTRL applies to CS_n.

Notes10: Package implementations must meet specifications if the designed Zpkg and Tpkg_delay fall within the ranges shown.

Notes11: Zpkg_Loopback and Tpkg_delay_Loopback applies to LBDQ and LBDQS.

Notes12: Zpkg_DQS and Tpkg_delay_DQS applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

Differential Input Voltage Levels for Clock

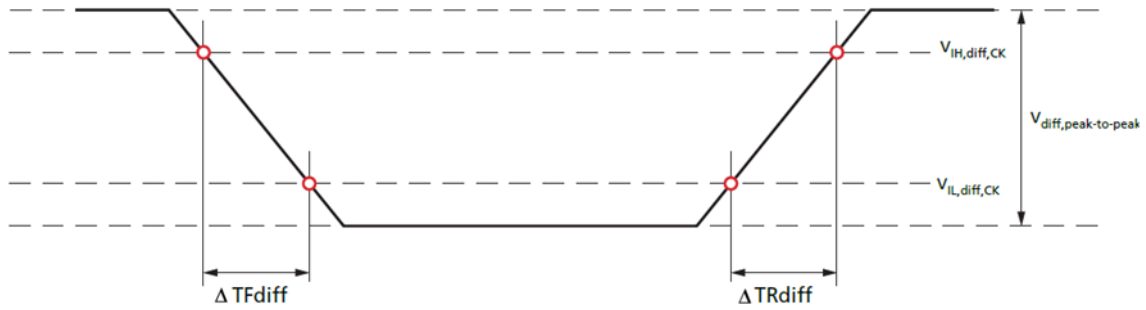
Symbol	Parameter	DDR5 4800/5600	Note
VIH,diffCK	Differential input high measurement level	0.75 x Vdiff,pk-pk	1,2
VIL,diffCK	Differential input low measurement level	0.25 x Vdiff,pk-pk	1,2

Note1: Vdiff,pk-pk defined in the Differential Input Slew Rate Definition for CK_t, CK_c figure

Note2: Vdiff,pk-pk is the mean high voltage minus the mean low voltage over 8UI samples.

Note3: All parameters are defined over the entire clock common mode range.

Differential Input Slew Rate Definition for Clock



Parameter	Measured		Defined By
	From	To	
Differential input slew rate for rising edge (CK_t - CK_c)	VIL,diffCK	VIH,diffCK	|(VIL,diffCK - VIH,diffCK)| / delta TRdiff
Differential input slew rate for falling edge (CK_t - CK_c)	VIH,diffCK	VIL,diffCK	(VIH,diffCK - VIL,diffCK) / delta TFdiff

Differential Input Slew Rate for Clock (CK_t, CK_c) — 4800-5600

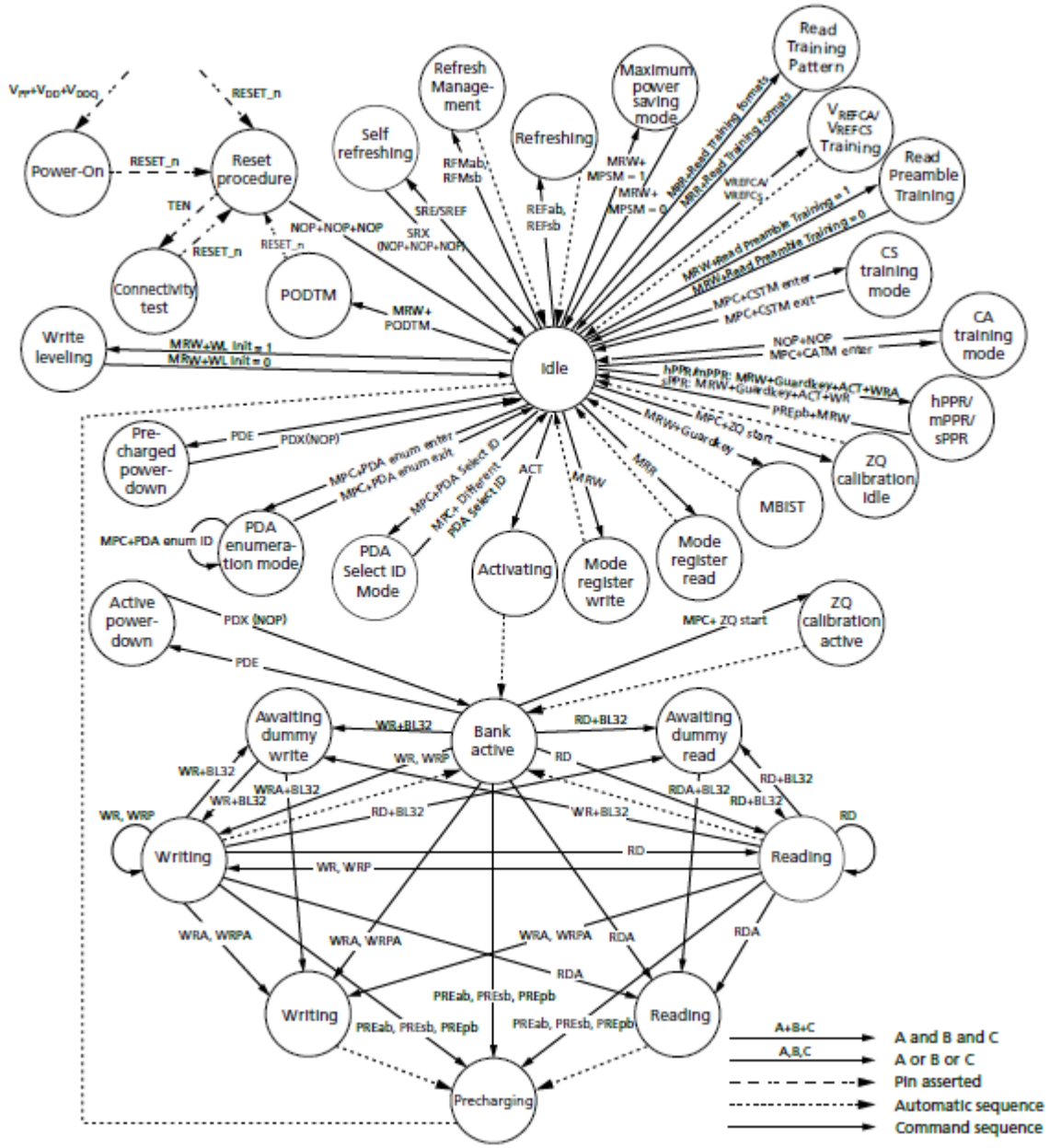
Parameter	Symbol	4800		5600		Units
		Min.	Max	Min.	Max	
Differential input slew rate for CK_t - CK_c	SRIdiff_CK	2	14	2	30	V/ns

Recommended DC Operating Conditions

VDD = VDDQ = 1.1V

Symbol	H2AD16G16F6S			Note
	IDD Max.	IDDQ Max.	IPPE Max.	
IDD0	58	22	10	
IDD0F	125	22	18	
IDD2N	30	21	4	
IDD2P	23	15	4	
IDD2NT	60	23	4	
IDD3N	50	21	7	
IDD3P	35	13	7	
IDD4R	265	290	10	
IDD4RC	265	290	10	
IDD4W	345	370	10	
IDD4WC	345	370	10	
IDD5B	230	23	56	
IDD5F	220	23	56	
IDD5C	95	23	25	
IDD6N	62	5	12	
IDD6E	80	8	16	
IDD7	420	290	40	
IDD8	16	6	4	
IDD6 Specification				
	IDD Max.	**IDDQ Max.**	**IPPE Max.**	
IDD6N	62	5	12	0 - 85 °C
IDD6E	80	8	16	0 - 95 °C

Simplified State Diagram



AC Operating Test Characteristics

DDR5- 4800 & 5600 Speed Bins

VDD = VDDQ = 1.1V

Symbol	Speed Bin	(DDR5-4800)		(DDR5-5600)		(DDR5-6400)		Units
	CL-nRCD-nRP	40-39-39		46-45-45		TBD		
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	
tAA	Internal read command to first data	16.000	22.222	16.000	22.222	-	-	ns
tRCD	Active to read or write delay	16.000	-	16.000	-	-	-	ns
tRP	Precharge command period	16.000	-	16.000	-	-	-	ns
tRC	Active to active/auto refresh command	48.000	-	48.000	-	-	-	ns
tRAS	Active to precharge command period	32	5×tREFI1 (Norm) 9×tREFI2(FGR)	32	5×tREFI1 (Norm) 9×tREFI2(FGR)	-	-	ns

Speed Bin	tAAmin(ns)	tRCDmin tRPmin(ns)	READ CL	Min.	Max.	Min.	Max.	Min.	Max.	Units
-	20.952	-	22	0.952	1.010	0.952	1.010	-	-	ns
3200	17.5	17.5	28	0.625	0.681	0.625	0.681	-	-	ns
3200	16.25	16.25	26	0.625	0.681	0.625	0.681	-	-	ns
3200	15	15	24	Reserved		Reserved		TBD		ns
3600	17.777	17.777	32	0.555	<0.625	0.555	<0.625	-	-	ns
3600	16.666	16.666	30	0.555	<0.625	0.555	<0.625	-	-	ns
3600	14.444	14.444	26	Reserved		Reserved		TBD		ns
4000	18	17.5	36	0.5	<0.555	0.5	<0.555	-	-	ns
4000	16	16	32	0.5	<0.555	0.5	<0.555	TBD		ns
4000	14	14	28	Reserved		Reserved		TBD		ns
4400	18.181	17.727	40	0.454	<0.5	0.454	<0.5	-	-	ns
4400	16.363	16.363	36	0.454	<0.5	0.454	<0.5	-	-	ns
4400	14.545	14.545	32	Reserved		Reserved		TBD		ns
4800	17.5	17.5	42	0.416	<0.454	0.416	<0.454	-	-	ns
4800	16.666	16.666	40	0.416	<0.454	0.416	<0.454	-	-	ns
4800	16.666	16.250	40	0.416	<0.454	0.416	<0.454	-	-	ns
4800	14.166	14.166	34	Reserved		Reserved		TBD		ns
5200	17.692	17.62	46	-	-	0.384	<0.416	-	-	ns
5200	16.153	16.153	42	-	-	0.384	<0.416	TBD		ns
5200	14.615	14.615	38	-	-	Reserved		TBD		ns
5600	17.857	17.5	50	-	-	0.357	<0.384	-	-	ns
5600	16.428	16.428	46	-	-	0.357	<0.384	-	-	ns
5600	16.428	16.071	46	-	-	0.357	<0.384	TBD		ns

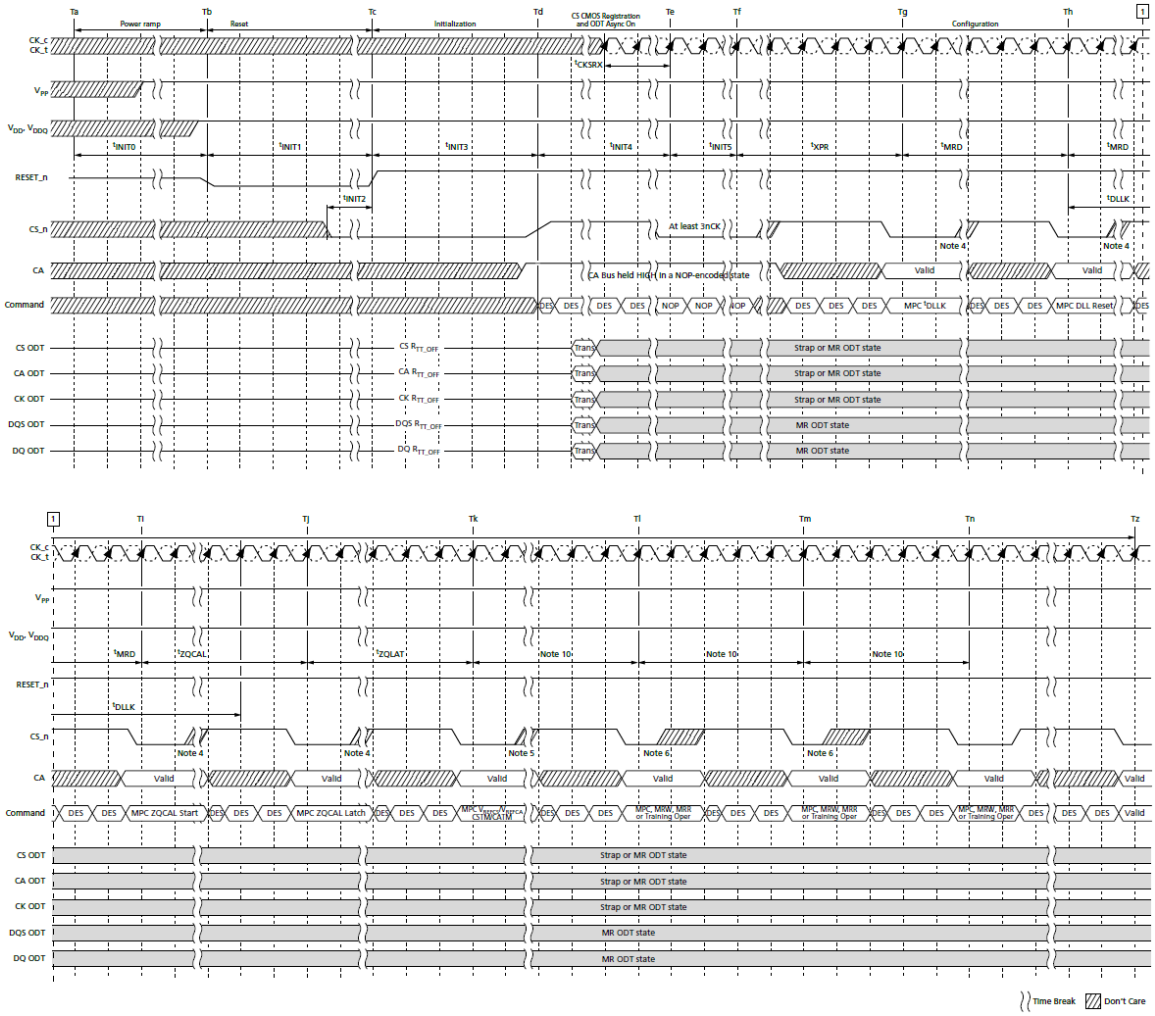
5600	14.285	14.285	40	-	-	Reserved		TBD		ns
				-	-	-	-			ns
				-	-	-	-			ns
				-	-	-	-			ns
				-	-	-	-			ns
				-	-	-	-			ns
				-	-	-	-			ns
Support CL Settings				22,26,28,30,32,36,40,42		22,26,28,30,32,36,40,42,46,50		TBD		nCK

Power-up and Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. While applying power (after Ta), RESET_n must be LOW (≤0.2 x VDDQ) while all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the Input Voltage Power-up and Power-down Sequence section that follows. During power up and power down, |VDDQ-VDD| must be equal to or less than 200mV, and VPP must always be equal to or greater than VDDQ.
2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ,DQS_t, DQS_c, CS_n, CK_t, CK_c and CA input levels must be between VSS and VDDQ to avoid latch-up.
3. Beginning at Tb, RESET_n must be maintained LOW for a minimum of tINIT1 (Tb to Tc), after which RESET_n may be de-asserted to HIGH (Tc). At least tINIT2 (10ns) before RESET_n deassertion, CS_n must be set LOW. All other input signals are don't care. The device supports the ability for RESET_n to be held LOW indefinitely.
4. After RESET_n is de-asserted (Tc), wait at least tINIT3 before driving CS_n HIGH.
5. After CS_n deasserts HIGH (Td), wait a minimum of tINIT4 to enable the CS_n, CK and CA, DQ, and DQS ODT to go to the defined strap initial state (Te). Clock (CK_t, CK_c) is required to be started and stabilized for tCKSRX before exit of tINIT4 (Te). Upon the completion of (Te), all ODT states (CA, CS_n, CK, DQ and DQS ODT) should be valid. The CS receiver should no longer be in its CMOS-based mode. ODT termination states remain uncalibrated until completion of ZQcal at (Tj).
6. Upon (Te), NOP commands must be issued for a minimum of tINIT5 to conclude exit of initialization process and start tXPR timer at (Tf). The system must wait at least tXPR before issuing any legal configuration commands (Tg). During early configuration steps (Tg to Tk), only MRR,MRW, MPC, VREFCS and VREFCA commands are legal. MRR and MRW command while legal, may not execute properly until CS and CA training routines are completed.
7. Between (Tg) and (Tj), the following initial configuration modes must be completed prior to other training modes:
   a) MPC for setting MR13 (tCCD/tDLLK/tCCD_L_WR/tCCD_L_WR2) must be issued before the MPC command to reset the DLL.
   b) MPC to execute DLL RESET must be issued before ZQCal Start.
   c) MPC to execute ZQCal Start followed by ZQCal Latch must be issued before any other training modes such as VREFCS, VREFCA, CS and CA Training.
8. Between (Tk to Tz), any number of legal configuration commands are allowed. Many trainingbased commands are optional and may be done at the system architect's discretion and may vary depending on the system, though proper setting of certain registers, such as those related to write leveling training, is required. The host must follow multicycle MPC timing requirements in cases where the alignment between CS_n, CA and CK is unknown, (that is, prior to successfully completing VREFCS, VREFCA, CS and CA training commands or host-provided successful training solutions). MRW and MRR commands can be used after the alignment between CS_n, CA and CK are known. Single-cycle CS_n assertions are allowed after setting MR2:OP[4] = 1.
9. After (Tz), and the completion of any training or calibration timing parameters (tZQLAT) is satisfied, the device is ready for normal operation and is able to accept any valid command. Any additional mode registers that have not previously been set up for normal operation should be written at this time. If the host uses writeback suppression mode, it should be set after the initial write process to prevent aliasing to a 2-bit error.
10. After all mode registers have been programmed for normal operation, optional MBIST mode can be entered by writing MR23:OP[4] to HIGH, followed by subsequent MR24 PPR guard keys. The device then drives ALERT_n to LOW for a maximum of tSELFTEST time. The device drives ALERT_N to HIGH to indicate the operation is complete. After ALERT_n is driven HIGH, the device is immediately ready to receive valid commands. The MBIST/mPPR transparency status must subsequently be checked in MR22:OP[2:0] to determine whether mPPR should be performed.

Reset Procedure with Stable Power



Note 1: From (Td) until (Te), the CA bus must be held HIGH in a NOP encoded state.

Note 2: From (Te) until (Tf), NOP commands must be applied on the CA bus.

Note 3: From (Tf) until (Tk), DES commands must be applied between legal commands (MRR, MRW, MPC,VREFCS, and VREFCA). MRR and MRW commands while legal, may not execute properly until CS and CA training routines are completed.

Note 4: Prior to ZQcal completion at (Tk), MPC commands will be multicycle as described in the MPC Command Timing section.

Note 5: From time point (Tk) until (Tl) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, must be multicycle (MR2:OP[4] = 0) as described in the MPC, VREFCS, and VREFCA timing sections.

Note 6: At time point (Tl), with successful completion of CS and CA training, an MRW command setting MR2:OP[4] =1 is recommended and enables MPC, VREFCS, VREFCA commands to be single-cycle,improving training duration.

Note 7: From time point (Tk) until (Tz), DES commands will be applied between legal commands (MRR, MRW,MPC, VREFCS and VREFCA).

Note 8: Starting at (TI), MRW commands must be issued to all mode registers that require non-default settings.

Note 9: Default ODT tolerances are wider prior to ZQ calibration.

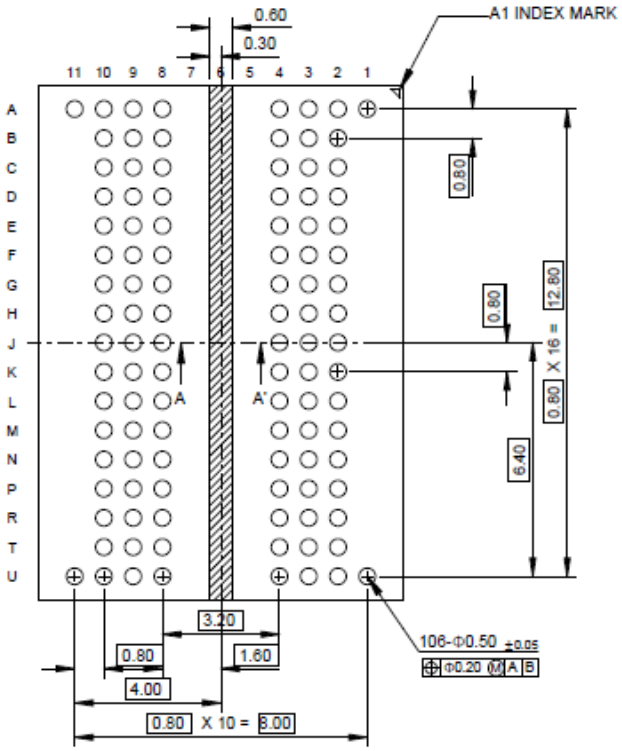
Note 10: All MPC/MRW/MRR to MPC/MRW/MRR commands must meet the timing restrictions required.

DDR5 Function Matrix

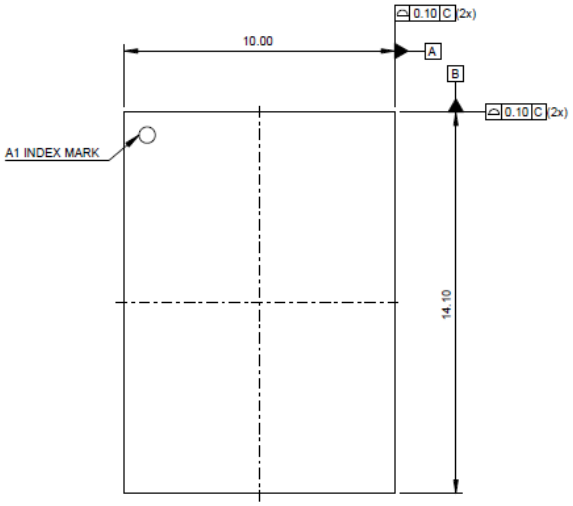
Functions	x16	NOTE
Write Leveling	V	
Temperature controlled Refresh	V	
Fine Granularity Refresh	V	
Same Bank Refresh	V	
Refresh for Management		
Data Mask	V	
Command Address Inversion	V	
TDQS		
ZQ calibration	V	
DQ Vref Training	V	
Per DRAM Addressability	V	
Mode Register Readout	V	
WRITE CRC	V	
READ CRC	V	
Programmable Preamble/Postamble	V	
Maximum Power Saving Mode	V	
Connectivity Test Mode	V	
Bit Error Rate Test	V	
Package Output Driver Test Mode	V	
3DS		
CA Training Mode	V	
CS Training Mode	V	
DQS interval Oscillator	V	
ECC Transparency and Error Scrub	V	
Lookback	V	
Duty Cycle Adjuster	V	

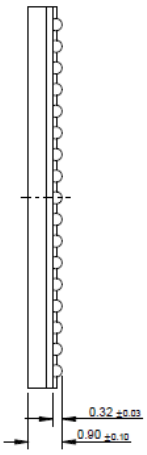
Package Description: 106Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



BOTTOM VIEW





TOP VIEW

SIDE VIEW

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Nov. 2023	Rico Yang	N/A
1.0	First SPEC. release.	Nov. 2023	Rico Yang	N/A