

8Gb (62Mx8Banksx16) DDR4 SDRAM

Descriptions

The 8Gb DDR4 SDRAM is organized as 64Mbit x16 I/Os x 8banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 3200Mb/sec/ pin (DDR4-3200) for general applications. The chip is designed to comply with the following key DDR4 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. The DDR4 device operates with a single 1.2V (1.14V~1.26V) power supply and 1.2V (1.14V~1.26V)VDDQ and 2.5V(2.375V~2.75V)VPP. The 8Gb DDR4 device is available in 96ball FBGAs.

Features

- JEDEC standard 1.2V (1.14V~1.26V)
- VDDQ = 1.2V (1.14V~1.26V)
- VPP = 2.5V (2.375V~2.75V)
- 8-bit pre-fetch
- 8 Banks (2 Bank Groups)
- Programmable CAS Write Latency (CWL):
9,10,11,12,14,16,18,20
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal (self) calibration: calibration through ZQ pin (RZQ: 240 ohm \pm 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95°C
- Support Industrial Temp (-40°C to 95°C)
 - tREFI 7.8us at -40°C \leq TCASE \leq 85°C
 - tREFI 3.9us at 85°C < TCASE \leq 95°C
- Connectivity Test Mode (TEN) is Supported
- Asynchronous Reset
- CRC for Read/Write data security
- Command address parity check
- DBI (Data Bus Inversion)
- Gear down mode
- POD (Pseudo Open Drain) interface for data input/output
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- PPR and sPPR is supported
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free

Ordering Information

Part No	Organization	Max. Data Rate	Package	Grade
H2A908G16A6OILC	512M X 16	DDR4-2400MHz 17-17-17	96 Ball BGA, 7.5x13.3mm	Commercial
H2A908G16A6OJLC	512M X 16	DDR4-2666MHz 19-19-19	96 Ball BGA, 7.5x13.3mm	Commercial
H2A908G16A6OKLC	512M X 16	DDR4-3200MHz 22-22-22	96 Ball BGA, 7.5x13.3mm	Commercial
H2A908G16A6OILI	512M X 16	DDR4-2400MHz 17-17-17	96 Ball BGA, 7.5x13.3mm	Industrial
H2A908G16A6OJLI	512M X 16	DDR4-2666MHz 19-19-19	96 Ball BGA, 7.5x13.3mm	Industrial
H2A908G16A6OKLI	512M X 16	DDR4-3200MHz 22-22-22	96 Ball BGA, 7.5x13.3mm	Industrial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n	VDD	L
M	VREFCA	BG0	A10/AP				A12/BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

Input / Output Functional Description

Type	Symbol	Description
Input	CK_t, CK_c	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
Input	CKE, (CKE1)	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c,ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
Input	CS_n, (CS1_n)	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
Input	ODT, (ODT1)	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, For x16 configurations ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
Input	ACT_n	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
Input	RAS_n/A16, CAS_n/A15, WE_n/A14	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
Input/Output	DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8

Input	BG0 - BG1	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
Input	BA0 - BA1	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
Input	A0 - A17	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for x4 configurations
Input	A10 / AP	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
Input	A12 / BC_n	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Input	RESET_n	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD,
Input / Output	DQ	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
Input / Output	DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c ,	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
Output	TDQS_t, TDQS_c	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, 12, 10 and TDQS_c is not used. x16 must disable the TDQS function via mode register A11 = 0 in MR1.

Input	PAR	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0 and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.
Input/Output	ALERT_n	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
Input	TEN	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
	NC	No Connect: No internal electrical connection is present.
Supply	VDDQ	DQ Power Supply: 1.2 V +/- 0.06 V
Supply	VSSQ	DQ Ground
Supply	VDD	Power Supply: 1.2 V +/- 0.06 V
Supply	VSS	Ground
Supply	VPP	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
Supply	VREFCA	Reference voltage for CA
Supply	ZQ	Reference Pin for ZQ calibration
NOTE : Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.3 ~ +1.5		V
VDD	Power Supply Voltage	-0.3 ~ +1.5		V
VDDQ	Power Supply Voltage	-0.3 ~ +1.5		V
VPP	Power Supply Voltage	-0.3 ~ +3.0		V
TOP	Operating Temperature Range	Commercial	0 ~ +95	°C
		Industrial	-40 to 95	
TSTG	Storage Temperature Range	-55 ~ +100		°C

Note:

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV.
- VPP must be equal or greater than VDD/VDDQ at all times.
- Overshoot area is above 1.5 V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	Supply voltage	1.14	1.2	1.26	V
VDDQ	Supply voltage for output	1.14	1.2	1.26	V
VPP	Wordline supply voltage	2.375	2.5	2.750	V

Note:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- DC bandwidth is limited to 20MHz.

Input/ Output Capacitance

Symbol	Parameters	Min.	Max.	Unit	Notes
CCK	Input capacitance	0.2	0.7	pF	1,3
CDCK	Input capacitance delta	0	0.05	pF	1,3,4
CDI_CTRL	Input capacitance delta	-0.1	0.1	pF	1,3,7,8
CDI_ADD_CMD	Input capacitance delta	-0.1	0.1	pF	1,2,9,10
CIO	Input/output capacitance	0.55	1.15	pF	1,2,3
CI	Input capacitance	0.2	0.7	pF	1,3,6
CDIO	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,11
CDDQS	Input/output capacitance delta	0	0.05	pF	1,2,3,5
CALERT	Input/output capacitance	0.5	1.5	pF	1,3
CZQ	Input/output pin capacitance, ZQ	-	2.3	pF	1,3,12
CTEN	Input/output capacitance	0.2	2.3	pF	1,3,13

Notes1: This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.

Notes2: DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS

Notes3: This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.

Notes4: Absolute value CK_T-CK_C

Notes5: Absolute value of CIO(DQS_T)-CIO(DQS_C)

Notes6: CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n, CAS_n/A16, WE_n/A14, ACT_n and PAR.

Notes7: CDI CTRL applies to ODT, CS_n and CKE

Notes8: CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))

Notes9: CDI_ADD_CMD applies to, A0-A17, BA0-BA1, BG0-BG1, RAS_n, CAS_n/A16, WE_n/A14, ACT_n and PAR.

Notes10: CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))

Notes11: CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))

Notes12: Maximum external load capacitance on ZQ pin: 5 pF.

Notes13: TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

DRAM Package Electrical Specifications

Parameters		Symbol	Min.	Max.	Unit	Notes
Input/ output	Zpkg	ZIO	45	85	ohm	
	Package delay	TdIO	14	45	ps	
	Lpkg	LIO	-	3.4	nH	
	Cpkg	CIO	-	0.82	pF	
DQS_t, DQS_c	Zpkg	ZIO DQS	45	85	ohm	
	Package delay	TdIO DQS	14	45	ps	
	Lpkg	LIO DQS	-	3.4	nH	
	Cpkg	CIO DQS	-	0.82	pF	
	Delta Zpkg	DZIO DQS	-	10	ohm	
	Delta delay	DTDIO DQS	-	5	ps	
Input CTRL pins	Zpkg	ZI CTRL	50	90	ohm	
	Package delay	TdI CTRL	14	42	ps	
	Lpkg	LI CTRL	-	3.4	nH	
	Cpkg	CI CTRL	-	0.7	pF	
Input CMD ADD pins	Zpkg	ZI ADD CMD	50	90	ohm	
	Package delay	TdI ADD CMD	14	52	ps	
	Lpkg	LI ADD CMD	-	3.9	nH	
	Cpkg	CI ADD CMD	-	0.86	pF	

DRAM Package Electrical Specifications(Continued)

Parameters		Symbol	Min.	Max.	Unit	Notes
CK_t, CK_c	Zpkg	ZCK	50	90	ohm	
	Package delay	TdCK	14	42	ps	
	Package delay	DZDCK	-	10	ohm	
	Delta delay	DTdDCK	-	5	ps	
Input CLK	Lpkg	LI CLK	-	3.4	nH	
	Cpkg	CI CLK	-	0.7	pF	
ZQ Zpkg		ZO ZQ	-	100	ohm	
ZQ delay		TdO ZQ	20	90	ps	
ALERT Zpkg		ZO ALERT	40	100	ohm	
ALERT delay		TdO ALERT	20	55	ps	

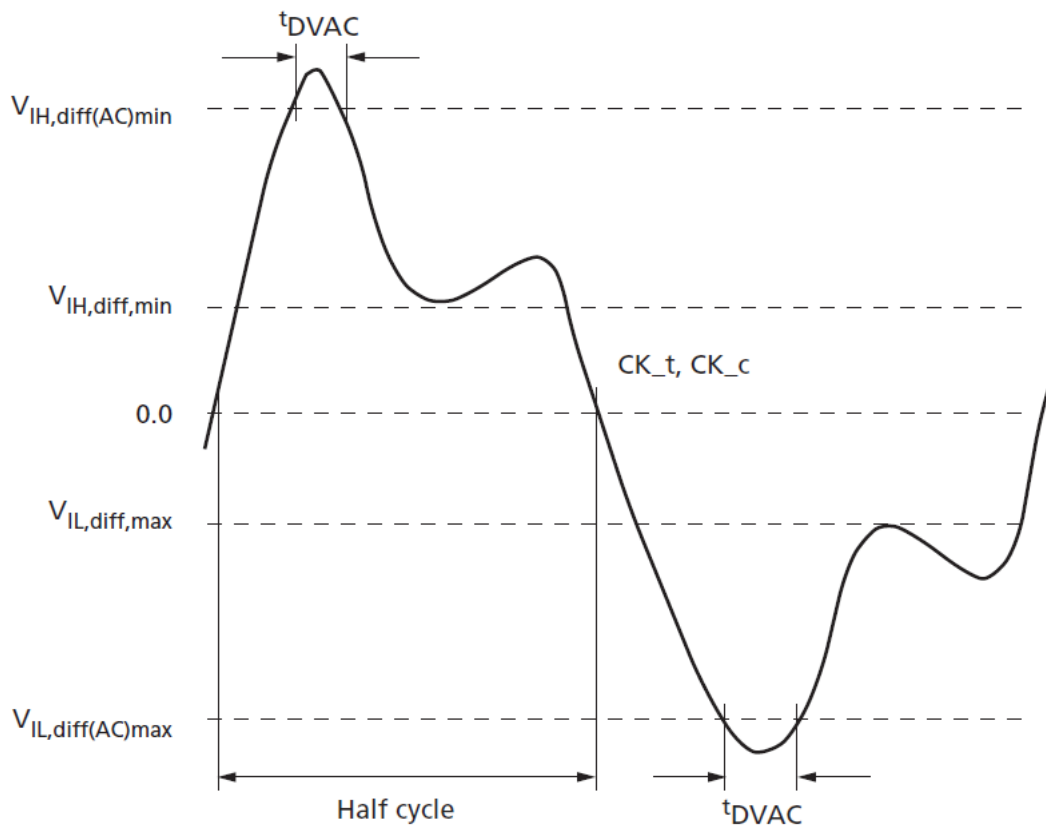
Notes1: Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown

Notes2: It is assumed that Lpkg can be approximated as $L_{pkg} = Z_o * T_d$

Notes3: It is assumed that Cpkg can be approximated as $C_{pkg} = T_d / Z_o$

AC and DC Differential Input Measurement Levels

Differential Inputs



Differential Input Swing Requirements for CK_t, CK_c

Symbol	Parameter	Min.	Max.	Units	Note
V _{IHdiff}	Differential input high	+0.135	See Note3	V	1
V _{ILdiff}	Differential input low	See Note3	-0.135	V	1
V _{IHdiff (AC)}	AC Differential input high	2x(V _{IH(AC)} -V _{REF})	See Note3	V	2
V _{ILdiff (AC)}	AC Differential input low	See Note3	2x(V _{REF} -V _{IL(AC)})	V	2

Note1: Used to define a differential signal slew-rate.

Note2: For CK_t, CK_c use V_{IH(AC)} and V_{IL(AC)} of ADD/CMD and V_{REFCA}.

Note3: These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (V_{IHCA(DC)} max, V_{ILCA(DC)}min) for single-ended signals as well as the limitations for overshoot and undershoot..

Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

Minimum Time AC Time tDVAC for CK

Slew Rate [V/ns]	tDVAC (ps) at [VIH,diff(AC) to VIL,diff(AC)]	
	200mV	TBDmV
>4.0	120	--
4.0	115	--
3.0	110	--
2.0	105	--
1.9	100	--
1.6	95	--
1.4	90	--
1.2	85	--
1.0	80	--
<1.0	80	--

Note: Below VIL(AC).

Single-Ended Requirements for CK Differential Signals

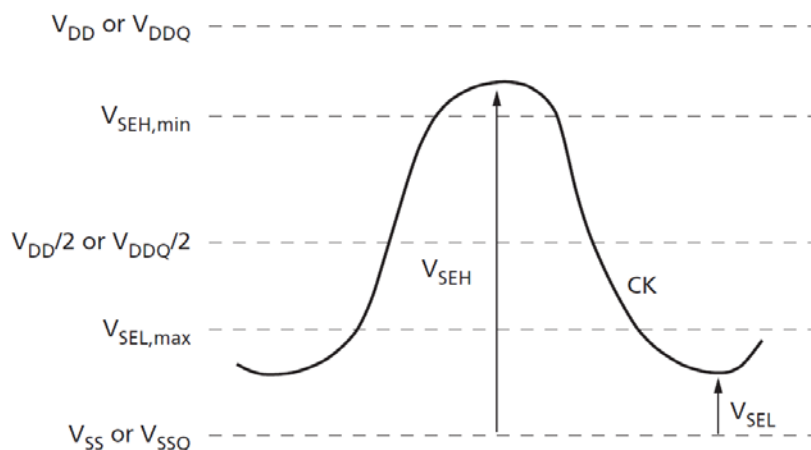
Each individual component of a differential signal (CK, DQS, /CK, /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(AC) / VIL(AC)) for Address/Command signals) in every half-cycle.

DQS, /DQS have to reach VSEHmin / VSELmax [approximately the ac-levels (VIH(AC) / VIL(AC)) for DQ signals] in every half-cycle preceding and following a valid transition.

Note that the applicable AC-levels for Address/Command and DQ's might be different per speed-bin etc. E.g., if VIHCA(AC100)/VILCA(AC100) is used for Address/Command signals, then these AC-levels apply also for the single-ended components of differential CK and /CK.

Single-Ended Requirements for CK



Single-Ended Requirements for CK

Symbol	Parameter	Min.	Max.	Units	Note
VSEH	Single-ended high-level for CK, /CK	$(VDD/2)+0.95$	See Note3	V	1,2
VSEL	Single-ended low-level for CK, /CK	See Note3	$(VDD/2)-0.95$	V	1,2

Note1: For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

Note2: ADDR/CMD VIH(AC) and VIL(AC) based on VREFCA.

Note3: These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

AC and DC Output Measurement Levels

Symbol	Parameter	Specification	Units	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	$1.1*VDDQ$	V	1
VOM(DC)	DC output middle measurement level (for IV curve linearity)	$0.8*VDDQ$	V	1
VOL(DC)	DC output low measurement level (for IV curve linearity)	$0.5*VDDQ$	V	1
VOH(AC)	AC output high measurement level (for output slew rate)	$(0.7+0.15)*VDDQ$	V	1
VOL(AC)	AC output low measurement level (for output slew rate)	$(0.7-0.15)*VDDQ$	V	1
VOHdiff(AC)	AC differential output high measurement level (for output slew rate)	$0.3*VDDQ$	V	2
VOLdiff(AC)	AC differential output low measurement level (for output slew rate)	$-0.3*VDDQ$	V	2

Notes1: The swing of $\pm 0.15 \times VDDQ$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7$ and an effective test load of 50Ω to $VTT = VDDQ$.

Notes2: The swing of $\pm 0.3 \times VDDQ$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7$ and an effective test load of 50Ω to $VTT = VDDQ$ at each differential output.

Recommended DC Operating Conditions

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
IDD0	Operating One Bank Active-Precharge Current (AL = 0) CKE: HIGH; External clock: On; tCK, nRC, nRAS, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: VDDQ; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the IDD0 Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	38	40	44	mA
IPP0	Operating One Bank Active-Precharge IPP Current (AL = 0) Same conditions as IDD0 above	4	4	4	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL = 0) CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, CL: see the previous table; BL: 8;1, 5 AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the IDD1 Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the following table); Output buffer and RTT: enabled in mode registers;2 ODT Signal: stable at 0	44	44	44	mA
IDD2P	Precharge Power-Down Current CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	11	11	11	mA
IDD2N	Precharge Standby Current (AL = 0) CKE: HIGH; External clock: On; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0; Pattern details: see the IDD2N and IDD3N Measurement-Loop Pattern table	18	18	19	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I _{DD3P}	Active Power-Down Current (AL = 0) CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	19	19	19	mA
I _{DD3N}	Active Standby Current (AL = 0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8 AL: 0; CS_n: stable at 1; Command, address, bank group address, ba address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0; Pattern details: see the IDD2N and IDD3N Measurement-Loop Pattern table.	27	27	27	mA
I _{DD4R}	Operating Burst Read Current (AL = 0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS_n: HIGH between RD; Command,address, bank group address, bank address inputs: partially toggling according to the IDD4R Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the IDD4R Measurement-Loop Pattern table; DM_n stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the IDD4R Measurement-Loop pattern table);Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	137	166	195	mA
I _{DD4W}	Operating Burst Write Current (AL = 0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8 AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4 Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to th IDD4W Measurement-Loop Pattern table; DM: stable at 0; Bank activi all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, (see IDD4W Measurement-Loop Pattern table);Output buffer and RTT enabled in mode registers (see note2); ODT signal: stable at HIGH	111	128	135	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I _{DD5B}	Burst Refresh Current (1X REF) CKE: HIGH; External clock: on; tCK, CL, nREFI: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between REF;Command, address, bank group address, bank address inputs: partially toggling according to the IDD5R Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: REF command every nREFI (see the IDD5R Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers2; ODT signal: stable at 0	204	204	204	mA
I _{PP5B}	Burst Refresh Current (1X REF) Same conditions as IDD5R above	18	18	18	mA
I _{DD6N}	Self Refresh Current: Normal Temperature Range TC: 0–85°C; Auto self refresh (ASR): disabled;3 Self refresh temperature range (SRT): normal;4 CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8;1 AL: 0; CS_n, command address, bank group address, bank address, data I/O: VDDQ; DM_n: stable at 1; Bank activity: SELF REFRESH operation ;Output buffer and RTT: enabled in mode registers;2 ODT signal: midlevel	22	22	22	mA
I _{PP6N}	Self Refresh IPP Current: Normal Temperature Range Same conditions as IDD6N above	4	4	4	mA
I _{DD7}	Operating Bank Interleave Read Current CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8;15 AL: CL -1; CS_n: HIGH between ACT and RDA; Command, address, group bank address, bank address inputs: partially toggling according to the IDD7 Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the IDD7 Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the IDD7 Measurement-Loop Pattern table; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	180	196	209	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I _{PP7}	Operating Bank Interleave Read IPP Current Same conditions as IDD7 above	14	16	18	mA
I _{DD8}	Maximum Power Down Current Place DRAM in MPSM then CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n:stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; 2 ODT signal: stable at 0	9	10	11	mA

Refresh Parameters

Parameter	Symbol	8G	Unit	Notes	
REF command to ACT or REF command time	tRFC (All bank groups)	350	ns	-	
Average periodic refresh interval	tREFI	0°C ≤ TC ≤ 85°C	7.8	μs	-
		85°C < TC ≤ 95°C	3.9	μs	*

Note: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

AC Operating Test Characteristics
DDR4-2400 & 2666 & 3200 Speed Bins

VDD = VDDQ = 1.2V ±60mV

Symbol	Speed Bin		(DDR4-2400)		(DDR4-2666)		(DDR4-3200)		Units
	CL-nRCD-nRP		17-17-17		19-19-19		22-22-22		
	Parameter		Min.	Max.	Min.	Max.	Min.	Max.	
tAA	Internal read command to first data		14.16	18	14.25	18	13.75	18	ns
tAA_DBI	Internal read command to first data with read DBI enabled		tAA(min) + 3nCK	tAA(max) + 3nCK	tAA(min) + 3nCK	tAA(max) + 3nCK	tAA(min) + 4nCK	tAA(max) + 4nCK	ns
tRCD	ACT to read or write delay		14.16	-	14.25	-	13.75	-	ns
tRP	PRE command period		14.16	-	14.25	-	13.75	-	ns
tRC	Active to active/auto refresh command		46.16	-	46.25	-	45.75	-	ns
tRAS	Active to precharge command period		32	9xtREFI	32	9xtREFI	32	9xtREFI	ns
READ: nonDBI	READ: DBI	WRITE	Min.	Max.	Min.	Max.	Min.	Max.	Units
CL=9	CL=11	CWL=9	Reserved		Reserved		Reserved		ns
CL=10	CL=12	CWL=9	1.5	1.6	1.5	1.6	Reserved		ns
CL=11	CL=13	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=12	CL=14	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=13	CL=15	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=14	CL=16	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=15	CL=18	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=16	CL=19	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=17	CL=20	CWL=12,16	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL=18	CL=21	CWL=12,16	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL=19	CL=22	CWL=14,18	-	-	0.75	<0.833	0.75	<0.833	ns
CL=20	CL=23	CWL=14,18	-	-	0.75	<0.833	0.75	<0.833	ns
CL=22	CL=26	CWL=16,20	-	-	-	-	0.625	<0.75	Ns
CL=24	CL=28	CWL=16,20	-	-	-	-	0.625	<0.75	ns
Support CL Settings			10-18		10-20		10-20,22,24		nCK
Support CL settings with read DBI			12-16, 18-21		12-15,17-23		12-16,18-24,26,28		nCK
Support CWL Settings			9-12, 14,16		9-12,14,16,18		9-12,14,16,18		nCK

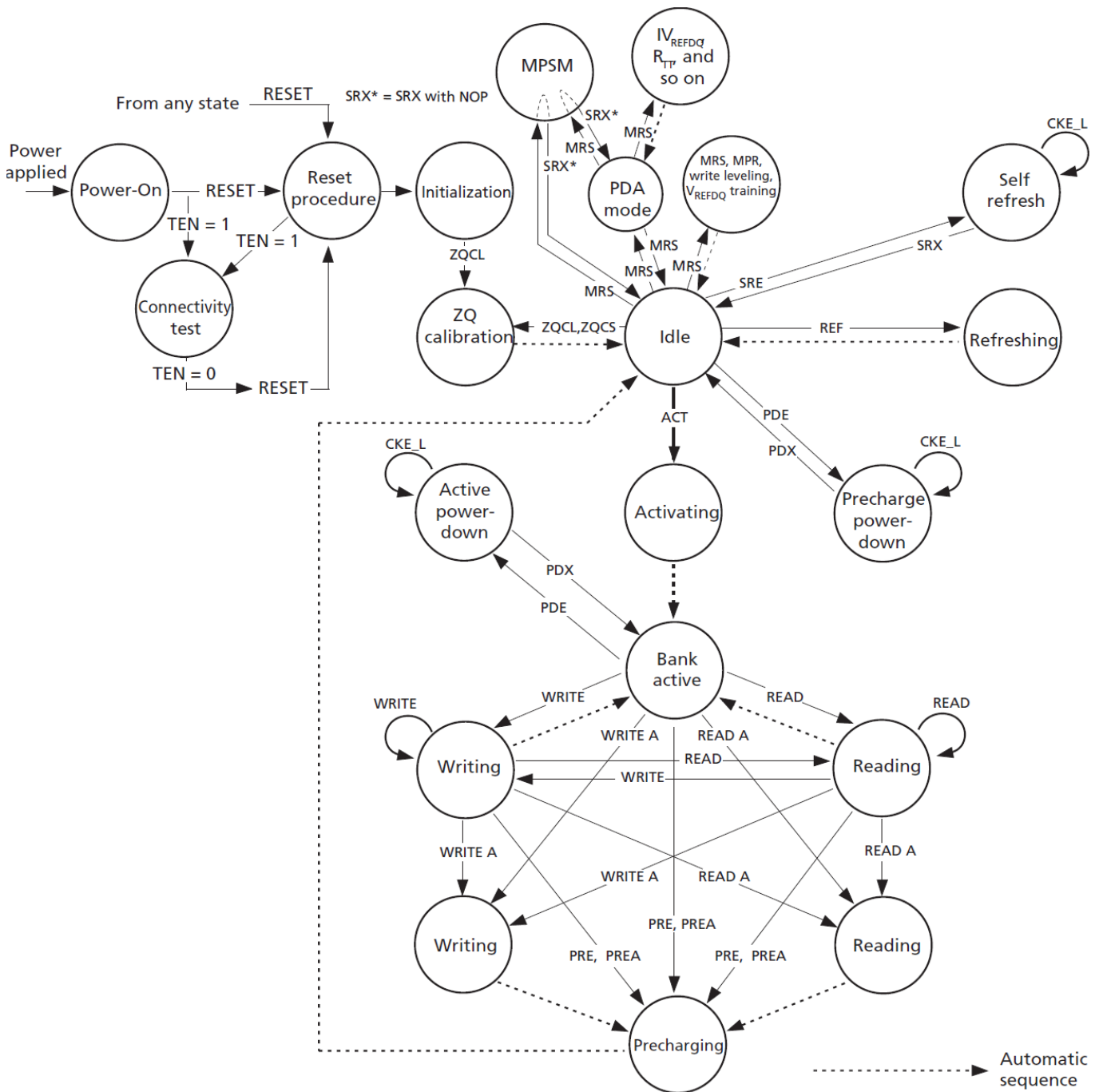
Speed Bin Table Note :

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-2400, 2666, and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Programmed 13.75ns on the DIMM SPD to be backward compatible to the lower frequency. The system operates clock cycle is calculated by dividing tAA, tRCD, tRP(in ns) by tCK(in ns) and rounding up to the next integer. tRC = 13.75ns + tRAS.
6. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
11. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
12. CL number in parentheses, it means that these numbers are optional.
13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

Simplified State Diagram



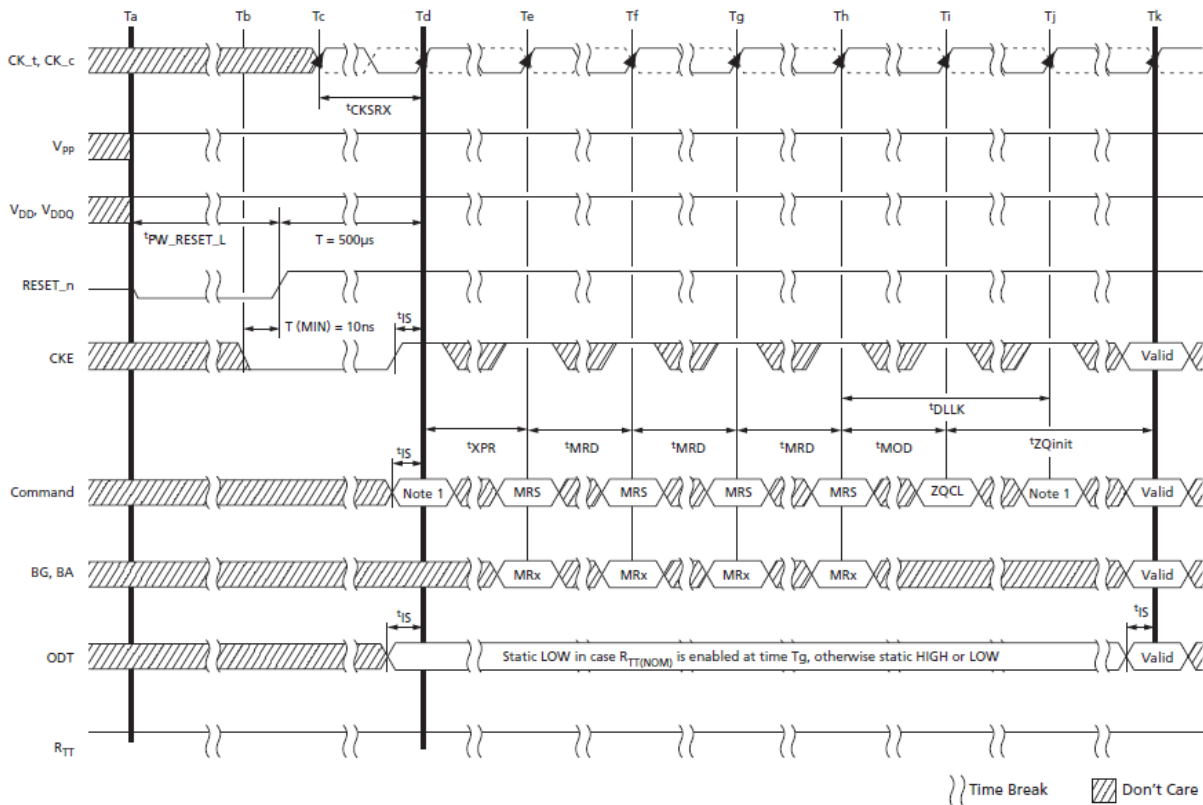
Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). /RESET needs to be maintained for minimum 700 us with stable power. CKE is pulled “Low” anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ volts.
 - VDD and VDDQ are driven from a single power converter output, AND
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
 - Vref tracks VDDQ/2. OR
 - Apply VDD without any slope reversal before or at the same time as VDDQ.
 - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After /RESET_n is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ($tXPR = \max(tXS ; 5 \times tCK)$)
6. Issue MRS command to load MR3 with all application settings, wait tMRD.
7. Issue MRS command to load MR6 with all application settings, wait tMRD.
8. Issue MRS command to load MR5 with all application settings, wait tMRD.
- 9 Issue MRS command to load MR4 with all application settings, wait tMRD.
10. Issue MRS command to load MR2 with all application settings, wait tMRD.
11. Issue MRS command to load MR1 with all application settings, wait tMRD.
12. Issue MRS command to load MR0 with all application settings, wait tMOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for tDLLK and tZQinit to complete.
15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).

Reset and Power up initialization sequence



Note 1: From time point T_d until T_k , a DES command must be applied between MRS and ZQCL commands.

Note 2: MRS commands must be issued to all mode registers that have defined settings.

Note 3: In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).

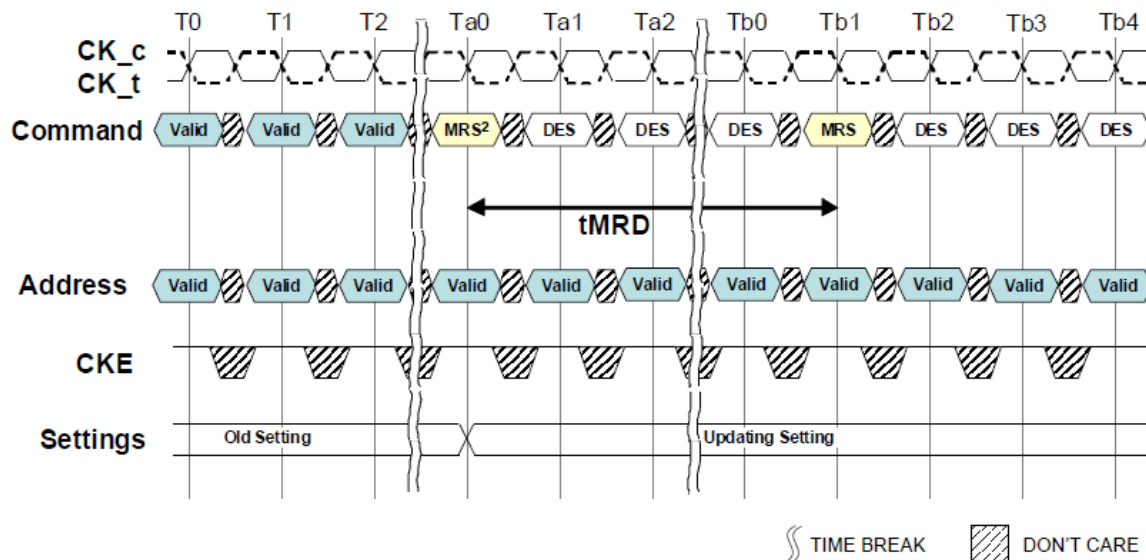
Note 4: TEN is not shown; however, it is assumed to be held LOW.

Register Definition

Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, **tMRD** is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in below.

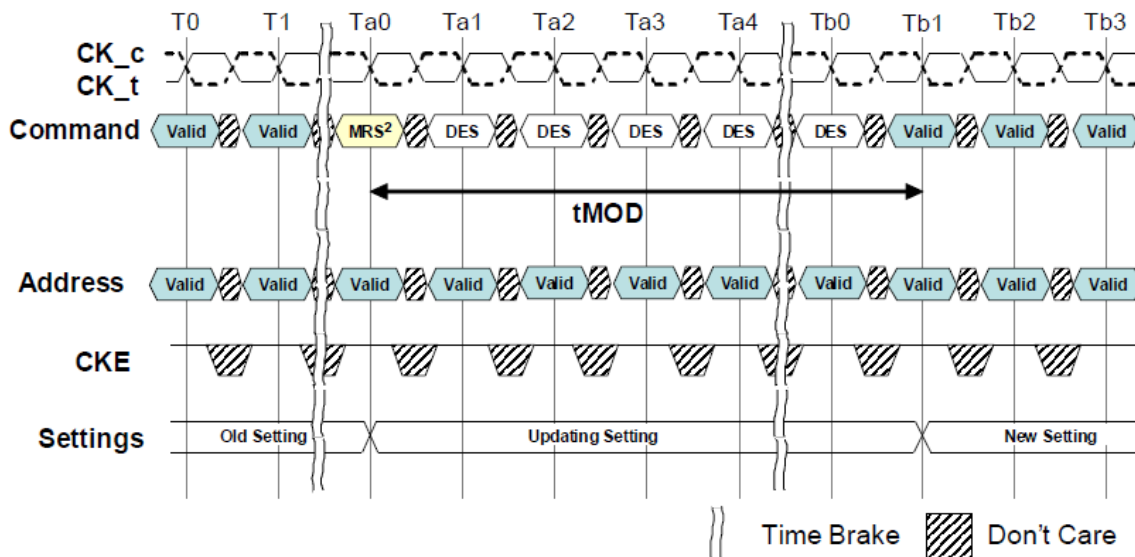


Note 1: This timing diagram shows C/A Parity Latency mode is "Disable" case.

Note 2: List of MRS commands exception that do not apply to tMRD

- Gear down mode
- tC/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- VrefDQ training Value, VrefDQ Training mode and VrefDQ training Range

The most MRS command to Non-MRS command delay, **tMOD**, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES shown in below.



Note 1: This timing diagram shows CA Parity Latency mode is “Disable” case.

Note 2: List of MRS commands exception that do not apply to tMOD.

- DLL Enable, DLL Reset
- VrefDQ training Value, internal Vref Monitor, VrefDQ Training mode and VrefDQ training Range
- Gear down mode
- Per DRAM addressability mode
- Maximum power saving mode
- CA Parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. The ODT signal may be registered high after tMOD has expired. ODT signal is a don't care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.

Mode Register

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13 ⁵ , A11:A9	WR and RTP ^{2,3}	Write Recovery and Read to Precharge for auto precharge(see Table 2)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12,A6:A4,A2	CAS Latency ⁴	(see Table 3)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

Note 1: Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Note 2: WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] =Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Note 3: The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

Note 4: The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency. Cas Latency controlled by A12 is optional for 4Gb device.

Note 5: A13 for WR and RTP setting is optional for 4Gb.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

CAS Latency

	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25 (only 3DS available)
1	0	0	0	1	26
1	0	0	1	0	27 (only 3DS available)
1	0	0	1	1	28
1	0	1	0	0	reserved for 29
1	0	1	0	1	30
1	0	1	1	0	reserved for 31
1	0	1	1	1	32
1	1	0	0	0	reserved

MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ³
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff ¹	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 4)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency	00 = 0(AL disabled) 10 = CL-2 01 = CL-1 11 = Reserved
A2, A1	Output Driver Impedance Control	(see Table 5)
A0	DLL Enable	0 = Disable ² 1 = Enable

Note 1: Outputs disabled - DQs, DQS_ts, DQS_cs.

Note 2: States reversed to “0 as Disable” with respect to DDR4.

Note 3: Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	TRR	0 = Disable 1 = Enable
A12	Write CRC	0 = Disable 1 = Enable
A11	RFU	0 = must be programmed to 0 during MRS
A11,A10:A9	RTT_WR	(see Table 6)
A8, A2	TRR Mode - BGn	00 = BG0 10 = BG2 01 = BG1 11 = BG3
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	(see Table 7)
A1:A0	TRR Mode - BAn	00 = Bank 0 10 = Bank 2 01 = Bank 1 11 = Bank 3

Note 1: Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CWL (CAS Write Latency)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 tCK Write Preamble		Speed Grade in MT/s for 2 tCK Write Preamble ¹	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	3200	2400	2666	2400
1	1	0	18		2666	3200	2666
1	1	1	20		3200		3200

Note 1: The 2 tCK Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

MR3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A11	MPR Read Format	00 = Serial 10 = Staggered 01 = Parallel 11 = ReservedTemperature
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 9)
A8:A6	Fine Granularity Refresh Mode	(see Table 8)
A5	Temperature sensor readout	0 : disabled 1: enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 10 = Page2 01 = Page1 11 = Page3 (see Table.8)

Note 1: Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Speed Bin
0	0	4nCK	1600
0	1	5nCK	1866,2133,2400
1	0	6nCK	TBD
1	1	RFU	RFU

MPR Data Format

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only
	01 = MPR1	CAS_n/ A15	WE_n/ A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/ A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency ⁴			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

Note 1: MPR used for C/A parity error log readout is enabled by setting A[2] in MR3

Note 2: For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.

Note 3: If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

Note 4: MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note	
BA1:BA0	00 = MPR0	PPR	RFU	RTT_WR	Temperature Sensor Status(Table 1)		CRC Write Enable	Rtt_WR		read-only	
		-	-	MR2	-	-	MR2	MR2			
		-	-	A11	-	-	A12	A10	A9		
	01 = MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down Enable		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency				CAS Write Latency					
		MR0				MR2					
		A6	A5	A4	A2	A12	A5	A4	A3		
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance			
		MR1			MR5			MR1			
		A10	A9	A6	A8	A7	A6	A2	A1		

MR bit for Temperature Sensor Readout

MR3 bit A5=1 : DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3).

Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2* tREFI)
1	1	rsvd

MPR page3 (Vendor use only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	

Note 1: MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific

MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	PPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self Refresh Abort	0 = Disable 1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 100 = 6 001 = 3 101 = 8 010 = 4 110 = Reserved 011 = 5 111 = Reserved (See Table 11)
A5	RFU	0 = must be programmed to 0 during MRS
A4	Internal Vref Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

Note 1: Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable 1 = Enable
A8:A6	RTT_PARK	(see Table 12)
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	(see Table 13)

Note 1: Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Note 2: When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600,1866,2133
0	1	0	5	2400
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Note 1: Parity latency must be programmed according to timing parameters by speed grade table.

MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	(see Table 14)
A9, A8	RFU	0 = must be programmed to 0 during MRS
A7	VrefDQ Training Enable	0 = Disable(Normal operation Mode) 1 = Enable(Training Mode)
A6	VrefDQ Training Range	(see Table 15)
A5:A0	VrefDQ Training Value	(see Table 16)

Note 1: Reserved for Register control word setting . DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond.

tCCD_L & tDLLK

A12	A11	A10	tCCD_L.min (nCK) ¹	tDLLKmin (nCK) ¹	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	≤ TBD
1	0	0	8		≤ TBD
1	0	1	Reserved		
1	1	0			
1	1	1			

Note 1: tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency.

VrefDQ Training : Range

A6	VrefDQ Range
0	Range 1
1	Range 2

VrefDQ Training : Values

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	-75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111	Reserved	Reserved

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^N tCK(abs)_j \right) / N \quad N = 200$$

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^N tCH_j \right) / \{N \times tCK(avg)\} \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^N tCL_j \right) / \{N \times tCK(avg)\} \quad N = 200$$

Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

Timing Parameters by Speed Grade

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	20	8	20	8	20	ns	22
Average Clock Period	tCK(avg)	0.833	<0.937	0.750	<0.833	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	$tCK(avg)_{min} + tJIT(per)_{min_tot}$ $tCK(avg)_{max} + tJIT(per)_{max_tot}$						tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-42	42	-38	38	-32	32	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-19	19	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-30	30	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	83	-	75	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	67	-	60	-	50	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-61	61	-55	55	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-73	73	-66	66	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	-73	73	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	-78	78	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	-83	83	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	-87	87	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	-91	91	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	-94	94	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	-96	96	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	-99	99	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	-101	101	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	-103	103	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	-104	104	-87	87	ps	
Cumulative error across 15 cycles	tERR(15per)	-118	118	-106	106	-89	89	ps	
Cumulative error across 16 cycles	tERR(16per)	-120	120	-108	108	-90	90	ps	
Cumulative error across 17 cycles	tERR(17per)	-122	122	-110	110	-92	92	ps	
Cumulative error across 18 cycles	tERR(18per)	-124	124	-112	112	-93	93	ps	
Cumulative error across n = 13, ... 49, 50 cycles	tERR(nper)	$tERR(nper)_{min} = ((1 + 0.68\ln(n)) * tJIT(per)_{total\ min})$ $tERR(nper)_{max} = ((1 + 0.68\ln(n)) * tJIT(per)_{total\ max})$						ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	55	-	40	-	ps	

Command and Address setup time to CK _t , CK _c referenced to Vref levels	tIS(Vref)	162	-	145	-	130	-	ps	
Command and Address hold time to CK _t , CK _c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	80	-	65	-	ps	
Command and Address hold time to CK _t , CK _c referenced to Vref levels	tIH(Vref)	162	-	145	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	410	-	385	-	340	-	ps	
Command and Address Timing									
CAS _n to CAS _n command delay for same bank group	tCCD_L	Max(5nC K,5ns)	-	Max(5nC K,5ns)	-	Max(5nC K,5ns)	-	nCK	34
CAS _n to CAS _n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nC K,3.3ns)	-	Max(4nC K,3ns)	-	Max(4nC K,2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nC K,3.3ns)	-	Max(4nC K,3ns)	-	Max(4nC K,2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	nCK	34

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nC K,4.9ns)		Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nC K,4.9ns)		Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	nCK	34
Four activate window for 2KB pagesize	tFAW_2K	Max(28n CK,30ns)		Max(28n CK,30ns)	-	Max(28n CK,30ns)	-	ns	34
Four activate window for 1KB pagesize	tFAW_1K	Max(20n CK,21ns)		Max(20n CK,21ns)	-	Max(20n CK,21ns)	-	ns	34
Four activate window for 1/2KB pagesize	tFAW_1/2K	Max(16n CK,13ns)		Max(16n CK,12ns)	-	Max(16n CK,10ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	ns	1,2,34
Delay from start of internal write transaction to	tWTR_L	max	-	max	-	max	-	ns	1,34

internal read command for same bank group		(4nCK,7.5ns)		(4nCK,7.5ns)		(4nCK,7.5ns)			
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	ns	
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	ns	1,28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	ns	2,29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	768	-	1024	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	nCK	
Multi-Purpose Register RecoveryTime	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
CS_n to Command AddressLatency									
CS_n to Command AddressLatency	tCAL	max(3nCK,3.748ns)	-	max(3nCK,3.748ns)	-	max(3nCK,3.748ns)	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.17	-	0.19	tCK(avg)/2	13,18
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.74	-	0.74	-	0.70	-	tCK(avg)/2	13,17,18
Data Strobe Timing									
DQS_t, DQS_c differential READPre-amble (2 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	tCK	
DQS_t, DQS_c differential READPostamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t, DQS_c differential output lowtime	tQSL	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-330	175	-310	170	-250	160	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	-	170	-	160	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-		
CS setup time to CE	tMPX_S	tIS(min)+tIHL(min)	-	tIS(min)+tIHL(min)	-	tIS(min)+tIHL(min)	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	

Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tR FC(min)+ 10ns)	-	max (5nCK,tR FC(min)+ 10ns)	-	max (5nCK,tR FC(min)+ 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min) + 10ns	-	tRFC(min) + 10ns	-	tRFC(min) + 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX- S_ABORT(mi n)	tRFC4(mi n) + 10ns	-	tRFC4(mi n) + 10ns	-	tRFC4(mi n) + 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(mi n) + 10ns	-	tRFC4(mi n) + 10ns	-	tRFC4(mi n) + 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(mi n)	-	tDLLK(mi n)	-	tDLLK(mi n)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nC K,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10 ns)	-	nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nC K,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10 ns)	-	nCK	
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6n s)	-	max (4nCK,6n s)	-	max (4nCK,6n s)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disabled delay	tCPDED	4	-	4	-	4	-	nCK	

Power Down Entry to Exit Timing	tPD	tCKE(min))	9*tREFI	tCKE(min))	9*tREFI	tCKE(min))	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(t WR/ tCK(avg))	-	WL+4+(t WR/ tCK(avg))	-	WL+4+(t WR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+W R+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP- BC4DEN	WL+2+(t WR/ tCK(avg))	-	WL+2+(t WR/ tCK(avg))	-	WL+2+(t WR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP- BC4DEN	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+W R+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16n CK,10ns)	-	max(16n CK,10ns)	-	max(16n CK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		-	
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.28	0.72	0.26	0.74	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	

Write leveling outputdelay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling outputerror	tWLOE	0	2	0	2	0	2	ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UN- KNOWN	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT _ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT _PW	72	144	80	160	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT _RSP	-	64	-	71	-	85	nCK	
Parity Latency	PL	5		5		6		nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
CRC Error Reporting									
CRC error toALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_ PW	6	10	6	10	6	10	nCK	
tREFI									
tRFC1 (min)	8Gb	350	-	350	-	350	-	ns	34
tRFC2 (min)	8Gb	260	-	260	-	260	-	ns	34
tRFC4 (min)	8Gb	160	-	160	-	160	-	ns	34

Note :

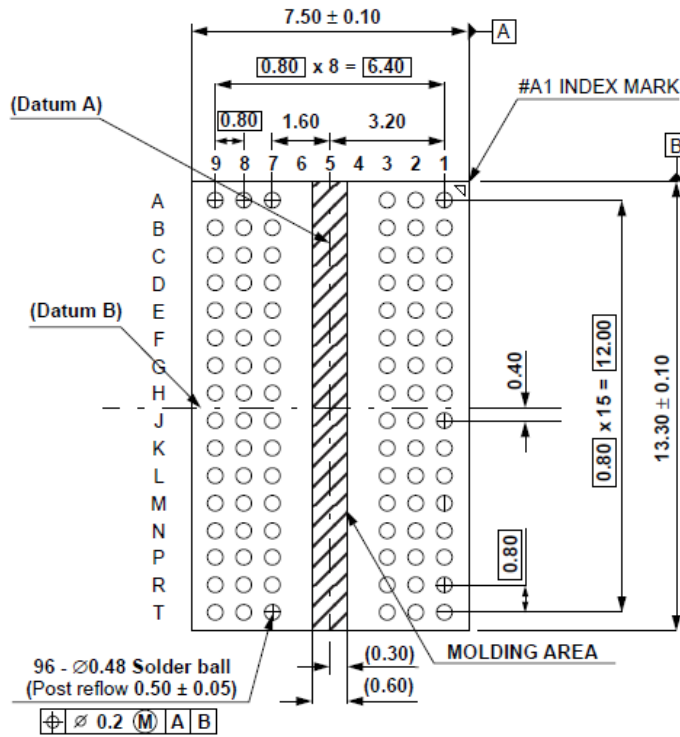
- Start of internal write transaction is defined as follows :
 - For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
 - For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
 - For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
- A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
- Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
- tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
- WR in clock cycles as programmed in MR0.
- tREFI depends on TOPER.
- CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
- For these parameters, the DDR4 SDRAM device supports $t_{nPARAM}[nCK]=RU\{t_{PARAM}[ns]/t_{CK}(avg)[ns]\}$, which is in clock cycles assuming all input clock jitter specifications are satisfied
- When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
- When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
- When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
- The max values are system dependent.

13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $t_{jit(per)}_{total}$ of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. $UI=tCK(avg).min/2$

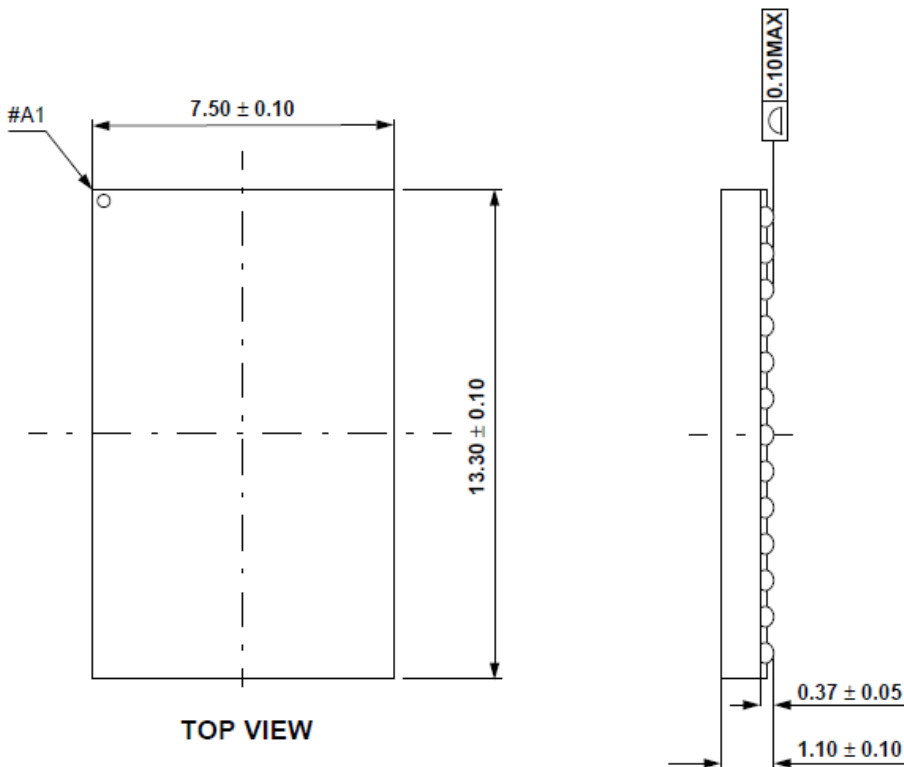
Package Description: 96Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Units : Millimeters



BOTTOM VIEW



TOP VIEW

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2021	Rico Yang	N/A
1.0	First SPEC. release.	Aug. 2021	Rico Yang	N/A