64Gb (256Mx8Banks×32)
Low Power DDR4 SDRAM

Descriptions

H2AB64G32E6R uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. Each command uses one clock cycle,during which command information is transferred on both the positive and negative edge of the clock. To achieve high-speed operation,our H2AB64G32E6R SDRAM adopt 16n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the H2AB64G32E6R effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal SDRAM core and eight corresponding n-bit wide,one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the H2AB64G32E6R are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For H2AB64G32E6R devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

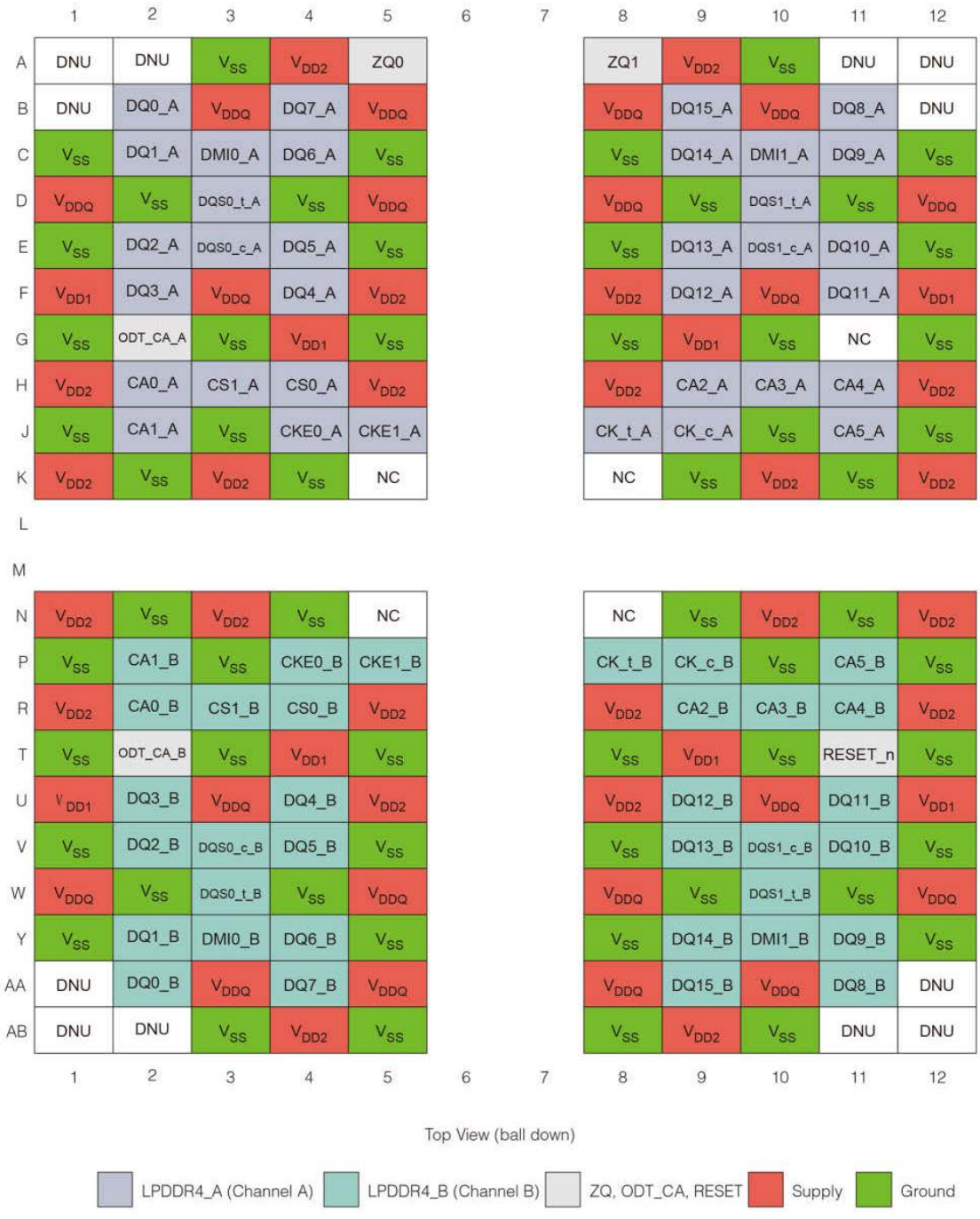
Features

- Frequency to 2133MHz (data rate: 4266Mbps/pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable Burst Lengths: 16,32
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock Stop capability during idle period
- RoHS-compliant, “green” packaging
- Programmable VSS (ODT) termination
- Auto Refresh and Self Refresh Modes
- FBGA “green” package - 200-ball VFBGA
- Operating temperature range：
  Single Low：-30˚C to 85˚C
  Commercial：0˚C to 85˚C
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- VDD1/VDD2/VDDQ= 1.8V/1.1V/1.1V or 0.6V

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2AB64G32E6RQAAC	2048M X 32	LP DDR4-4266	200Ball BGA,10x14.5mm	Commercial
H2AB64G32E6RQAASL	2048M X 32	LP DDR4-4266		Single Low

Pin Assignment



200-Ball FBGA

Pin Description (Simplified)

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE1_A, CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B, CS1_B	Input	Chip select: Each rank (0,1) in each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT control: LPDDR4X: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level. LPDDR4: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to VSS (or left floating with a weak pull- down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI),the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its Own DMI signals.

ZQ0, ZQ1	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V_{SS}	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	-	Do not use: Must be grounded or left floating.
NC	-	No connect: Not internally connected.

SDRAM Addressing

Configuration			2048Meg x 32 〈 64Gb/Package 〉
Die Configuration	Channel A, Rank 0		x16 mode x 1 die
	Channel B, Rank 0		x16 mode x 1 die
	Channel A, Rank 1		x16 mode x 1 die
	Channel B, Rank 1		x16 mode x 1 die
Die Addressing	Device density (per die)		16Gb
	Device density (per channel)		16Gb
	Configuration(per die)		128Mb × 16 DQ × 8 banks
	Number of channels (per die)		1
	Number of banks (per channel)		8
	Array prefetch (bits, per channel)		256
	Number of rows (per channel)		131,072
	Number of columns (fetch boundaries)		64
	Page size (bytes)		2048
	Channel density (bits per channel)		17,179,869,184
	Total density (bits per die)		17,179,869,184
	Bank address		BA[2:0]
	x16	Row address	R[16:0]
		Column address	C[9:0]
	Burst starting address boundary		64-bit

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Voltage on any ball relative to VSS	-0.4 ~ 1.5	V
V_{DD1}	VDD1 supply voltage relative to VSS	-0.4 ~ 2.1	V
V_{DD2}	VDD2 supply voltage relative to VSS	-0.4 ~ 1.5	V
V_{DDQ}	VDDQ supply voltage relative to VSS	-0.4 ~ 1.5	V
T_{STG}	Storage Temperature (plastic)	-55 ~ 125	˚C

Note 1: For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.

Note 2: Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Units
C_{CK}	Input capacitance, CK_t and CK_c	0.5	0.9	pF
C_{DCK}	Input capacitance delta, CK_t and CK_c	0	0.09	pF
C_{I}	I Input capacitance, all other input-only pins	0.5	0.9	pF
C_{DI}	Input capacitance delta, all other input-only pins	-0.1	0.1	pF
C_{IO}	Input/output capacitance, DQ, DMI, DQS_t, DQS_c	0.7	1.3	pF
C_{DDQS}	Input/output capacitance delta, DQS_t, DQS_c	0	0.1	pF
C_{DIO}	Input/output capacitance delta, DQ, DMI	-0.1	0.1	pF
C_{ZQ}	Input/output capacitance, ZQ pin	0	5.0	pF

Note 1: This parameter is not subject to production testing. It is verified by design and characterization.

Note 2: This parameter is not subject to production test. It is verified. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSS, VSS applied and all other pins floating.

Note 3: Absolute value of CKCK_t – CKCK_c

Note 4: CI applies to CS, CKE and CA[5:0].

Note 5: CDI = CI – 0.5 × (CCK_t + CKCK_c); it does not apply to CKE.

Note 6: DMI loading matches DQ and DQS.

Note 7: Absolute value of CDQS_t and CDQS_c.

Note 8: CDIO = CIO – Average(CDQn, CDMI, CDQS_t, CDQS_c) in byte-lane

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V
V_{DD2}	Core Supply voltage 2	1.06	1.10	1.17	V
V_{DDQ}	I/O buffer power	0.57	0.6	0.65	V

Notes: 1. VDD1 uses significantly less power than VDD2.

Notes: 2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

Notes: 3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VREF(CA),max_r0	VREF(CA) range-0 MAX operating point	-	-	30%	VDD2	1,11
VREF(CA),min_r0	VREF(CA) range-0 MIN operating point	10%	-	-	VDD2	1,11
VREF(CA),max_r1	VREF(CA) range-1 MAX operating point	-	-	42%	VDD2	1,11
VREF(CA),min_r1	VREF(CA) range-1 MIN operating point	22%	-	-	VDD2	1,11
VREF(CA),step	VREF(CA) step size	0.30%	0.40%	0.50%	VDD2	2
VREF(CA),set_tol	VREF(CA) set tolerance	–1.00%	0.00%	1.00%	VDD2	3,4,6
		–0.10%	0.00%	0.10%	VDD2	3,5,7
tVREF_TIME-SHORT	VREF(CA) step time	-	-	100	ns	8
tVREF_TIME-MIDDLE		-	-	200	ns	12
tVREF_TIME-LONG		-	-	500	ns	9
tVREF_time_weak		-	-	1	ms	13,14
VREF(CA)_val_tol	VREF(CA) valid tolerance	–0.10%	0.00%	0.10%	VDD2	10

Notes:

1. VREF(CA) DC voltage referenced to VDD2(DC).
2. VREF(CA) step size increment/decrement range. VREF(CA) at DC level.
3. VREF(CA),new = VREF(CA),old + n × VREF(CA),step; n = number of steps; if increment, use "+"; if decrement, use "-".
4. The minimum value of VREF(CA) setting tolerance = VREF(CA),new - 1.0% × VDD2. The maximum value of VREF(CA) setting tolerance = VREF(CA),new + 1.0% × VDD2. For n > 4.
5. The minimum value of VREF(CA) setting tolerance = VREF(CA),new - 0.10% × VDD2. The maximum value of VREF(CA) setting tolerance = VREF(CA),new + 0.10% × VDD2. For n < 4.
6. Measured by recording the minimum and maximum values of the VREF(CA) output over the range, drawing a straight line between those points and comparing all other VREF(CA) output settings to that line.
7. Measured by recording the minimum and maximum values of the VREF(CA) output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other VREF(CA) output settings to that line.
8. Time from MRW command to increment or decrement one step size for VREF(CA) .
9. Time from MRW command to increment or decrement VREF,min to VREF,max or VREF,max to VREF,min change across the VREF(CA) range in VREF voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
11. DRAM range-0 or range-1 set by MR12 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREF(CA) range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
14. tVREF_time_weak covers all VREF(CA) range and value change conditions are applied to tVREF_TIME-SHORT/MIDDLE/LONG.

IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Current	Notes
Operating one bank active-precharge current: tCK=tCK(MIN); tRC=tRC(MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD01	VDD1	TBD	
	IDD02	VDD2	TBD	
	IDD0Q	VDDQ	TBD	
Idle power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2P1	VDD1	TBD	
	IDD2P2	VDD2	TBD	
	IDD2PQ	VDDQ	TBD	
Idle power-down standby current with clock stop: CK_t =LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2PS1	VDD1	TBD	
	IDD2PS2	VDD2	TBD	
	IDD2PSQ	VDDQ	TBD	
Idle non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2N1	VDD1	TBD	
	IDD2N2	VDD2	TBD	
	IDD2NQ	VDDQ	TBD	
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2NS1	VDD1	TBD	
	IDD2NS2	VDD2	TBD	
	IDD2NSQ	VDDQ	TBD	
Active power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus	IDD3P1	VDD1	TBD	
	IDD3P2	VDD2	TBD	

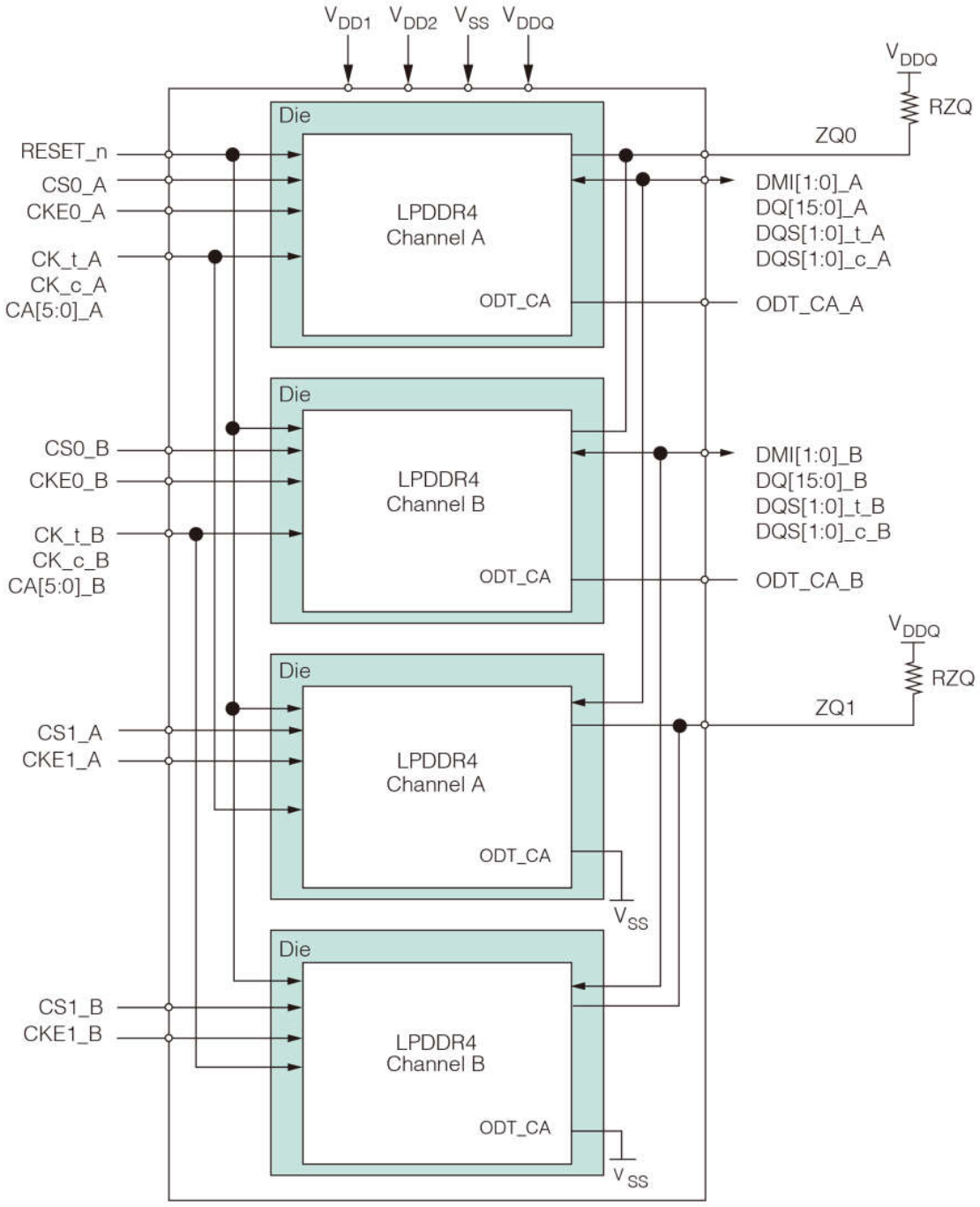
inputs are switching;Data bus inputs are stable; ODT is disabled	IDD3PQ	VDDQ	TBD	
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3PS1	VDD1	TBD	
	IDD3PS2	VDD2	TBD	
	IDD3PSQ	VDDQ	TBD	
Active non-power-down standby current: tCK = tCK (MIN);CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3N1	VDD1	TBD	
	IDD3N2	VDD2	TBD	
	IDD3NQ	VDDQ	TBD	
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3NS1	VDD1	TBD	
	IDD3NS2	VDD2	TBD	
	IDD3NSQ	VDDQ	TBD	

Parameter/Condition	Symbol	Power Supply	Current	Notes
Operating burst READ current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN);CA bus inputs are switching; 50% data change each burst transfer;ODT is disabled	IDD4R1	VDD1	TBD	
	IDD4R2	VDD2	TBD	
	IDD4RQ	VDDQ	TBD	
Operating burst WRITE current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL =WL(MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4W1	VDD1	TBD	
	IDD4W2	VDD2	TBD	
	IDD4WQ	VDDQ	TBD	
All-bank REFRESH burst current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tRFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD51	VDD1	TBD	
	IDD52	VDD2	TBD	
	IDD5Q	VDDQ	TBD	

All-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5AB1	VDD1	TBD	
	IDD5AB2	VDD2	TBD	
	IDD5ABQ	VDDQ	TBD	
Per-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands tRC = Trefi/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5PB1	VDD1	TBD	
	IDD5PB2	VDD2	TBD	
	IDD5PBQ	VDDQ	TBD	
Power-down self refresh current: CK_t = LOW, CK_c = HIGH;CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled(25℃)	IDD61	VDD1	TBD	
	IDD62	VDD2	TBD	
	IDD6Q	VDDQ	TBD	

Notes:
1.Published IDD values except IDD4RQ are the maximum of the distribution of the arithmeticmean. Refer to the following note for IDD4RQ;.
2.IDD4RQ value is reference only. Typical value. DBI disabled, VOH = VDDQ/3, TC = 25°C.
3.Measurement conditions of IDD4R and IDD4W values: DBI disabled, BL = 16.

Package Block Diagram –Quad-Die, Dual-Channel



Initialization Timing Parameters

Parameter	Min.	Max.	Unit	Comment
tINIT0	-	20	ms	Maximum voltage ramp time
tINIT1	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2	-	ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5	-	tCK	Minimum stable clock before first CKE HIGH
tINIT5	2	-	us	Minimum idle time before first MRW/MRR command
tCKb	Note 1, 2		ns	Clock cycle time during boot

Notes: 1. Minimum tCKb guaranteed by DRAM test is 18ns.

Notes: 2. The system may boot at a higher frequency than dictated by minimum tCKb. The higher boot frequency is system dependent.

AC Characteristics

Clock Timing

Symbol	Parameter	Min/Max	Data Rate		Unit
			3733	4266	
$t_{CK(avg)}$	Average clock period	Min	535	468	ps
		Max	100	100	ns
$t_{CH(avg)}$	Average HIGH pulse width	Min	0.46	0.46	$t_{CK(avg)}$
		Max	0.54	0.54	$t_{CK(avg)}$
$t_{CL(avg)}$	Average LOW pulse width	Min	0.46	0.46	$t_{CK(avg)}$
		Max	0.54	0.54	$t_{CK(avg)}$
$t_{CK(abs)}$	Absolute clock period	Min	$t_{CK(avg)}$ MIN + $t_{JIT(per)}$ MIN		ps
$t_{CH(abs)}$	Absolute clock HIGH pulse width	Min	0.43	0.43	$t_{CK(avg)}$
		Max	0.57	0.57	$t_{CK(avg)}$
$t_{CL(abs)}$	Absolute clock LOW pulse width	Min	0.43	0.43	$t_{CK(avg)}$
		Max	0.57	0.57	$t_{CK(avg)}$
$t_{JIT(per)}$, allowed	Clock period jitter	Min	-34	-30	ps
		Max	34	30	ps
$t_{JIT(cc)}$, allowed	Maximum clock jitter between two consecutive clock cycles (with clock period jitter)	Max	68	68	ps

Read Output Timing

Symbol	Parameter	Min/ Max	Data Rate		Unit
			3733	4266	
tDQSCK	DQS output access time from CK	Min	1500		ps
		Max	3500		ps
tDQSCK_ VOLT	DQS output access time from CK_t/CK_c – voltage variation	Max	7		ps/mV
tDQSCK_ TEMP	DQS output access time from CK_t/CK_c – temperature variation	Max	4		ps°/C
tDQSCK_r ank2rank	CK to DQS rank to rank variation	Max	1.0		ns
tDQSQ	DQS-DQ skew	Max	0.18		UI
tQH	DQ output hold time total from DQS_t, DQS_c	Min	Min (tQSH, tQSL)		ps
tRPRE	READ preamble	Min	1.8		tCK(avg)
tRPST	READ postamble	Min	0.4		tCK(avg)
tLZ(DQS)	DQS Low-Z from clock	Min	(RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200ps		ps
tLZ(DQ)	DQ Low-Z from clock	Min	(RL x tCK) + tDQSCK(Min) - 200ps		ps
tHZ(DQS)	DQS High-Z from clock	Min	(RL x tCK) + tDQSCK(Max)+(BL/2 x tCK) + (tRPST(Max) x tCK) - 100ps		ps
tHZ(DQ)	DQ High-Z from clock	Max	t(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps		ps
tQW_total	Data output valid window time total, per pin	Min	0.70	0.70	UI
tDQSQ_DBI	DQS_t, DQS_c to DQ skew total, per group, per access	Max	0.18		UI
tQH_DBI	DQ output hold time total from DQS_t, DQS_c	Min	MIN(tQSH_DBI, tQSL_DBI)		ps
tQW_total_DBI	Data output valid window time total, per pin	Min	0.70	0.70	UI
tQSL	DQS_t, DQS_c differential output LOW time	Min	tCL(abs) – 0.05		tCK(avg)
tQSH	DQS_t, DQS_c differential output HIGH time	Min	tCH(abs) – 0.05		tCK(avg)
tQSL-DBI	DQS_t, DQS_c differential output LOW time	Min	tCL(abs) – 0.045		tCK(avg)
tQSH-DBI	DQS_t, DQS_c differential output HIGH time	Min	tCH(abs) – 0.045		tCK(avg)

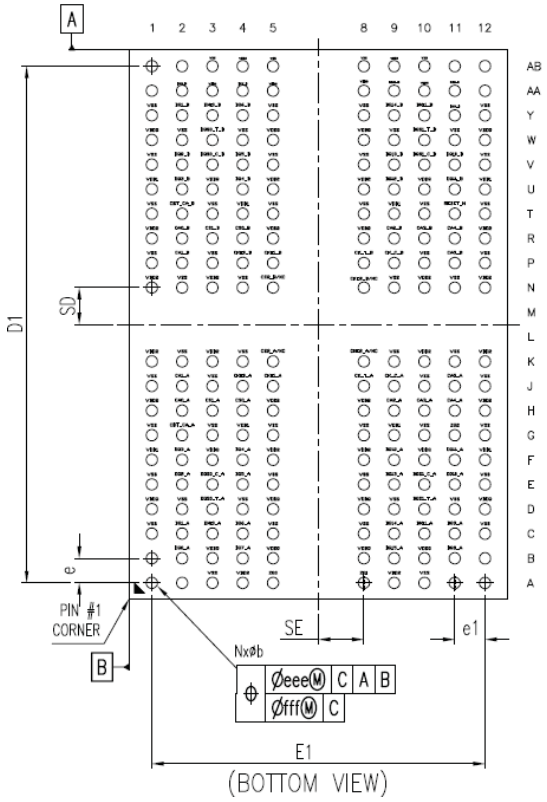
Write Timing

Note UI = tCK(AVG)(MIN)/2

Symbol	Parameter	3733/4266		Unit
		Min	Max	
TdIVW_total	Rx timing window total at VdIVW voltage levels	-	0.25	UI
TdIVW_1-bit	Rx timing window 1-bit toggle (at VdIVW voltage levels)	-	TBD	UI
TdIPW	DQ and DMI input pulse width (at VCENT_DQ)	0.45	-	UI
tDQS2DQ	tDQS2DQ	200	800	ps
tDQDQ	DQ-to-DQ offset	-	30	ps
tDQS2DQ _temp	DQ-to-DQS offset temperature variation	-	0.6	ps/°C
tDQS2DQ _volt	DQ-to-DQS offset voltage variation	-	33	Ps/50mV
t DQS2DQ _rank2ran k	DQ-to-DQS offset rank to rank variation	-	200	Ps
tDQSS	WRITE command to first DQS transition	0.75	1.25	tCK(avg)
tDQSH	DQS input HIGH-level width	0.4	-	tCK(avg)
tDQSL	DQS input LOW-level width	0.4	-	tCK(avg)
tDSS	DQS falling edge to CK setup time	0.2	-	tCK(avg)
tDSH	DQS falling edge from CK hold time	0.2	-	tCK(avg)
tWPST	Write postamble	0.4	-	tCK(avg)
tWPRE	Write preamble	1.8	-	tCK(avg)

Package Description

200-ball FBGA 10x14.5mm



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	0.97	1.04	0.035	0.038	0.041
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.69	0.76	0.83	0.027	0.030	0.033
b	0.25	0.30	0.35	0.010	0.012	0.014
D	14.40	14.50	14.60	0.567	0.571	0.575
E	9.90	10.00	10.10	0.390	0.394	0.398
e	0.65 BSC.			0.026 BSC.		
e1	0.80 BSC.			0.031 BSC.		
JEDEC	MO-311(REF.)/MM					
aaa	0.10					
bbb	0.10					
ddd	0.09					
eee	0.15					
fff	0.08					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
200	1.20 BSC.	0.975 BSC.	8.80 BSC.	13.65 BSC.

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Feb. 2020	Rico Yang	N/A
1.0	First SPEC. release.	May. 2020	Rico Yang	N/A