32Gb (128M×8Banks×32) Low Power DDR4 SDRAM

Descriptions

H2AB32G32E6R uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. Each command uses one clock cycle,during which command information is transferred on both the positive and negative edge of the clock. To achieve high-speed operation,our H2AB32G32E6R SDRAM adopt 16n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the H2AB32G32E6R effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal SDRAM core and eight corresponding n-bit wide,one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the H2AB32G32E6R are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.
For H2AB32G32E6R devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Features

- Frequency to 1866MHz (data rate: 3733Mbps/pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable Burst Lengths: 16,32
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock Stop capability during idle period
- RoHS-compliant, “green” packaging
- Programmable VSS (ODT) termination
- Auto Refresh and Self Refresh Modes
- FBGA “green” package - 200-ball VFBGA
- Operating temperature range：
  Single Low：-30°C to 85°C
  Commercial：0°C to 85°C
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- VDD1/VDD2/VDDQ= 1.8V/1.1V/1.1V or 0.6V

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2AB32G32E6RPAAC	1024M X 32	LP DDR4-3733	200Ball	Commercial
H2AB32G32E6RPAASL	1024M X 32	LP DDR4-3733	BGA,10x14.5mm	Single Low

Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			NC	V_{DD2}	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	V_{SS}	CKE0_A	NC			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	NC			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	NC	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_c_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_c_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_t_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	DNU	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

200-Ball FBGA

Pin Description (Simplified)

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A , CKE0_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled on the rising edge of CK.
CS0_A, CS0_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the Command Truth Table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT control: LPDDR4X: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level. LPDDR4: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to VSS (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B , DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A , DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual-use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command. The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	—	Do not use: Must be grounded or left floating.
NC	—	No connect: Not internally connected.

SDRAM Addressing

Configuration（32Gb/Package）			1Gig x 32
Die Configuration (for package)	Channel A, Rank 0		x 16 mode x 1 die
	Channel B, Rank 0		x 16 mode x 1 die
	Channel A, Rank 1		——
	Channel B, Rank 1		——
Die Addressing	Device density (per die)		16Gb
	Device density (per channel)		16Gb
	Configuration(per die)		128Mb × 16 DQ × 8 banks × 1 channel
	Number of channels (per die)		1
	Number of banks (per channel)		8
	Array pre-fetch (bits, per channel)		256
	Number of rows (per channel)		131,072
	Number of columns (fetch boundaries)		64
	Page size (bytes)		2048
	Channel density (bits per channel)		17,179,869,184
	Total density (bits per die)		17,179,869,184
	Bank address		BA[2:0]
	x 16	Row address	R[16:0]
		Column address	C[9:0]
	Burst starting address boundary		64-bit

Mode Registers

MR5 Basic Configuration 1 (MA[5:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b : Micron

MR8 Basic Configuration 4 (MA[5:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S16 SDRAM (16n-prefetch)
Density	Read-only	OP[5:2]	0110b: 32Gb dual-channel die/16Gb single-channel die
I/O width	Read-only	OP[7:6]	00b: x16/channel

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Voltage on any ball relative to VSS	-0.4 ~ 1.5	V
V_{DD1}	VDD1 supply voltage relative to VSS	-0.4 ~ 2.1	V
V_{DD2}	VDD2 supply voltage relative to VSS	-0.4 ~ 1.5	V
V_{DDQ}	VDDQ supply voltage relative to VSS	-0.4 ~ 1.5	V
T_{STG}	Storage Temperature (plastic)	-55 ~ 125	˚C

Note 1: For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.

Note 2: Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Units
C_{CK}	Input capacitance, CK_t and CK_c	0.5	0.9	pF
C_{DCK}	Input capacitance delta, CK_t and CK_c	0	0.09	pF
C_{I}	I Input capacitance, all other input-only pins	0.5	0.9	pF
C_{DI}	Input capacitance delta, all other input-only pins	-0.1	0.1	pF
C_{IO}	Input/output capacitance, DQ, DMI, DQS_t, DQS_c	0.7	1.3	pF
C_{DDQS}	Input/output capacitance delta, DQS_t, DQS_c	0	0.1	pF
C_{DIO}	Input/output capacitance delta, DQ, DMI	-0.1	0.1	pF
C_{ZQ}	Input/output capacitance, ZQ pin	0	5.0	pF

Note 1: This parameter is not subject to production testing. It is verified by design and characterization.
Note 2: Absolute value of CKCK_t – CKCK_c
Note 3: CI applies to CS, CKE and CA[5:0].
Note 4: CDI = CI – 0.5 × (CCK_t + CKCK_c); it does not apply to CKE.
Note 5: DMI loading matches DQ and DQS.
Note 6: Absolute value of CDQS_t and CDQS_c.
Note 7: CDIO = CIO – Average(CDQn, CDMI, CDQS_t, CDQS_c) in byte-lane

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V
V_{DD2}	Core Supply voltage 2	1.06	1.10	1.17	V
V_{DDQ}	I/O buffer power	0.57/1.06	0.6/1.10	0.65/1.17	V

Notes: 1. VDD1 uses significantly less power than VDD2.
Notes: 2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
Notes: 3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: tCK=tCK(MIN); tRC=tRC(MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stopped: CK_t =LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2PS1	VDD1	
	IDD2PS2	VDD2	
	IDD2PSQ	VDDQ	3
Idle non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NSQ	VDDQ	3
Active power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3PS1	VDD1	
	IDD3PS2	VDD2	
	IDD3PSQ	VDDQ	4
Active non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Operating burst READ current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Operating burst WRITE current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL =WL(MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All-bank REFRESH burst current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tRFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4

Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5ABQ	VDDQ	4
Per-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands tRC = Trefi/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5PB1	VDD1	
	IDD5PB2	VDD2	
	IDD5PBQ	VDDQ	4
Power-down self refresh current(-30°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	IDD61	VDD1	6,7,9
	IDD62	VDD2	6,7,9
	IDD6Q	VDDQ	4,6,7,9

Notes: 1. Published IDD values are the maximum of the distribution of the arithmetic mean.

Notes: 2. ODT disabled: MR11[2:0] = 000B.

Notes: 3. IDD current specifications are tested after the device is properly initialized.

Notes: 4. Measured currents are the summation of VDDQ and VDD2.

Notes: 5. Guaranteed by design with output load = 5pF and RON = 40 Ω.

Notes: 6. The 1x Self Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self Refresh, before going into the elevated Temperature range.

Notes: 7. This is the general definition that applies to full array Self Refresh.

Notes: 8. This is the general definition that applies to full array Self Refresh.

Notes: 9. This is the general definition that applies to full array Self Refresh.

IDD Parameters – Single Die

VDD2 = 1.06–1.17V; LPDDR4X: VDDQ = 0.57–0.65V; LPDDR4: VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V; TC = –30°C to +85°C

Symbol		Supply	Speed Grade 3733Mbps		Unit
			LPDDR4X	LPDDR4	
IDD0	IDD01	VDD1	5	5	mA
	IDD02	VDD2	26	26	
	IDD0Q	VDDQ	0.75	0.75	
IDD2P	IDD2P1	VDD1	2.88	2.88	mA
	IDD2P2	VDD2	4.08	4.08	
	IDD2PQ	VDDQ	0.75	0.75	
IDD2PS	IDD2PS1	VDD1	2.88	2.88	mA
	IDD2PS2	VDD2	4.08	4.08	
	IDD2PSQ	VDDQ	0.75	0.75	
IDD2N	IDD2N1	VDD1	2.4	2.4	mA
	IDD2N2	VDD2	14	14	
	IDD2NQ	VDDQ	0.75	0.75	
IDD2NS	IDD2NS1	VDD1	2.4	2.4	mA
	IDD2NS2	VDD2	12	12	
	IDD2NSQ	VDDQ	0.75	0.75	
IDD3P	IDD3P1	VDD1	2.4	2.4	mA
	IDD3P2	VDD2	6.2	6.2	
	IDD3PQ	VDDQ	0.75	0.75	
IDD3PS	IDD3PS1	VDD1	2.4	2.4	mA
	IDD3PS2	VDD2	6.2	6.2	
	IDD3PSQ	VDDQ	0.75	0.75	
IDD3N	IDD3N1	VDD1	3.4	3.4	mA
	IDD3N2	VDD2	16	16	
	IDD3NQ	VDDQ	0.75	0.75	
IDD3NS	IDD3NS1	VDD1	3.4	3.4	mA
	IDD3NS2	VDD2	14	14	
	IDD3NSQ	VDDQ	0.75	0.75	
IDD4R	IDD4R1	VDD1	13.2	13.2	mA
	IDD4R2	VDD2	246	246	
	IDD4RQ	VDDQ	63	94	
IDD4W	IDD4W1	VDD1	13.2	13.2	mA
	IDD4W2	VDD2	192	192	
	IDD4WQ	VDDQ	0.75	0.75	

DC Characteristics(Continued)

(IDD Specifications; VDD2, VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V)

Symbol		Supply	Speed 3733Mbps		Unit
			LPDDR4X	LPDDR4	
IDD5	IDD51	VDD1	23	23	mA
	IDD52	VDD2	110	110	
	IDD5Q	VDDQ	0.75	0.75	
IDD5AB	IDD5AB1	VDD1	6.6	6.6	mA
	IDD5AB2	VDD2	24	24	
	IDD5ABQ	VDDQ	0.75	0.75	
IDD5PB	IDD5PB1	VDD1	4.8	4.8	mA
	IDD5PB2	VDD2	24	24	
	IDD5PBQ	VDDQ	0.75	0.75	

Notes: 1. Measurement conditions of IDD4R and IDD4W values: DBI disabled, BL = 16.

Notes: 2. Published IDD values except ID4RQ are the maximum of the distribution of the arithmetic mean. Refer to another note for IDD4RQ.

Notes: 3. IDD4RQ value is reference only. Typical value. DBI Disabled, VOH = 0.5 x VDDQ, Tc = 25°C

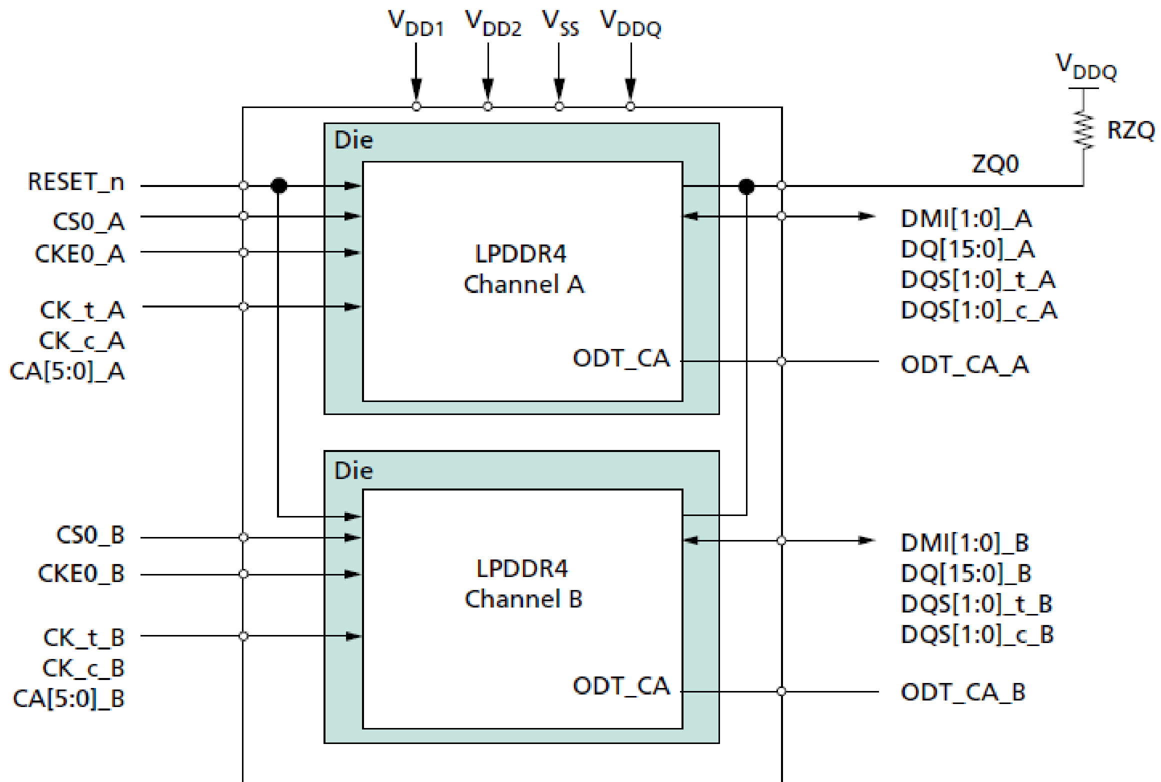
IDD6 Partial Array Self-refresh current;
VDD2,VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V; LPDDR4X:VDDQ= 0.57~0.65V

PASR	Supply	Temp.		Unit
		25°C	85°C	
Full Array(3733Mbps) LPDDR4/LPDDR4X	VDD1	0.62	5.16	mA
	VDD2	1.39	10.8	
	VDDQ	0.01	0.75	

Notes: 1. IDD values reflect dual-channel operation with the same pattern for each channel.

Notes: 2. IDD6 25°C is the typical, and IDD6 85°C is the maximum of the distribution of the arithmetic mean.

Package Block Diagram – Dual-Die, Dual-Channel



Initialization Timing Parameters

Parameter	Min.	Max.	Unit	Comment
tINIT0	-	20	ms	Maximum voltage ramp time
tINIT1	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2	-	ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5	-	tCK	Minimum stable clock before first CKE HIGH
tINIT5	2	-	us	Minimum idle time before first MRW/MRR command
tCKb	Note 1, 2		ns	Clock cycle time during boot

Notes: 1. Minimum tCKb guaranteed by DRAM test is 18ns.

Notes: 2. The system may boot at a higher frequency than dictated by minimum tCKb. The higher boot frequency is system dependent.

Refresh rate is determined by the value in MR4 OP[2:0]

Symbol	Parameter	Min/Max	Data Rate		Unit
			3200	3733	
Core Parameters					
RL-A	READ latency (DBI disabled)	Min	28	32	tCK(avg)
RL-B	READ latency (DBI enabled))	Min	32	36	tCK(avg)
WL-A	WRITE latency (Set A)	Min	14	16	tCK(avg)
WL-B	WRITE latency (Set B)	Min	26	30	tCK(avg)
tRC	ACTIVATE-to-ACTIVATE command period	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge		ns
tSR	Minimum self refresh time (entry to exit)	Min	MAX(15ns, 3nCK)		ns
tXSR	Self refresh exit to next valid command delay	Min	MAX(tRFCab + 7.5ns, 2nCK)		ns
tCCD	CAS-to-CAS delay	Min	8		tCK(avg)
tCCDMW	CAS-to-CAS delay masked write	Min	32		tCK(avg)
tRTP	Internal READ to PRECHARGE command delay	Min	Max (7.5ns, 8nCK)		ns
tRCD	RAS-to-CAS delay	Min	Max (18ns, 4nCK)		ns
tRPpb	Row precharge time (single bank)	Min	Max (18ns, 3nCK)		ns
tRPpab	Row precharge time (all banks)	Min	Max (21ns, 3nCK)		ns
tRAS	Row active time	Min	Max (42ns, 3nCK)		ns
		Max	MIN(9 × tREFI × Refresh Rate1, 70.2)		us
tWR	WRITE recovery time	Min	Max (18ns, 4nCK)		ns
tWTR	WRITE-to- READ command delay	Min	Max (10ns, 8nCK)		ns
tRRD	Active bank A to active bank B	Min	Max (10ns, 4nCK)	Max (7.5ns, 4nCK)	ns
tPPD	Precharge-to-precharge delay	Min	4		tCK(avg)
tFAW	Four-bank activate window	Min	40		ns
tESCKE	Delay from SRE command to CKE input LOW	Min	MAX(1.75ns, 3nCK)		-

Notes: 1. Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
2. Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired.

Refresh Requirement Parameters

Parameter		Symbol	Density(per channel)	Unit
			16Gb	
Refresh window (tREFW):(1 × Refresh)		tREFW	32	ms
Required number of REFRESH commands in tREFW window		R	8192	-
Average refresh interval (1 × Refresh)	REFab	tREFI	3.904	us
	REFpb	tREFIpb	488	ns
REFRESH cycle time (all banks)		tRFCab	380	ns
REFRESH cycle time (per bank)		tRFCpb	190	ns
Per bank refresh to per bank refresh time (different bank)		tPBR2PBR	90	ns

Temperature Derating Parameters

Symbol	Parameter	Min/Max	Data Rate		Unit
			3200	3733	
tDQSCKd	DQS output access time from CK_t/CK_c (derated)	Max	3600		ps
tRCDd	RAS-to-CAS delay (derated)	Min	tRCD + 1.875		ns
tRCd	ACTIVATE-to-ACTIVATE command period (same bank, derated)	Min	tRC + 3.75		ns
tRASd	Row active time (derated)	Min	tRAS + 1.875		ns
tRPd	Row precharge time (derated)	Min	tRP + 1.875		ns
tRRDd	Active bank A to active bank B (derated)	Min	tRRD + 1.875		ns

Notes: 1. Timing derating applies for operation above 85°C.

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction

Symbol	Parameter	Min/Max	notes
tCK(avg) and nCK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit tCK(avg) represents the actual clock average tCK(avg) of the input clock under operation. Unit nCK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge.tCK(avg) can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	tCK(avg) = (Σ tCKj) /N Where N = 200	
tCK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
tCH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	tCH(avg) = (Σ tCHj) /(N × tCK(avg)) Where N = 200	
tCL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	tCL(avg) =(Σ tCLj) /(N × tCK(avg)) Where N = 200	
tJIT(per)	The single-period jitter defined as the largest deviation of any signal tCK from tCK(avg).	tJIT(per) = min/max of (tCKi – tCK(avg)) Where i = 1 to 200	1
tJIT(per),act	The actual clock jitter for a given system.		
tJIT(per), allowed	The specified clock period jitter allowance.		
tJIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. tJIT(cc) defines the cycle-to-cycle jitter.	tJIT(cc) = max of (tCKi + 1 – tCKi)	1
tERR(nper)	The cumulative error across n multiple consecutive cycles from tCK(avg).	tERR(nper) = (Σ tCKj) – (n × tCK(avg))	1
tERR(nper),act	The actual clock jitter over n cycles for a given system.		
tERR(nper), allowed	The specified clock jitter allowance over n cycles.		
tERR(nper),min	The minimum tERR(nper).	tERR(nper),min = (1 + 0.68LN(n)) × tJIT(per),min	2
tERR(nper),max	The maximum tERR(nper).	tERR(nper),max = (1 + 0.68LN(n)) × tJIT(per),max	2
tJIT(duty)	Defined with absolute and average specifications for tCH and tCL, respectively.	tJIT(duty),min = MIN((tCH(abs),min – tCH(avg),min), (tCL(abs),min – tCL(avg),min)) × tCK(avg) tJIT(duty),max = MAX((tCH(abs),max – tCH(avg),max), (tCL(abs),max – tCL(avg),max)) × tCK(avg)	

Notes: 1. Not subject to production testing.

2. Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

tCK(abs), tCH(abs), and tCL(abs) Definitions

Symbol	Parameter	Minimum	Unit
tCK(abs)	Absolute clock period	tCK(avg),min + tJIT(per),min	ps
tCH(abs)	Absolute clock HIGH pulse width	tCH(avg),min + tJIT(duty),min2/tCK(avg),min	tCK(avg)
tCL(abs)	Absolute clock LOW pulse width	tCL(avg),min + tJIT(duty),min2/tCK(avg),min	tCK(avg)

Notes: 1. tCK(avg),min is expressed in ps for this table.
2. tJIT(duty),min is a negative value.

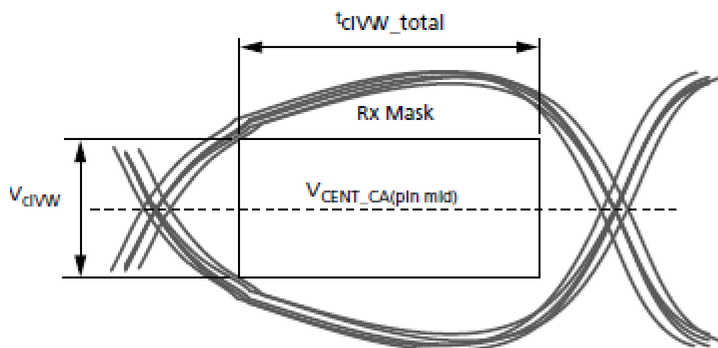
Clock AC Timing

Symbol	Parameter	Min/Max	Data Rate		Unit
			3200	3733	
tCK(avg)	Average clock period	Min	625	535	ps
		Max	100	100	ns
tCH(avg)	Average HIGH pulse width	Min	0.46	0.46	tCK(avg)
		Max	0.54	0.54	tCK(avg)
tCL(avg)	Average LOW pulse width	Min	0.46	0.46	tCK(avg)
		Max	0.54	0.54	tCK(avg)
tCK(abs)	Absolute clock period	Min	tCK(avg) MIN + tJIT(per) MIN		ps
tCH(abs)	Absolute clock HIGH pulse width	Min	0.43	0.43	tCK(avg)
		Max	0.57	0.57	tCK(avg)
tCL(abs)	Absolute clock LOW pulse width	Min	0.43	0.43	tCK(avg)
		Max	0.57	0.57	tCK(avg)
tJIT(per), allowed	Clock period jitter	Min	-40	-34	ps
		Max	40	34	ps
tJIT(cc), allowed	Maximum clock jitter between two consecutive clock cycles (with clock period jitter)	Max	80	68	ps

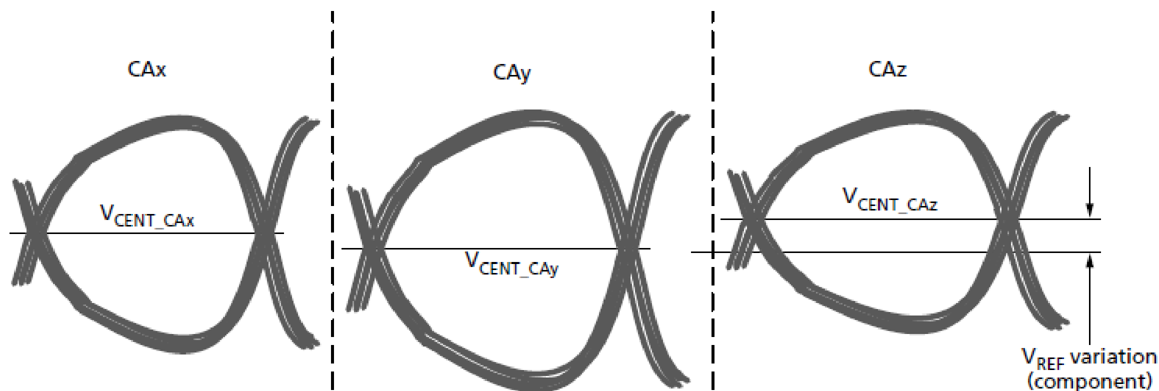
CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.
The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

CA Receiver (Rx) Mask

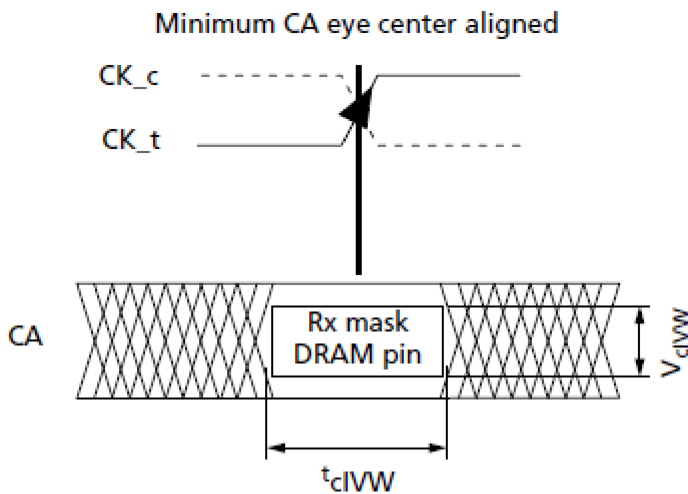


Across Pin VREF (CA) Voltage Variation



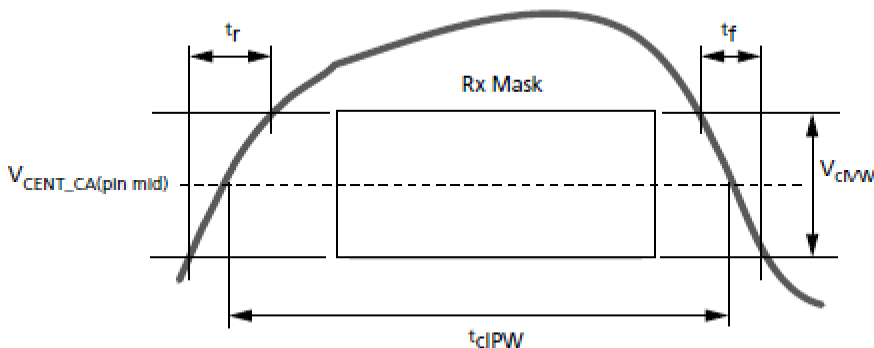
VCENT_CA(pin mid) is defined as the midpoint between the largest VCENT_CA voltage level and the smallest VCENT_CA voltage level across all CA and CS pins for a given DRAM component. Each CA VCENT level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level VREF will be set by the system to account for RON and ODT settings.

Across Pin VREF (CA) Voltage Variation



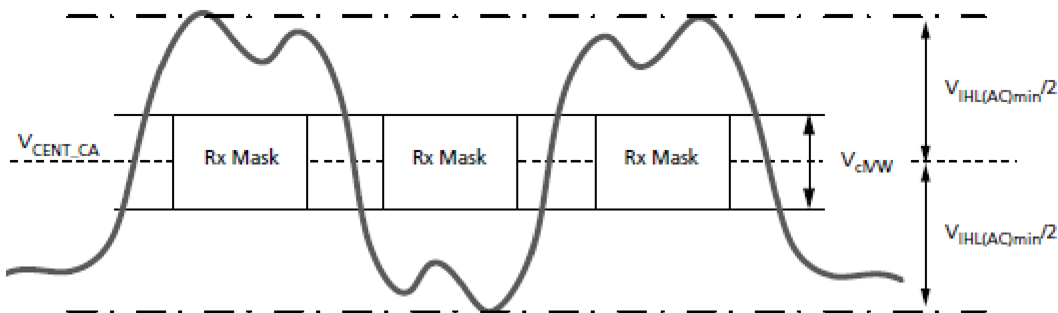
Notes: 1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around VCENT_CA(pin mid).

CA tcIPW and SRIN_cIVW Definition (for Each Input Pulse)



Notes: 1. SRIN_cIVW = VdIVW_total/(tr or tf); signal must be monotonic within tr and tf range.

CA VIHL_AC Definition (for Each Input Pulse)



DRAM CMD/ADR, CS

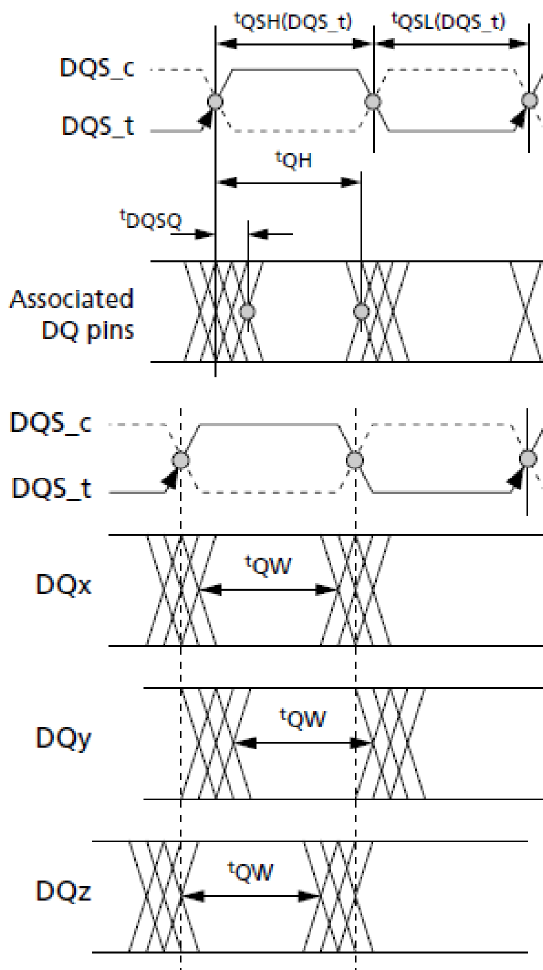
Symbol	Parameter	DQ- 3200/3733		Unit	Notes
		Min	Max		
VcIVW	Rx mask voltage peak-topeak	--	155	mV	1,2,3
TcIVW	Rx Timing Window	--	0.3	UI	1,2,3
VIHL(AC)	CA AC input pulse amplitude peak-to-peak	190	--	mV	4,7
TcIPW	CA input pulse width	0.6	--	UI	5
SRIN_cIVW	Input slew rate over VcIVW	1	7	V/ns	6

Notes: 1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.

2. Rx mask voltage VcIVW total(MAX) must be centered around VCENT_CA(pin mid).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. CA-only input pulse signal amplitude into the receiver must meet or exceed VIHL(AC) at any point over the total UI. No timing requirement above level. VIHL(AC) is the peak-topeak voltage centered around VCENT_CA(pin mid), such that VIHL(AC)/2 (MIN) must be met both above and below VCENT_CA.
5. CA only minimum input pulse with defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW mask is centered at VCENT_CA(pin mid).
7. VIHL(AC) does not have to be met when no transitions are occurring.

DQ Tx Voltage and Timing

tQH and tDQSQ Across DQ Signals per DQS Group



Read Output Timing

Symbol	Parameter	Min/ Max	Data Rate		Unit
			3200	3733	
tDQSCK	DQS output access time from CK	Min	1500		ps
		Max	3500		ps
tDQSCK_ VOLT	DQS output access time from CK_t/CK_c – voltage variation	Max	7		ps/mV
tDQSCK_ TEMP	DQS output access time from CK_t/CK_c – temperature variation	Max	4		ps°/C
tDQSCK_r ank2rank	CK to DQS rank to rank variation	Max	1.0		ns
tDQSQ	DQS-DQ skew	Max	0.18		UI
tQH	DQ output hold time total from DQS_t, DQS_c	Min	Min (tQSH, tQSL)		ps
tRPRE	READ preamble	Min	1.8		tCK(avg)
tRPST	READ postamble	Min	0.4		tCK(avg)
tLZ(DQS)	DQS Low-Z from clock	Min	(RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200ps		ps
tLZ(DQ)	DQ Low-Z from clock	Min	(RL x tCK) + tDQSCK(Min) - 200ps		ps
tHZ(DQS)	DQS High-Z from clock	Min	(RL x tCK) + tDQSCK(Max)+(BL/2 x tCK) + (tRPST(Max) x tCK) - 100ps		ps
tHZ(DQ)	DQ High-Z from clock	Max	t(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps		ps
tQW_total	Data output valid window time total, per pin	Min	0.70	0.70	UI
tDQSQ_DBI	DQS_t, DQS_c to DQ skew total, per group, per access	Max	0.18		UI
tQH_DBI	DQ output hold time total from DQS_t, DQS_c	Min	MIN(tQSH_DBI, tQSL_DBI)		ps
tQW_total_DBI	Data output valid window time total, per pin	Min	0.70	0.70	UI
tQSL	DQS_t, DQS_c differential output LOW time	Min	tCL(abs) – 0.05		tCK(avg)
tQSH	DQS_t, DQS_c differential output HIGH time	Min	tCH(abs) – 0.05		tCK(avg)
tQSL-DBI	DQS_t, DQS_c differential output LOW time	Min	tCL(abs) – 0.045		tCK(avg)
tQSH-DBI	DQS_t, DQS_c differential output HIGH time	Min	tCH(abs) – 0.045		tCK(avg)

Notes: 1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak to peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.

2. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the MAX[ABS(tDQSCK(MIN)@V1 -tDQSCK(MAX)@V2), ABS(tDQSCK(MAX)@V1 - tDQSCK(MIN)@V2)]/ABS(V1 - V2).

3. tDQSCK_temp MAX delay variation as a function of temperature.

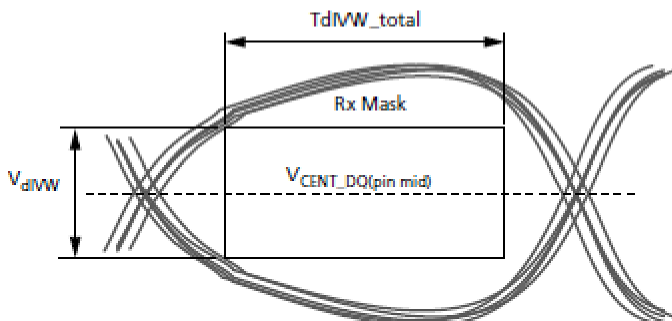
4. The same voltage and temperature are applied to tDQSCK_rank2rank.

5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c,as measured from one falling edge to the next consecutive rising edge.
10. tQSH describes the instantaneous differential output high pulse width on DQS_t -DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN tCH(ABS) and tCL(ABS). When the input clock jitter MIN tCH(ABS) and tCL(ABS) is 0.44 or greater than tCK(AVG), the minimum value of tQSL will be tCL(ABS) - 0.04 and tQSH will be tCH(ABS) -0.04.

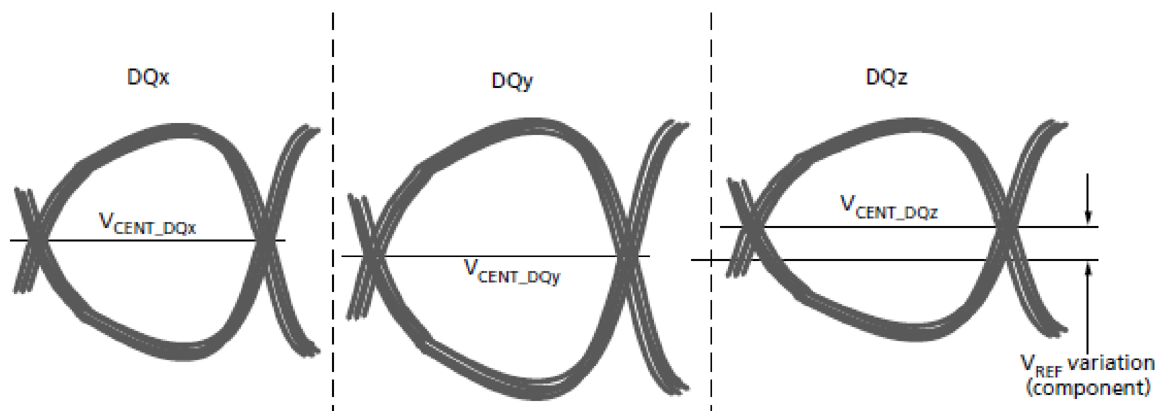
DQ Rx Voltage and Write Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask (VdIVW_total, TdIVW_total) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

DQ Receiver (Rx) Mask

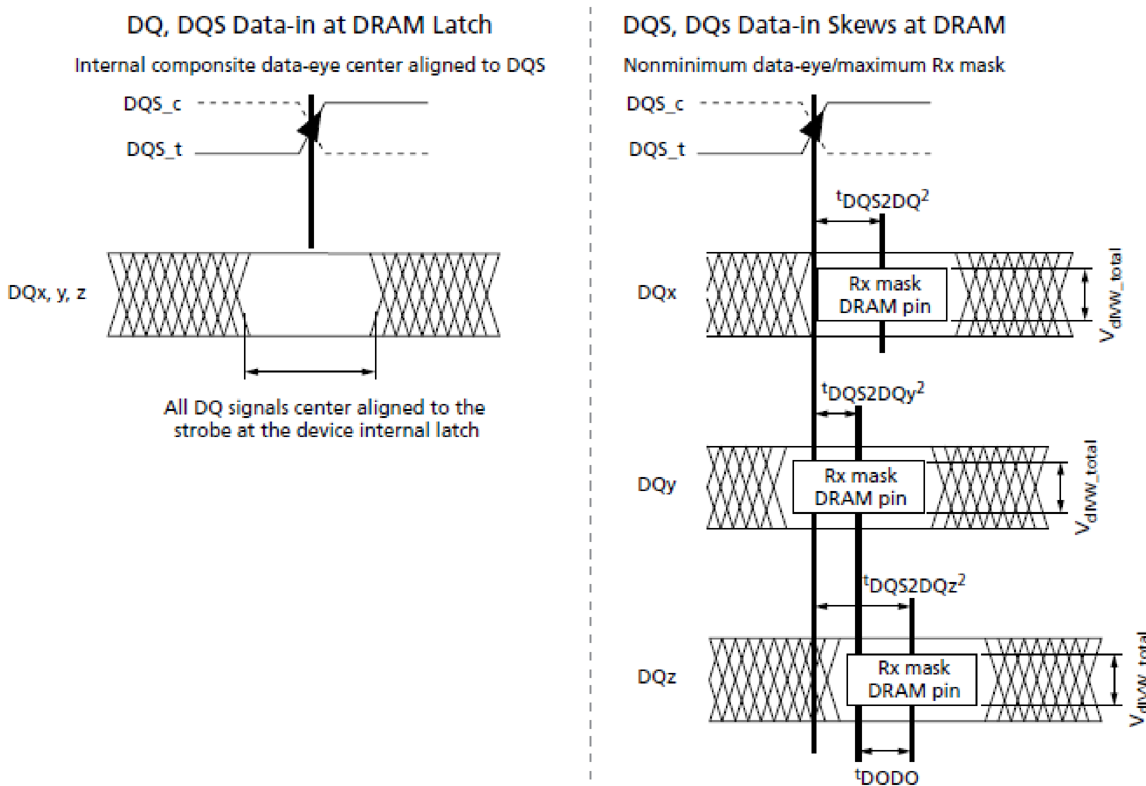


Across Pin VREF DQ Voltage Variation



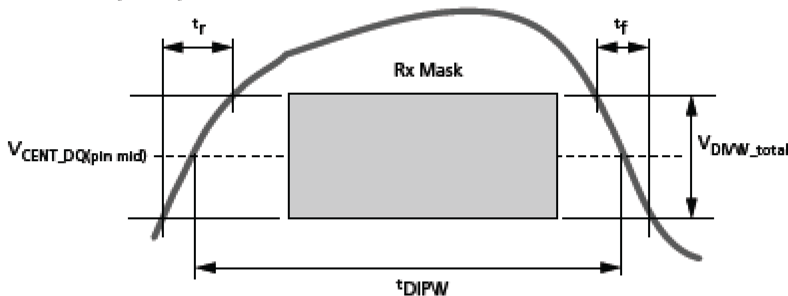
VCENT_DQ(pin_mid) is defined as the midpoint between the largest VCENT_DQ voltage level and the smallest VCENT_DQ voltage level across all DQ pins for a given DRAM component.Each VCENT_DQ is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for RON and ODT settings.

DQ-to-DQS tDQS2DQ and tDQDQ



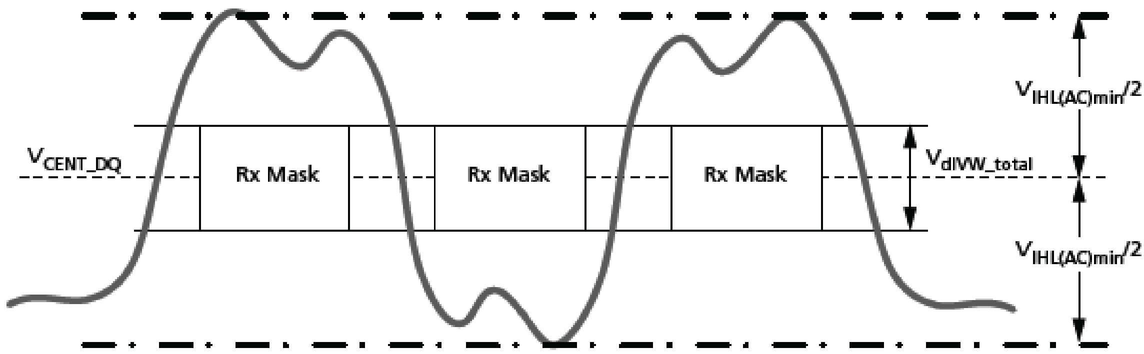
Notes: 1. These timings at the DRAM pins are referenced from the internal latch.
2. tDQS2DQ is measured at the center (midpoint) of the TdIVW window.
3. DQz represents the MAX tDQS2DQ in this example.
4. DQy represents the MIN tDQS2DQ in this example.

DQ tDIPW and SRIN_dIVW Definition for Each Input Pulse



Notes: 1. SRIN_dIVW = VdIVW_total/(tr or tf) signal must be monotonic within tr and tf range.

DQ VIHL(AC) Definition (for Each Input Pulse)



DQs In Receive Mode

Note UI = tCK(AVG)(MIN)/2

Symbol	Parameter	3200/3733		Unit
		Min	Max	
VdIVW_total	Rx mask voltage – peak-topeak	-	140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)	-	0.25	UI
VIHL_(AC)	DQ AC input pulse amplitude pk-pk	180	-	mV
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45	-	UI
tDQS2DQ	DQ to DQS offset	200	800	ps
tDQ2DQ	DQ to DQ offset	-	30	ps
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	ps/°C
tDQS2DQ_voltage	DQ to DQS offset voltage variation	-	33	Ps/50mV
SRIN_dIVW	Input slew rate over VdIVW_total	1	7	V/ns
tDQS2DQ_rank2rank	DQ to DQS offset rank to rank variation	-	200	ps
A.The RX voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600for all speed bins.				

Notes:

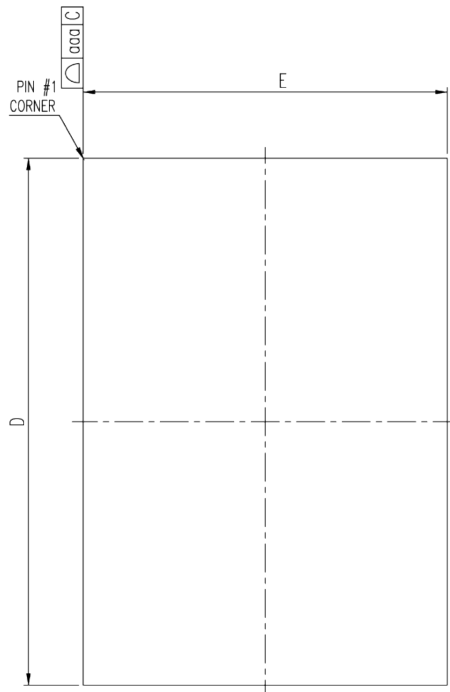
1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
6. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process,

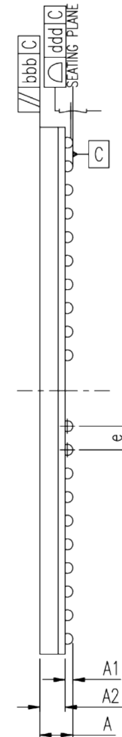
voltage and temperature variation.

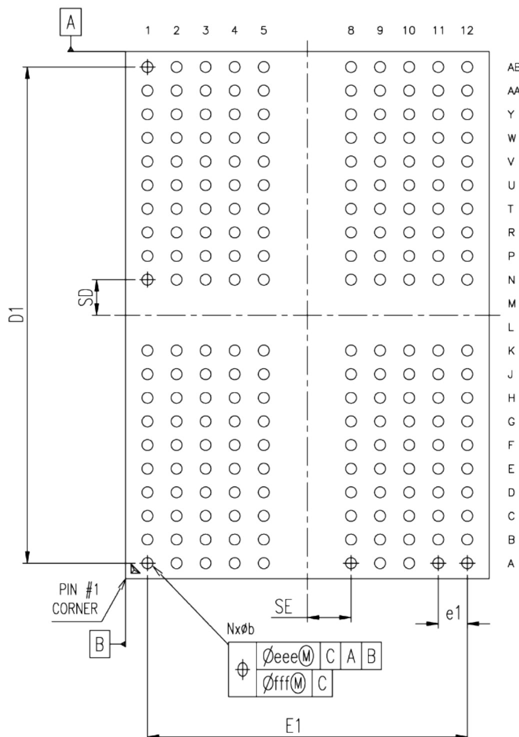
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ = VDD2 is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. VIHL_AC does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
15. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
16. tDQS2DQ_rabk2rank support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209- 4A may not support this parameter.

Package Description

200-ball FBGA 10x14.5mm







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.00	---	---	0.039
A1	---	0.21	---	---	0.008	---
A2	0.64	0.70	0.76	0.025	0.028	0.030
b	0.25	0.30	0.35	0.010	0.012	0.014
D	14.40	14.50	14.60	0.567	0.571	0.575
E	9.90	10.00	10.10	0.390	0.394	0.398
e	0.65 BSC.			0.026 BSC.		
e1	0.80 BSC.			0.031 BSC.		
JEDEC	MO-311(REF.)/MM					
aaa	0.10					
bbb	0.10					
ddd	0.08					
eee	0.15					
fff	0.08					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
200	1.20 BSC.	0.975 BSC.	8.80 BSC.	13.65 BSC.

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Feb. 2020	Rico Yang	N/A
1.0	First SPEC. release.	May. 2020	Rico Yang	N/A