128Mb (1M×4Banks×32) Synchronous SDRAM

Descriptions

The H2A11283233B is Synchronous Dynamic Random Access Memory (SDRAM) organized as 1Meg words x 4 banks by 32 bits. All inputs and outputs are synchronized with the positive edge of the clock.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

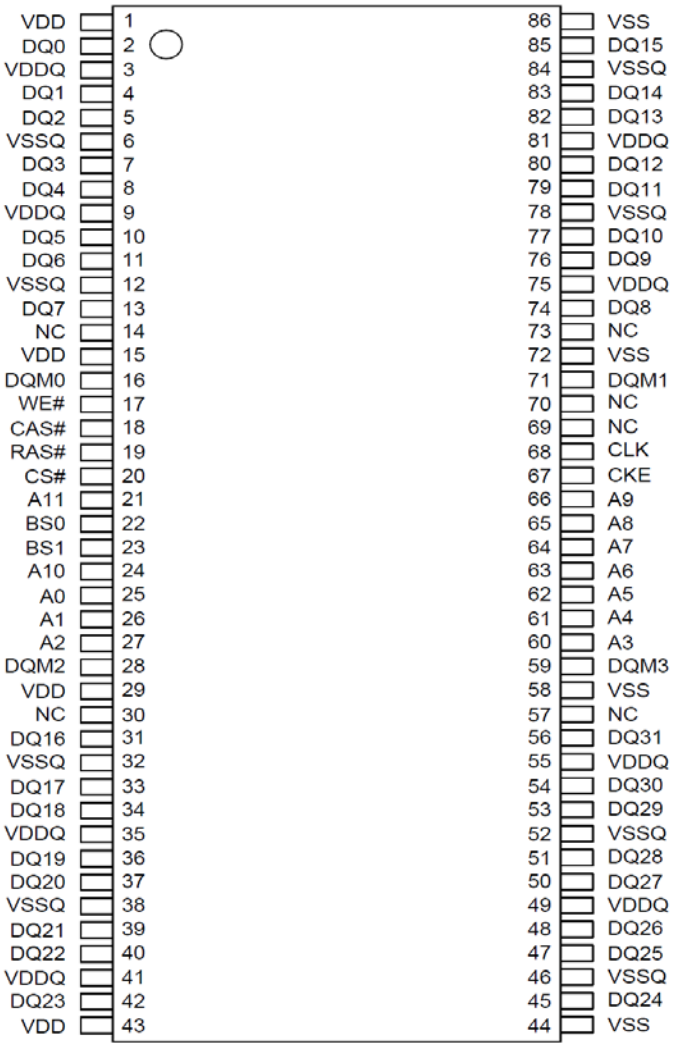
Features

- 1,048,576 Words × 4 banks × 32 bits organization
- Single 3.3V±0.3V Power Supply
- Self Refresh Mode
- CAS Latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and full page
- Burst Read, Single Writes Mode
- Byte Data Controlled by DQM
- Auto-precharge and Controlled Precharge
- 4K Refresh cycles / 64 mS
- Interface: LVTTL
- Packaged in TSOP II 86 pin, 400 mil – 0.50
- Using Lead free materials with RoHS compliant

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A11283233BM1C	4M X 32	PC-166MHz (3-3-3)	86pin TSOP(II)	Commercial

Pin Assignment



Pin Description (Simplified)

Pin	Name	Function
25-27, 60-66, 24,21	A0−A11	**(Address)** Multiplexed pins for row and column address. Row address: A0−A11. Column address: A0−A7. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
22, 23	BS0, BS1	**(Bank Select)** Select bank to activate during row address latch time, or bank to read/write during address latch time.
2,4,5,7,8,10,11, 13,74,76,77,79, 80,82,83,85,31, 33,34,36,37,39, 40,42,45,47,48, 50,51,53,54,56	DQ0−DQ31	**(Data Input/ Output)** Multiplexed pins for data input and output.
20	/CS	**(Chip Select)** Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
19	/RAS	**(Row Address Strobe)** Command input. When sampled at the rising edge of the clock, /RAS, /CAS and /WE define the operation to be executed.
18	/CAS	**(Column Address Strobe)** Referred to /RAS
17	/WE	**(Write Enable)** Referred to /RAS

Pin Description (Simplified)

Pin	Name	Function
16,71,28,59	DQM0~3	**(Input/Output Mask)** The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
68	CLK	**(Clock Inputs)** System clock used to sample inputs on the rising edge of clock.
67	CKE	**(Clock Enable)** CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
1,15,29,43	V_{DD}	**(Power)** Power for input buffers and logic circuit inside DRAM.
44,58,72,86	V_{SS}	**(Ground)** Ground for input buffers and logic circuit inside DRAM.
3,9,35,41,49, 55,75,81	V_{DDQ}	**(Power for I/O buffer)** Separated power from VDD, to improve DQ noise immunity.
6,12,32,38, 46,52,78, 84	V_{SSQ}	**(Ground for I/O Buffer)** Separated ground from VSS, to improve DQ noise immunity.
14,30,57, 69,70,73	NC	**(No Connection)** No connection.

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ V_{DD} + 0.3		V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ 4.6		V
T_{OPR}	Operating Temperature Range	Commercial	0 ~ +70	°C
T_{SOLDER}	Soldering Temperature (10s)	260		˚C
P_D	Power Dissipation	1		W
I_{OUT}	Short Circuit Current	50		mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Capacitance (V_{CC}=3.3V, f=1MHz, T_A=25°C)

Symbol	Parameter	Min.	Max.	Units
C_{CLK}	Input Capacitance (CLK)	-	3.5	pF
C_I	Input Capacitance (A0 to A11, BS0,BS1, /CS, /RAS, /CAS , /WE, DQM, CKE)	-	3.8	pF
C_{IO}	Input/Output Capacitance	-	6.5	pF

Note: These parameters are periodically sampled and not 100% tested

Recommended DC Operating Conditions (T_A=-0°C ~+70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V_{IH}	Input High Voltage ***(Note 1)***	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage ***(Note 2)***	-0.3	-	0.8	V

Note 1 : VIH (max.) = VDD/VDDQ+1.5V for pulse width ≤ 5 nS.
Note 2 : VIL (min.) = VSS/VSSQ-1.5V for pulse width ≤ 5 nS.

DC Characteristics

(V_{DD}=3.3V±0.3V, T_A=0°C ~ 70°C)

Symbol	Parameter	Test Conditions	PC-166MHz Max.	Units
I_{DD1}	Operating Current tCK = min., tRC = min. Active precharge command cycling without burst operation ***(Note 3)***	1 Bank Operation	130	mA
I_{DD2}	Standby Current tCK = min., CS = VIH VIH/L = VIH (min.)/VIL (max.) ***(Note 3)***	CKE = VIH	45	
I_{DD2P}	Bank: Inactive state ***(Note 3)***	CKE = VIL (Power Down mode)	2	
I_{DD2S}	Standby Current CLK = VIL, CS = VIH VIH/L=VIH (min.)/VIL (max.)	CKE = VIH	15	
I_{DD2PS}	Bank: Inactive state	CKE = VIL (Power Down mode)	2	
I_{DD3}	No Operating Current tCK = min., CS = VIH(min)	CKE = VIH	70	
I_{DD3P}	Bank: Active state (4 Banks)	CKE = VIL (Power Down mode)	15	
I_{DD4}	Burst Operating Current (tCK = min.) Read/ Write command cycling ***(Note 3,4)***		200	
I_{DD5}	Auto Refresh Current (tCK = min.) Auto refresh command cycling ***(Note 3)***		230	
I_{DD6}	Self Refresh Current (CKE = 0.2V) Self Refresh mode		2	

Note 1: Operation exceeds “Absolute Maximum Ratings” may cause permanent damage to the devices.

Note 2: All voltages are referenced to VSS.

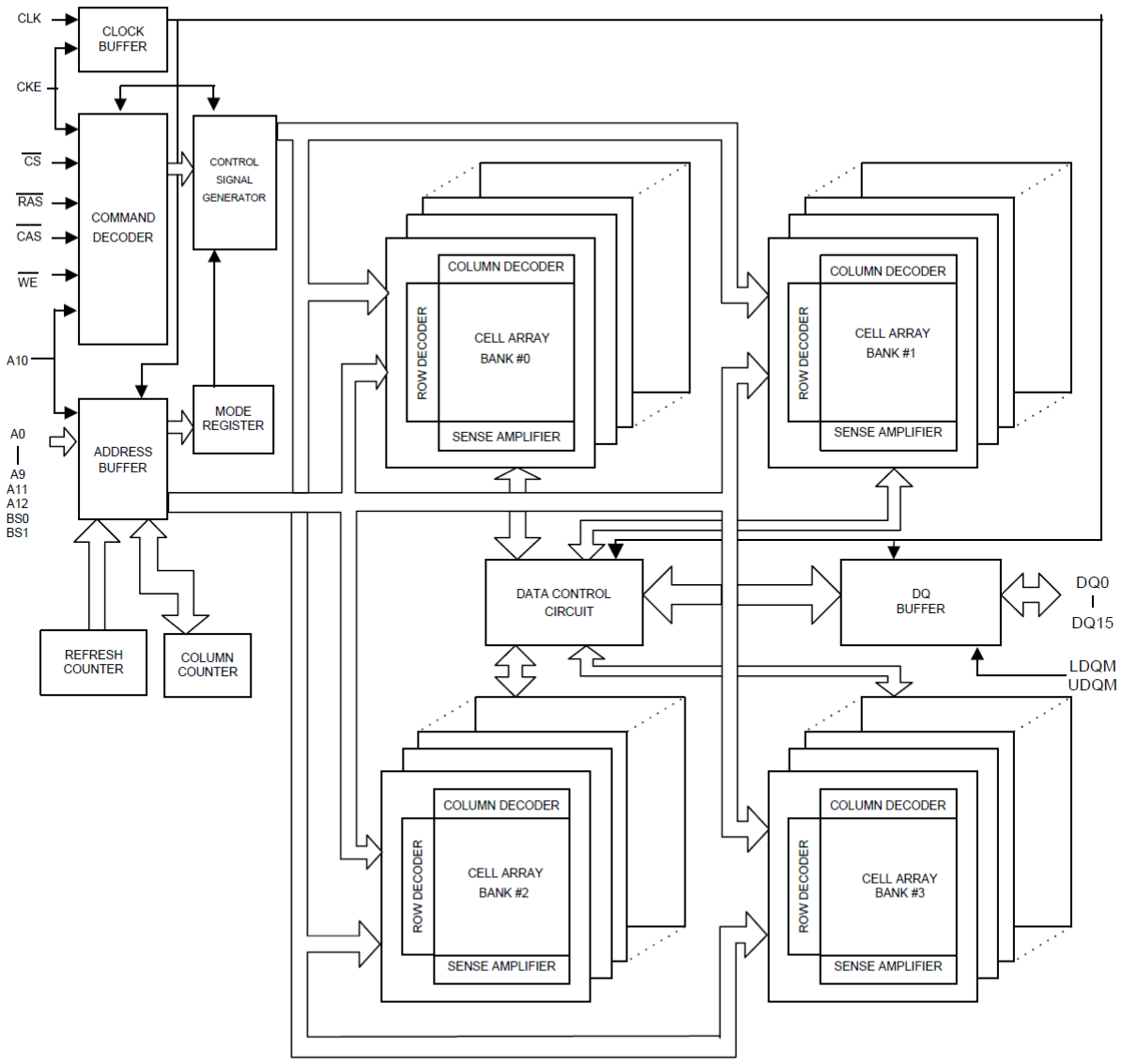
Note 3: These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of tCK and tRC.

Note 4: These parameters depend on the output loading conditions. Specified values are obtained with output open.

Note 5: Power up sequence please refer to “Functional Description” section described before.

Note 6: AC test load diagram.

Block Diagram

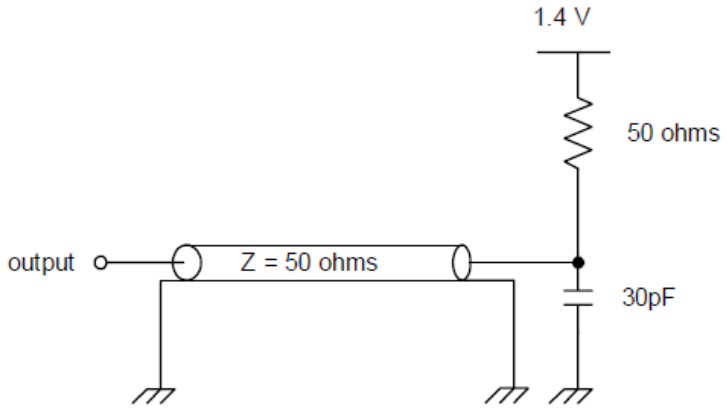


Note: The cell array configuration is 8192 * 512 * 16.

AC Operating Test Conditions

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

Item	Conditions
Output Reference Level	1.4V/1.4V
Output Load	See diagram as below
Input Signal Level	2.4V/0.4V
Transition Time of Input Signals	1.1ns
Input Reference Level	1.4V



AC TEST LOAD

AC Characteristics

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

Symbol	Parameter		166 MHz		Units
			Min.	Max.	
t_{OH}	Output Data Hold Time ***(Note 9)***		3		ns
t_{HZ}	Output Data High Impedance Time ***(Note 7)***	CL=3	3	6	ns
t_{LZ}	Output Data Low Impedance Time ***(Note 9)***		0		ns
t_{SB}	Power Down Mode Entry Time		0	6	ns
t_T	Transition Time of CLK (Rise and Fall)		0.5	1	ns
t_{DS}	Data-in-Set-up Time ***(Note 8)***		1.5		ns
t_{DH}	Data-in Hold Time ***(Note 8)***		1.0		ns
t_{AS}	Address Set-up Time ***(Note 8)***		1.5		ns
t_{AH}	Address Hold Time ***(Note 8)***		1.0		ns
t_{CKS}	CKE Set-up Time ***(Note 8)***		1.5		ns
t_{CKH}	CKE Hold Time ***(Note 8)***		1.0		ns
t_{CMS}	Command Set-up Time ***(Note 8)***		1.5		ns
t_{CMH}	Command Hold Time ***(Note 8)***		1.0		ns
t_{REF}	Refresh Time			64	ms
t_{RSC}	Mode Register Set Cycle Time		12		ns
t_{XSR}	Exit self refresh to ACTIVE command		72		ns

AC Characteristics (Continued)

(V_{DD}=3.3V±0.3V, T_A=0°C ~70°C)

Symbol	Parameter		166 MHz		Units
			Min.	Max.	
t_{RC}	Ref/Active to Ref/Active Command Period		60		ns
t_{RAS}	Active to Precharge Command Period		42	100k	ns
t_{RCD}	Active to Read/Write Command Delay Time		18		ns
t_{CCD}	Read/Write(a) to Read/Write(b) Command Period		1		t_{CK}
t_{RP}	Precharge to Active(b) Command Period		18		
t_{RRD}	Active(a) to Active(b) Command Period		12		
t_{WR}	Write Recovery Time	CL=3	2		t_{CK}
t_{CK}	CLK Cycle Time	CL=3	6	1K	ns
t_{CH}	CLK High Level Width ***(Note 8)***		2		ns
t_{CL}	CLK Low Level Width ***(Note 8)***		2		ns
t_{AC}	Access Time from CLK ***(Note 9)***	CL=3		5	ns

* All voltages referenced to V_{SS}.

Note 7: tHZ defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.

Note 8: Assumed input rise and fall time (tT) = 1nS.
If tr & tf is longer than 1nS, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]nS should be added to the parameter.

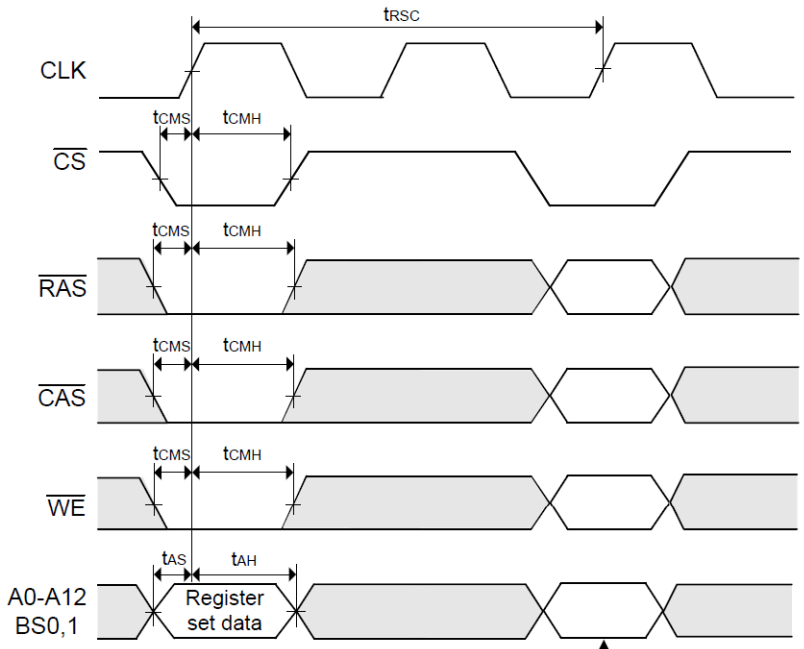
Note 9: If clock rising time (tT) is longer than 1nS, (tT/2-0.5)nS should be added to the parameter.

Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs. (Like a conventional DRAM) During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed V_{DD}+0.3V on any of the input pins or V_{DD} supplies. (CLK signal started at same time) After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command.

To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

Address Input for Mode Register Set



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	Reserved
A11	"0"	
A12	"0"	
BS0	"0"	
BS1	"0"	

	Burst Length	
A2 A1 A0	Sequential	Interleave
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1		
1 1 0		
1 1 1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

A6 A5 A4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

* "Reserved" should stay "0" during MRS cycle.

Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	0	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page*	n	n	n	Cn Cn+1 Cn+2……	-

* Page length is a function of I/O organization and column addressing □ 32 (CA0 ~ CA7): Full page = 256bits

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A11, A9~A10
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	L	H	H	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. DQM Truth Table

Command	Symbol	CKE		/CS
		n-1	n	
Data Write/Output Enable	ENB	H	X	H
Data Mask/Output Disable	MASK	H	X	L
Upper Byte Write Enable/Output Enable	BSTH	H	X	L
Read	READ	H	X	L
Read with Auto Pre-charge	READA	H	X	L
Write	WRIT	H	X	L
Write with Auto Pre-charge	WRITA	H	X	L
Bank Activate	ACT	H	X	L
Pre-charge Select Bank	PRE	H	X	L
Pre-charge All Banks	PALL	H	X	L
Mode Register Set	MRS	H	X	L

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

3. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Activating	Clock Suspend Mode Entry		H	L	X	X	X	X	X
Any	Clock Suspend Mode		L	L	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit		L	H	X	X	X	X	X
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	X	X	X	X	X
Power Down	Power Down Exit		L	H	X	X	X	X	X

H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	Nop or power down ***(Note 1)***
	L	H	H	X	X	NOP or BST	Nop or power down ***(Note 1)***
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 2)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 2)***
	L	L	H	H	BA/RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Refresh or self refresh ***(Note 3)***
	L	L	L	L	Op-Code	MRS	Mode register accessing
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	X	X	NOP or BST	Nop
	L	H	L	H	BA/CA/A10	READ/READA	Begin read: Determine AP ***(Note 4)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write: Determine AP ***(Note 4)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	Pre-charge ***(Note 5)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 3)***
	L	L	L	L	Op-Code	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end → Row active
	L	H	H	H	X	NOP	Continue burst to end → Row active
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read: Determine AP ***(Note 6)***
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start write: Determine AP ***(Note 6,7)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging ***(Note 3)***
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering
	L	H	H	H	X	NOP	Continue burst to end → Write recovering
	L	H	H	L	X	BST	Burst stop → Row active
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read: Determine AP 7, 8 ***(Note 6,7)***
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new write: Determine AP 7 ***(Note 6)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst, pre-charging ***(Note 8)***
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	Continue burst to end → Pre-charging
	L	H	H	H	X	NOP	Continue burst to end → Pre-charging
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 2)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ***(Note 2)***
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	Burst to end → Write recovering with auto pre-charge
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto pre-charge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 2)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ***(Note 2)***
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	Nop → Enter idle after tRP
	L	H	H	H	X	NOP	Nop → Enter idle after tRP
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 2)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after tRP
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	Nop → Enter idle after tRCD
	L	H	H	H	X	NOP	Nop → Enter idle after tRCD
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 2)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2,9)***
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ***(Note 2)***
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

4. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	Nop → Enter row active after tDPL
	L	H	H	H	X	NOP	Nop → Enter row active after tDPL
	L	H	H	L	X	BST	Nop → Enter row active after tDPL
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP ***(Note 7)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ***(Note 2)***
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Write Recovering with AP	H	X	X	X	X	DESL	Nop → Enter pre-charge after tDPL
	L	H	H	H	X	NOP	Nop → Enter pre-charge after tDPL
	L	H	H	L	X	BST	Nop → Enter pre-charge after tDPL
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 2,7)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 2)***
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	Op-Code	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	Nop → Enter idle after tRC
	L	H	H	X	X	NOP/BST	Nop → Enter idle after tRC
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL
Mode Register Accessing	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X	READ/WRIT	ILLEGAL
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 1: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode.All input buffers except CKE will be disabled.

Note 2: Illegal to bank in specified states;
Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 3: If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode. All input buffers except CKE will be disabled.

Note 4: Illegal if t_{RCD} is not satisfied.

Note 5: Illegal if t_{RAS} is not satisfied.

Note 6: Must satisfy burst interrupt condition.

Note 7: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 8: Must mask preceding data which don't satisfy t_{DPL}.

Note 9: Illegal if t_{RRD} is not satisfied.

5. Command Truth Table for CKE

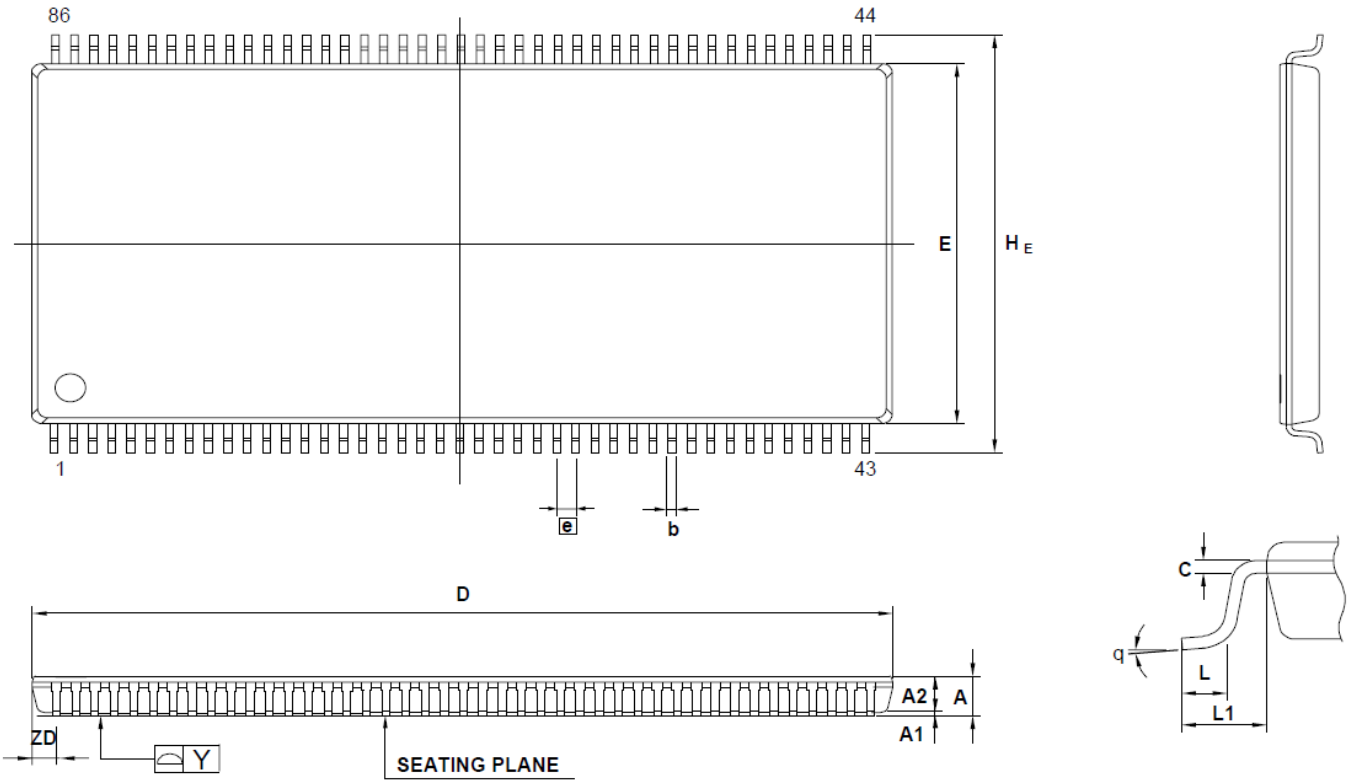
Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit self refresh
	L	H	H	X	X	X	X	Self refresh recovery
	L	H	L	H	H	X	X	Self refresh recovery
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	Maintain self refresh
Self Refresh Recovery	H	H	H	X	X	X	X	Idle after tRC
	H	H	L	H	H	X	X	Idle after tRC
	H	H	L	H	L	X	X	ILLEGAL
	H	H	L	L	X	X	X	ILLEGAL
	H	L	H	X	X	X	X	ILLEGAL
	H	L	L	H	H	X	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
Power Down	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit power down
	L	H	X	X	X	X	X	Exit power down → Idle
	L	L	X	X	X	X	X	Maintain power down mode
Both Banks Idle	H	H	H	X	X	X		Refer to operations in Operative Command Table
	H	H	L	H	X	X		
	H	H	L	L	H	X		
	H	H	L	L	L	H	X	Refresh
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	H	L	H	X	X	X		
	H	L	L	H	X	X		
	H	L	L	L	H	X		
	H	L	L	L	L	H	X	Self refresh ***(Note 10)***
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down ***(Note 10)***
Row Active	H	X	X	X	X	X	X	Refer to operations in Operative Command Table
	L	X	X	X	X	X	X	Power down ***(Note 10)***
Any State Other than Listed above	H	H	X	X	X	X		Refer to operations in Operative Command Table
	H	L	X	X	X	X	X	Begin clock suspend next cycle ***(Note 11)***
	L	H	X	X	X	X	X	Exit clock suspend next cycle
	L	L	X	X	X	X	X	Maintain clock suspend

H = High level, L = Low level, X = High or Low level (Don't care)

Notes 10: Self refresh can be entered only from the both banks idle state. Power down can be entered only from both banks idle or row active state.

Notes 11: Must be legal command as defined in Operative Command Table

Package Description



Controlling Dimension: Millimeters

SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.00	—	—	0.039	—
b	0.17	—	0.27	0.007	—	0.011
c	0.12	—	0.21	0.005	—	0.008
D	22.12	22.22	22.62	0.871	0.875	0.905
E	10.06	10.16	10.26	0.396	0.400	0.404
H_E	11.56	11.76	11.96	0.455	0.463	0.471
e	—	0.50	—	—	0.020	—
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	—	0.80	—	—	0.032	—
Y	—	—	0.10	—	—	0.004
ZD	—	0.61	—	—	0.024	—

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Apr. 2018	Ternence Chen	N/A
1.0	First SPEC. release.	Apr. 2018	Ternence Chen	N/A