8Gb (64MX16Banks×8) DDR4 SDRAM

Descriptions

The 8Gb DDR4 SDRAM is organized as 64Mbit x8 I/Os x 16banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 3200Mb/sec/ pin (DDR4-3200) for general applications. The chip is designed to comply with the following key DDR4 SDRAM fea-tures such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset. All of the control and address inputs are synchronized with a pair of exter-nally supplied differential clocks. Inputs are latched at the crosspoint of dif-ferential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fash-ion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. The DDR4 device operates with a single 1.2V (1.14V~1.26V) power supply and 1.2V (1.14V~1.26V). The 8Gb DDR4 device is available in 78ball FBGAs.

Features

- JEDEC standard 1.2V (1.14V~1.26V)
- VDDQ = 1.2V (1.14V~1.26V)
- 8-bit pre-fetch
- 16 internal banks (x8): 4 groups of 4 banks each
- Programmable CAS Latency (posted CAS):
  10,11,12,13,14,15,16,17,18,19,20,22,24
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal (self) calibration: calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- On Die Termination using ODT pin
- Connectivity Test Mode (TEN) is Supported
- Asynchronous Reset
- CRC for Read/Write data security
- Command address parity check
- DBI (Data Bus Inversion)
- Gear down mode
- POD (Pseudo Open Drain) interface for data input/output
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- PPR and sPPR is supported

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A908G08A6OIACC	1024M X 8	DDR4-2400MHz 17-17-17	78 Ball BGA, 7.5x11mm	Commercial
H2A908G08A6OJACC	1024M X 8	DDR4-2666MHz 19-19-19	78 Ball BGA, 7.5x11mm	Commercial
H2A908G08A6OKACC	1024M X 8	DDR4-3200MHz 22-22-22	78 Ball BGA, 7.5x11mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

78-Ball FBGA – x8 (Top View)

1	2	3		7	8	9
VDD	VSSQ	TDQS_c	**A**	DM_n/DBI_n/TDQS_t	VSSQ	VSS
VPP	VDDQ	DQS_c	**B**	DQ1	VDDQ	ZQ
VDDQ	DQ0	DQS_t	**C**	VDD	VSS	VDDQ
VSSQ	DQ4	DQ2	**D**	DQ3	DQ5	VSSQ
VSS	VDDQ	DQ6	**E**	DQ7	VDDQ	VSS
VDD	NC	ODT	**F**	CK_t	CK_c	VDD
VSS	NC	CKE	**G**	CS_n	NC	TEN
VDD	WE_n/A14	ACT_n	**H**	CAS_n/A15	RAS_n	VSS
VREFCA	BG0	A10/AP	**J**	A12/BC_n	BG1	VDD
VSS	BA0	A4	**K**	A3	BA1	VSS
RESET_n	A6	A0	**L**	A1	A5	ALERT_n
VDD	A8	A2	**M**	A9	A7	VPP
VSS	A11	PAR	**N**	NC	A13	VDD

Input / Output Functional Description

Type	Symbol	Description
Input	CK_t, CK_c	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
Input	CKE, (CKE1)	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the powe on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c,ODT and CKE are disabled during power-down. Input buffers excluding CKE, are disabled during Self-Refresh.
Input	CS_n, (CS1_n)	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
Input	C0,C1,C2	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
Input	ODT, (ODT1)	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 conurations. For x16 conuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
Input	ACT_n	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
Input	RAS_n/A16. CAS_n/ A15. WE_n/A14	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
Input/Output	DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8

Input	BG0 - BG1	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X8 have BG0 and BG1.
Input	BA0 - BA1	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
Input	A0 - A17	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/ BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 conuration.
Input	A10 / AP	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
Input	A12 / BC_n	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Input	RESET_n	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD,
Input / Output	DQ	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
Input / Output	DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c,DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
Output	TDQS_t, TDQS_c	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.

Input	PAR	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0, and C0-C2 (3DS devices). Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
Input/Output	ALERT_n	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
Input	TEN	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins.It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
	NC	No Connect: No internal electrical connection is present.
Supply	VDDQ	DQ Power Supply: 1.2 V +/- 0.06 V
Supply	VSSQ	DQ Ground
Supply	VDD	Power Supply: 1.2 V +/- 0.06 V
Supply	VSS	Ground
Supply	VPP	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
Supply	VREFCA	Reference voltage for CA
Supply	ZQ	Reference Pin for ZQ calibration
NOTE Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.3 ~ +1.5		V
VDD	Power Supply Voltage	-0.3 ~ +1.5		V
VDDQ	Power Supply Voltage	-0.3 ~ +1.5		V
VPP	Power Supply Voltage	-0.3 ~ +3.0		V
TOP	Operating Temperature Range	Commercial	0 ~ +95	°C
TSTG	Storage Temperature Range	-55 ~ +100		°C

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	1.14	1.2	1.26	V
V_{DDQ}	Supply voltage for output	1.14	1.2	1.26	V
V_{PP}	Wordline supply voltage	2.375	2.5	2.750	V

Input/ Output Capacitance

Symbol	Parameters	Min.	Max.	Unit	Notes
CCK	Input capacitance	0.2	0.7	pF	2,3
CDCK	Input capacitance delta	0	0.05	pF	2,3,6
CDI_CTRL	Input capacitance delta	-0.1	0.1	pF	2,3,8,9
CDI_ADD_CMD	Input capacitance delta	-0.1	0.1	pF	1,2,10,11
CIO	Input/output capacitance	0.55	1.15	pF	1,2,3
CI	Input capacitance	0.2	0.7	pF	2,3,4
CDIO	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,4
CDDQS	Input/output capacitance delta	0	0.05	pF	2,3,5
CALERT	Input/output capacitance	0.5	1.5	pF	2,3
CZQ	Input/output pin capacitance, ZQ	-	2.3	pF	2,3,12
CTEN	Input/output capacitance	0.2	2.3	pF	2,3,13

Notes1: Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.

Notes2: This parameter is not subject to a production test; it is verified by design and characterization. The capacitance is measured according to the JEP147 specification, “Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA),” with VDD, VDDQ, VSS, and VSSQ applied and all other pins floating (except the pin under test, CKE,RESET_n and ODT, as necessary). VDD = VDDQ = 1.5V, VBIAS = VDD/2 and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.

Notes3: This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.

Notes4: CDIO = CIO(DQ, DM) - 0.5 × (CIO(DQS_t) + CIO(DQS_c)).

Notes5: Absolute value of CIO (DQS_t), CIO (DQS_c)

Notes6: Absolute value of CCK_t, CCK_c

Notes7: CI applies to ODT, CS_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.

Notes8: CDI_CTRL applies to ODT, CS_n, and CKE.

Notes9: CDI_CTRL = CI(CTRL) - 0.5 × (CI(CLK_t) + CI(CLK_c)).

Notes10: CDI_ADD_CMD applies to A[17:0], BA1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.

Notes11: CDI_ADD_CMD = CI(ADD_CMD) - 0.5 × (CI(CLK_t) + CI(CLK_c)).

Notes12: Maximum external load capacitance on ZQ pin: 5pF.

Notes13: Only applicable if TEN pin does not have an internal pull-up.

DRAM Package Electrical Specifications

Parameters		Symbol	Min.	Max.	Unit	Notes
Input/ output	Zpkg	ZIO	45	85	ohm	1,2,4
	Package delay	TdIO	14	42	ps	1,3,4
	Lpkg	LIO	-	3.3	nH	10
	Cpkg	CIO	-	0.78	pF	11
DQS_t, DQS_c	Zpkg	ZIO DQS	45	85	ohm	1,2
	Package delay	TdIO DQS	14	42	ps	1,3
	Lpkg	LIO DQS	-	3.3	nH	10
	Cpkg	CIO DQS	-	0.78	pF	11
	Delta Zpkg	DZDIO DQS	-	10	ohm	1,2,6
	Delta delay	DTdDIO DQS	-	5	ps	1,3,6
Input CTRL pins	Zpkg	ZI CTRL	50	90	ohm	1,2,8
	Package delay	TdI CTRL	14	42	ps	1,3,8
	Lpkg	LI CTRL	-	3.4	nH	10
	Cpkg	CI CTRL	-	0.7	pF	11
Input CMD ADD pins	Zpkg	ZI ADD CMD	50	90	ohm	1,2,7
	Package delay	TdI ADD CMD	14	45	ps	1,3,7
	Lpkg	LI ADD CMD	-	3.6	nH	10
	Cpkg	CI ADD CMD	-	0.74	pF	11

DRAM Package Electrical Specifications(Continued)

Parameters		Symbol	Min.	Max.	Unit	Notes
CK_t, CK_c	Zpkg	ZCK	50	90	ohm	1,2
	Package delay	TdCK	14	42	ps	1,3
	Package delay	DZDCK	-	10	ohm	1,2,5
	Delta delay	DTdCK	-	5	ps	1,3,5
Input CLK	Lpkg	LI CLK	-	3.4	nH	11
	Cpkg	CI CLK	-	0.7	pF	11
ZQ Zpkg		ZO ZQ	40	100	ohm	1,2
ZQ delay		TdO ZQ	20	90	ps	1,3
ALERT Zpkg		ZO ALERT	40	100	ohm	1,2
ALERT delay		TdO ALERT	20	55	ps	1,3

Notes1: The package parasitic (L and C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, and VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS, and VSSQ shorted and all other signal pins shorted at the die, not pin, side.

Notes2: Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).

Notes3: Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).

Notes4: ZIO and TdIO apply to DQ, DM, TDQS_t and TDQS_c.

Notes5: Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).

Notes6: Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).

Notes7: ZI ADD CMD and TdI ADD CMD apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, and WE_n.

Notes8: ZI CTRL and TdI CTRL apply to ODT, CS_n, and CKE.

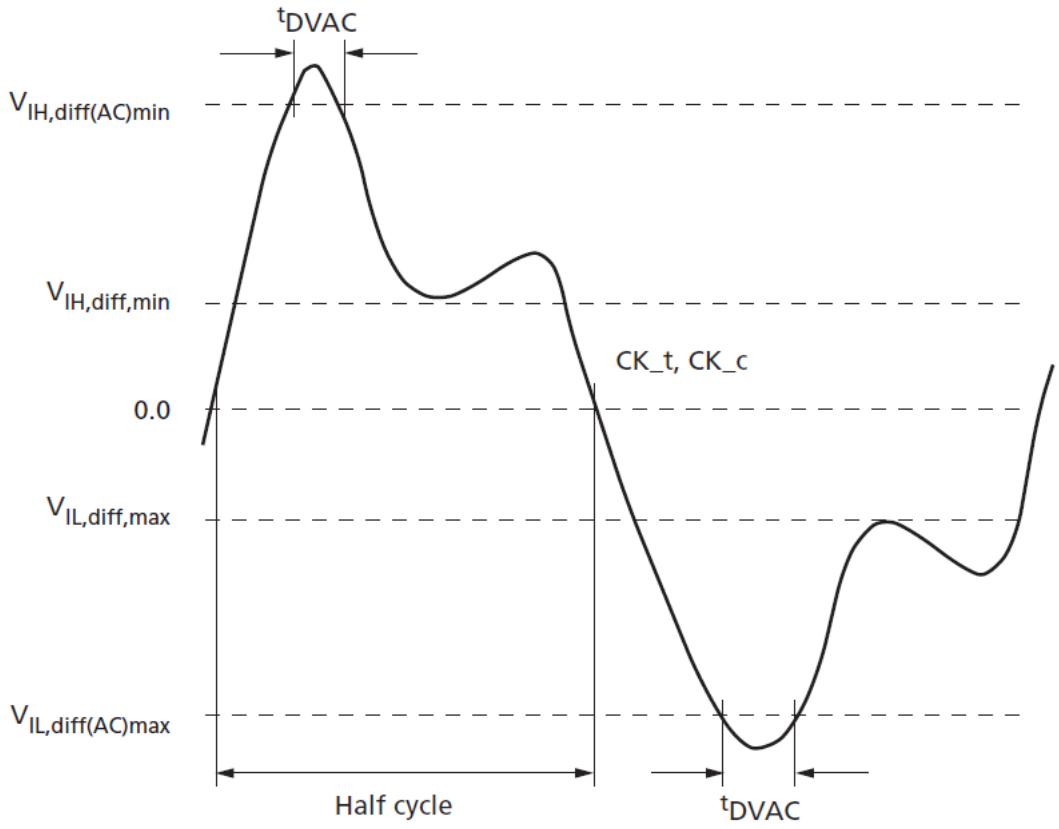
Notes9: Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.

Notes10: It is assumed that Lpkg can be approximated as Lpkg = ZO × Td.

Notes11: It is assumed that Cpkg can be approximated as Cpkg = Td/ZO.

AC and DC Differential Input Measurement Levels

Differential Inputs



Differential Input Swing Requirements for CK_t, CK_c

Symbol	Parameter	Min.	Max.	Units	Note
VIHdiff	Differential input high	+0.135	See ***Note3***	V	1
VILdiff	Differential input low	See ***Note3***	-0.135	V	1
VIHdiff (AC)	AC Differential input high	2x(VIH(AC)-VREF)	See ***Note3***	V	2
VILdiff (AC)	AC Differential input low	See ***Note3***	2x(VREF-VIL(AC))	V	2

Note1: Used to define a differential signal slew-rate.

Note2: For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

Note3: These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (VIHCA(DC) max, VILCA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot..

Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

Minimum Time AC Time tDVAC for CK

Slew Rate [V/ns]	tDVAC (ps) at [VIH,diff(AC) to VIL,diff(AC)]	
	200mV	TBDmV
>4.0	120	--
4.0	115	--
3.0	110	--
2.0	105	--
1.9	100	--
1.6	95	--
1.4	90	--
1.2	85	--
1.0	80	--
<1.0	80	--
Note: Below VIL(AC).		

Single-Ended Requirements for CK Differential Signals

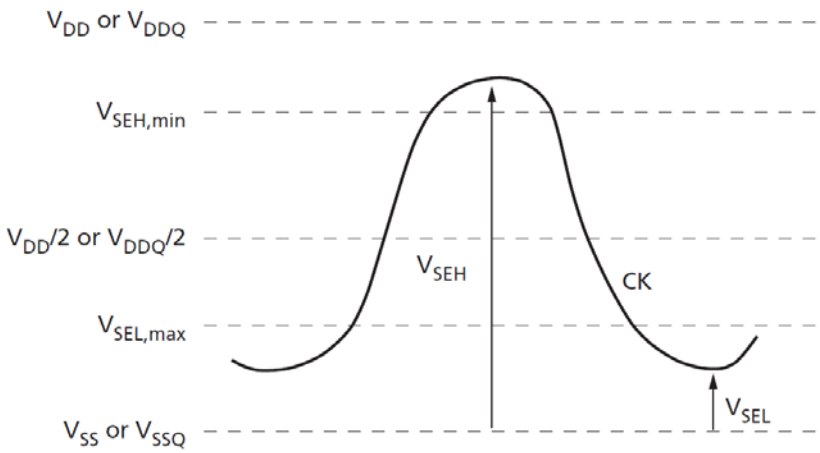
Each individual component of a differential signal (CK, DQS, /CK, /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(AC) / VIL(AC)) for Address/Command signals) in every half-cycle.

DQS, /DQS have to reach VSEHmin / VSELmax [approximately the ac-levels (VIH(AC) / VIL(AC)) for DQ signals] in every half-cycle preceding and following a valid transition.

Note that the applicable AC-levels for Address/Command and DQ's might be different per speed-bin etc. E.g., if VIHCA(AC100)/VILCA(AC100) is used for Address/Command signals, then these AC-levels apply also for the single-ended components of differential CK and /CK.

Single-Ended Requirements for CK



Single-Ended Requirements for CK

Symbol	Parameter	Min.	Max.	Units	Note
VSEH	Single-ended high-level for CK, /CK	(VDD/2)+0.095	See ***Note3***	V	1,2
VSEL	Single-ended low-level for CK, /CK	See ***Note3***	(VDD/2)-0.095	V	1,2

Note1: For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

Note2: ADDR/CMD VIH(AC) and VIL(AC) based on VREFCA.

Note3: These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

AC and DC Output Measurement Levels

Symbol	Parameter	Specification	Units	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1*VDDQ	V	1
VOM(DC)	DC output middle measurement level (for IV curve linearity)	0.8*VDDQ	V	1
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5*VDDQ	V	1
VOH(AC)	AC output high measurement level (for output slew rate)	(0.7+0.15)*VDDQ	V	1
VOL(AC)	AC output low measurement level (for output slew rate)	(0.7-0.15)*VDDQ	V	1
VOHdiff(AC)	AC differential output high measurement level (for output slew rate)	0.3*VDDQ	V	2
VOLdiff(AC)	AC differential output low measurement level (for output slew rate)	-0.3*VDDQ	V	2

Notes1: The swing of ±0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to VTT = VDDQ.

Notes2: The swing of ±0.3 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to VTT = VDDQ at each differential output.

Recommended DC Operating Conditions

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I_{DD0}	**Operating One Bank Active-Precharge Current (AL = 0)** CKE: HIGH; External clock: On; tCK, nRC, nRAS, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: VDDQ; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the IDD0 Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	27	28	31	mA
I_{PP0}	**Operating One Bank Active-Precharge IPP Current (AL = 0)** Same conditions as IDD0 above	4	4	4	mA
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL = 0)** CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, CL: see the previous table; BL: 8;1, 5 AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank addres inputs, Data I/O: partially toggling according to the IDD1 Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the followi table); Output buffer and RTT: enabled in mode registers;2 ODT Signal stable at 0	32	32	34	mA
I_{DD2P}	**Precharge Power-Down Current** CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n: stal at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	11	11	13	mA
I_{DD2N}	**Precharge Standby Current (AL = 0)** CKE: HIGH; External clock: On; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address,bank group address bank address Inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stab at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0; Pattern details: see the IDD2N and IDD3N Measurement-Loop Pattern table	18	18	20	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I_{DD3P}	**Active Power-Down Current (AL = 0)** CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address,bank group address, bank address inputs: stable at 1; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	19	19	21	mA
I_{DD3N}	**Active Standby Current (AL = 0)** CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and	27	27	30	mA
I_{DD4R}	**Operating Burst Read Current (AL = 0)** CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS_n: HIGH between RD; Command,address, bank group address, bank address inputs: partially toggling according to the IDD4R Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the IDD4R Measurement-Loop Pattern table; DM_n stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the IDD4R Measurement-Loop pattern table);Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	82	99	114	mA
I_{DD4W}	**Operating Burst Write Current (AL = 0)** CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4W Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the IDD4W Measurement-Loop Pattern table; DM: stable at 0; Bank activity: all banks open, WR commands cycling throu banks: 0, 0, 1, 1, 2, 2, ... (see IDD4W Measurement-Loop Pattern table);Output buffer and RTT: enabled in mode registers (see note2); ODT signal: stable at HIGH	80	92	106	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I_{DD5B}	**Burst Refresh Current (1X REF)** CKE: HIGH; External clock: on; tCK, CL, nREFI: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between REF;Command, address, bank group address, bank address inputs: partially toggling according to the IDD5R Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: REF command every nREFI (seethe IDD5R Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers2; ODT signal:stable at 0	230	230	230	mA
I_{PP5B}	**Burst Refresh Current (1X REF)** Same conditions as IDD5R above	25	25	25	mA
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** TC: 0–85°C; Auto self refresh (ASR): disabled;3 Self refresh temp erature range (SRT): normal;4 CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8;1 AL: 0; CS_n, command, address, bank group address, bank address, data I/O: VDDQ; DM_n: stable at 1; Bank activity: SELF REFRESH operation ;Output buffer and RTT: enabled in mode registers;2 ODT signal: midlevel	21	21	21	mA
I_{PP6N}	**Self Refresh IPP Current: Normal Temperature Range** Same conditions as IDD6N above	4	4	4	mA
I_{DD7}	**Operating Bank Interleave Read Current** CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8;15 AL: CL -1; CS_n: HIGH between ACT and RDA; Command, address, group bank adress, bank address inputs: partially toggling according to the IDD7 Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the IDD7 Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the IDD7 Measurement-Loop Pattern table; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	135	147	158	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2400	2666	3200	Units
		Max			
I_{PP7}	**Operating Bank Interleave Read IPP Current** Same conditions as IDD7 above	10	11	11	mA
I_{DD8}	**Maximum Power Down Current** Place DRAM in MPSM then CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n:stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; 2 ODT signal: stable at 0	9	10	11	mA

***Note*：**

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6

   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2

   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s, 2666MT/s
   100] : 3200MT/s

   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate

   DLL disabled : set MR1 [A0 = 0]

   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s, 2666MT/s
   011] : 3200MT/s

   Read DBI enabled : set MR5 [A12 = 1]

   Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10] : Extended Temperature range
   11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

Refresh Parameters

Parameter	Symbol		8G	Unit	Notes
REF command to ACT or REF command time	tRFC (All bank groups)		350	ns	-
Average periodic refresh interval	tREFI	0°C ≦ TC ≦ 85°C	7.8	μs	-
		85°C < TC ≦ 95°C	3.9	μs	*

Note: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

AC Operating Test Characteristics

DDR4-2400 & 2666 & 3200 Speed Bins

VDD = VDDQ = 1.2V ±60mV

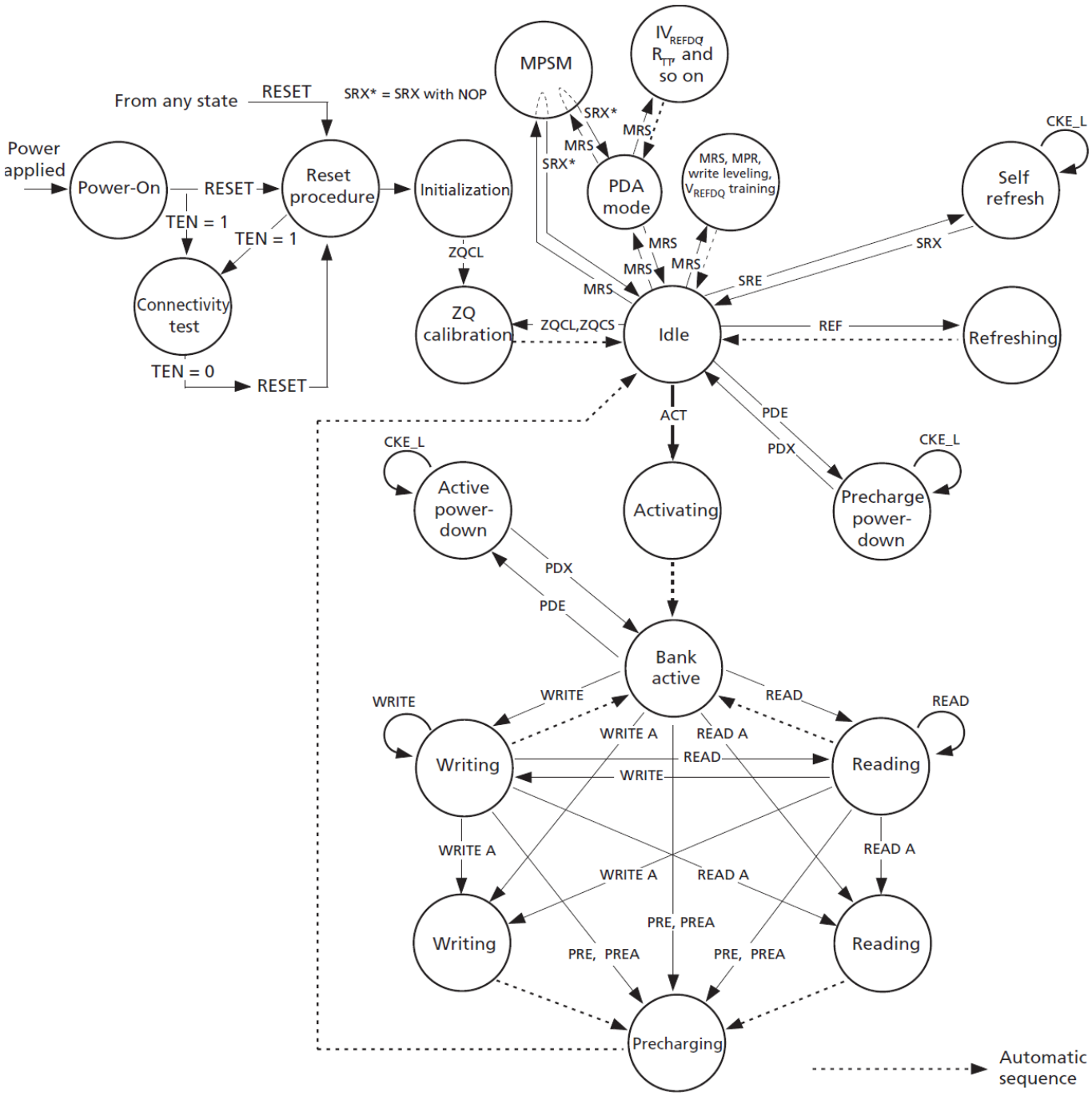
Symbol	Speed Bin		(DDR4-2400)		(DDR4-2666)		(DDR4-3200)		Units
	CL-nRCD-nRP		17-17-17		19-19-19		22-22-22		
	Parameter		Min.	Max.	Min.	Min.	Min.	Max.	
tAA	Internal read command to first data		14.16	18	14.25	18	13.75	18	ns
tRCD	Active to read or write delay		14.16	-	14.25	-	13.75	-	ns
tRP	Precharge command period		14.16	-	14.25	-	13.75	-	ns
tRC	Active to active/auto refresh command		46.16	-	46.25	-	45.75	-	ns
tRAS	Active to precharge command period		32	9xtREFI	32	9xtREFI	32	9xtREFI	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Min.**	**Max.**	**Min.**	**Min.**	**Max.**	**Max.**	**Units**
CL=9	CL=11	CWL=9	Reserved		Reserved		Reserved		ns
CL=10	CL=12	CWL=9	1.5	1.6	1.5	1.6	1.5	1.6	ns
CL=11	CL=13	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=12	CL=14	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=13	CL=15	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=14	CL=16	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=15	CL=18	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=16	CL=19	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=17	CL=20	CWL=12,16	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL=18	CL=21	CWL=12,16	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL=19	CL=22	CWL=14,18	-	-	0.750	<0.833	0.750	<0.833	ns
CL=20	CL=23	CWL=14,18	-	-	0.750	<0.833	0.750	<0.833	ns
CL=22	CL=26	CWL=16,20	-	-	-	-	0.625	<0.75	
CL=24	CL=28	CWL=16,20	-	-	-	-	0.625	<0.75	
Support CL Settings			10-18		10-20		10-20,22,24		nCK
Support CL settings with read DBI			12-16, 18-21		12-15, 17-23		12-16, 18-24,26,28		nCK
Support CWL Settings			9-12, 14,16		9-12, 14,16,18		9-12, 14,16,18,20		nCK

Speed Bin Table Note：

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-2400, 2600, 3200 Speed Bin Tables are valid only when Gear_Down mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section "Rounding Algorithms".
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. ‘Reserved’ settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
11. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
12. CL number in parentheses, it means that these numbers are optional.
13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

Simplified State Diagram



Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). /RESET needs to be maintained for minimum 700 us with stable power. CKE is pulled “Low” anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2. OR
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After /RESET_n is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

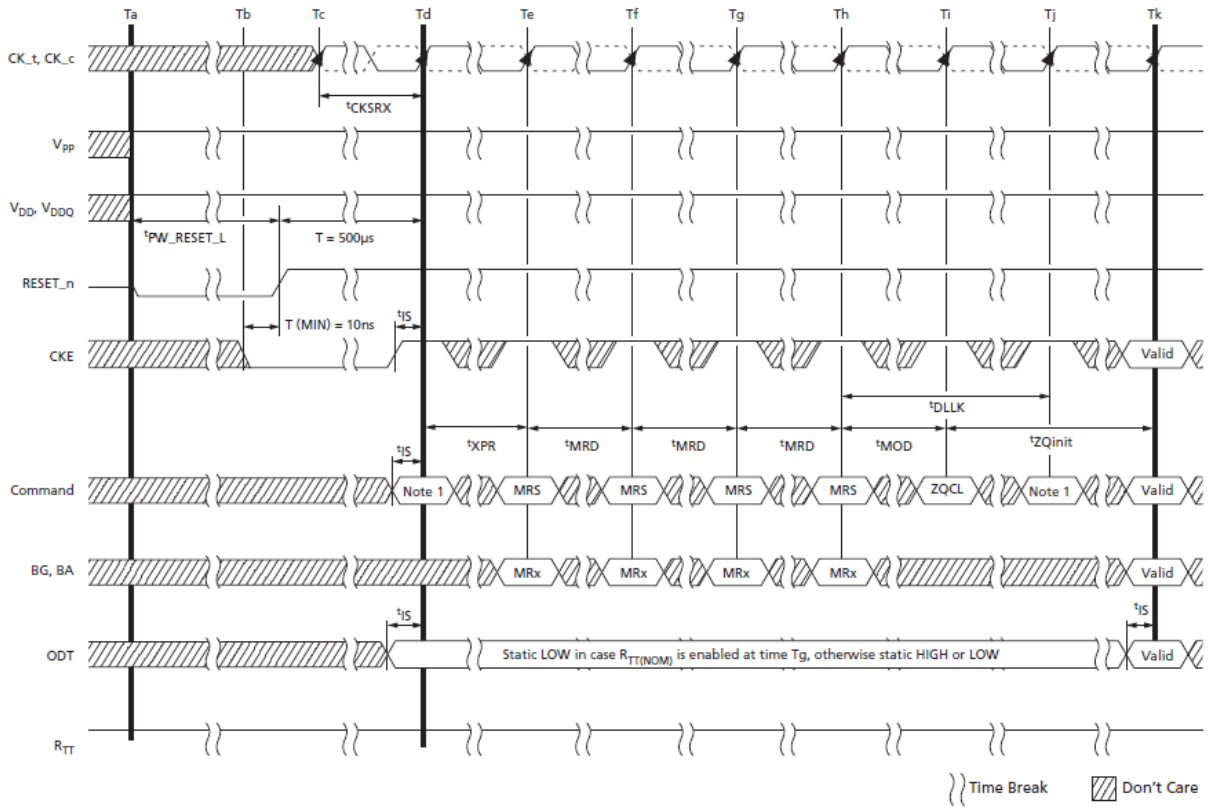
3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. *(tXPR=max (tXS ; 5 x tCK)*

6. Issue MRS command to load MR3 with all application settings, wait tMRD.
7. Issue MRS command to load MR6 with all application settings, wait tMRD.
8. Issue MRS command to load MR5 with all application settings, wait tMRD.
9 Issue MRS command to load MR4 with all application settings, wait tMRD.
10. Issue MRS command to load MR2 with all application settings, wait tMRD.
11. Issue MRS command to load MR1 with all application settings, wait tMRD.
12. Issue MRS command to load MR0 with all application settings, wait tMOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for tDLLK and tZQinit to complete.

Reset and Power up initialization sequence



Note 1: From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.

Note 2: MRS commands must be issued to all mode registers that have defined settings.

Note 3: In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).

Note 4: TEN is not shown; however, it is assumed to be held LOW.

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject t o pro- duction test.

Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK(abs)j \right) / N \qquad N = 200$$

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj \right) / \{N \times tCK(avg)\} \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj \right) / \{N \times tCK(avg)\} \qquad N = 200$$

Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

Timing Parameters by Speed Grade

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	0.833	<0.937	0.750	<0.833	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot tCK(avg)m ax + tJIT(per)max_tot						tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-42	42	-38	38	-32	32	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-19	19	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-30	30	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	83	-	75	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	67	-	60	-	50	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-61	61	-55	55	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-73	73	-66	66	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	-73	73	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	-78	78	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	-83	83	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	-87	87	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	-91	91	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	-94	94	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	-96	96	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	-99	99	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	-101	101	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	-103	103	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	-104	104	-87	87	ps	
Cumulative error across 15 cycles	tERR(15per)	-118	118	-106	106	-89	89	ps	
Cumulative error across 16 cycles	tERR(16per)	-120	120	-108	108	90	90	ps	
Cumulative error across 17 cycles	tERR(17per)	-122	122	-110	110	-92	92	ps	
Cumulative error across 18 cycles	tERR(18per)	-124	124	-112	112	-93	93	ps	
Cumulative error across n = 13, . .. 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	55	-	40	-	ps	

Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	162	-	145	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	80	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	162	-	145	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	410	-	385	-	340	-	ps	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)		Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)		Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)		Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,15ns)		Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	ns	1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		1,34

Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		34
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	768	-	1024	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register RecoveryTime	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	max(3nCK, 3.748ns)	-	max(3nCK, 3.748ns)	-	max(3nCK, 3.748ns)	-	nCK	
Mode Register Se commandt cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL		tMOD+tCAL	-	tMOD+tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+tCAL		tMOD+tCAL	-	tMOD+tCAL	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.17	-	0.18	-	0.20	tCK(avg)/2	13,18,39,49
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.74	-	0.74	-	0.70	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device: (tQH - tDQSQ)	tDVWd	0.64	-	0.64	-	0.64	-	UI	17,18,39

of each UI on a given DRAM									,49
Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t,CK_c	tLZ(DQ)	-330	175	-310	170	-250	160	ps	39
DQ high impedance time from CK_t,CK_c	tHZ(DQ)	-	175	-	170	-	160	ps	39
Data Strobe Timing									
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	tCK	39,40
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE2	NA	NA	1.8	NOTE44	1.8	NOTE 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE45	0.33	NOTE45	0.33	NOTE 45	tCK	39

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output lowtime	tQSL	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble)	tWPRE2	NA		1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-330	175	-310	170	-250	160	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	-	170	-	160	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	-0.5	0.5	-0.5	0.5	-0.5	0.5	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-175	175	-170	170	-160	160	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		290		270		260	ps	37,38,39

MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-		
CS setup time to CKE	tMPX_S	tIS(min)+ tIHL(min)	-	tIS(min)+ tIHL(min)	-	tIS(min)+ tIHL(min)	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	nCK	

Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max (5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	

PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		nCK	
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.28	0.72	0.26	0.74	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144	80	160	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	64		71		85	nCK	
Parity Latency	PL	5		5		6		nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
Geardown timing									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	tXPR	-	tXPR	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	tXS	-	tXS	-		
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	tMOD +4nCK	-	tMOD +4nCK	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	tMOD	-	tMOD	-		27
Geardown setup time	tGEAR_setup	-	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	2	-	2	-	nCK	
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	ns	34

Note：

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

DDR4 Function Matrix

Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	x16	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V		

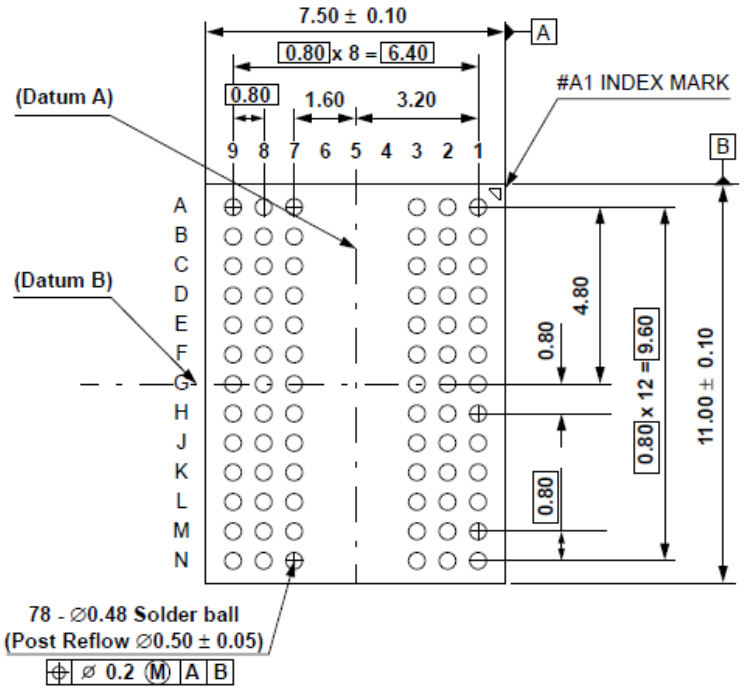
Function Matrix (By Speed. V:Supported, Blank:Not supported)

Functions	DLL Off mode	DLL On mode			NOTE
	equal or slower than 250Mbps	1600/1866/2133 Mbps	2400Mbps	2666/2933/ 3200Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh	V	V	V	V	
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion	V	V	V	V	
TDQS		V	V	V	
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity		V	V	V	
Control Gear Down Mode				V	
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode		V	V	V	
Boundary Scan Mode	V	V	V	V	

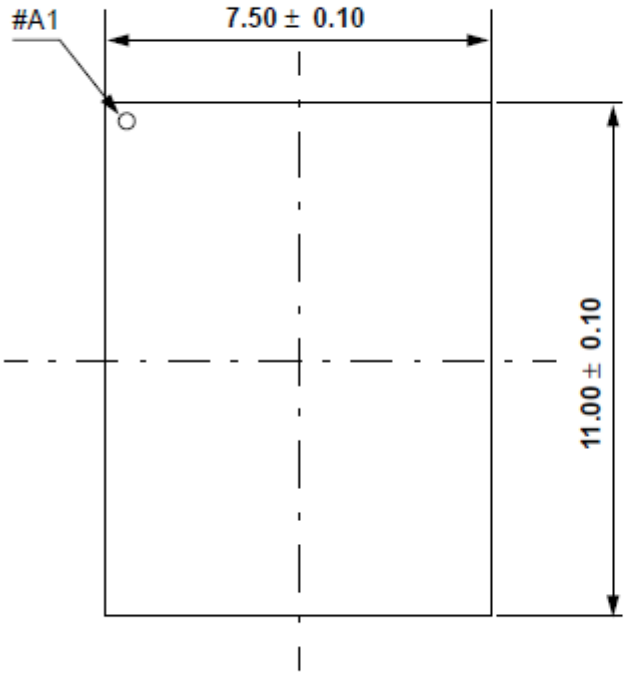
Package Description: 78Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)

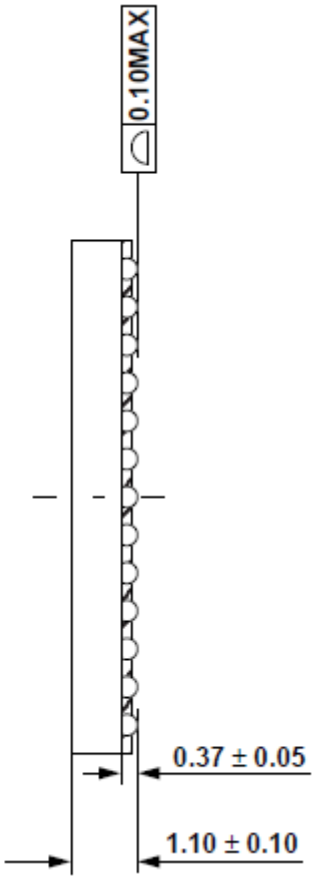
Units : Millimeters



BOTTOM VIEW



TOP VIEW



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2019	Rico Yang	N/A
1.0	First SPEC. release.	Aug. 2019	Rico Yang	N/A