1Gb (8MX8Banks×16) DDR2 SDRAM

Descriptions

The H2A301G1656C is a high speed Double Date Rate 2 (DDR2) Synchronous DRAM fabricated with ultra high performance CMOS process containing 1G bits which organized as 8Mbits x 8 banks by 16 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 1066 Mb/sec/pin (DDR2-1066) for general applications. The chip is designed to comply with the following key DDR2 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) Off-Chip Driver (OCD) impedance adjustment and On Die Termination (4) normal and weak strength data output driver. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style. The 1Gb DDR2 devices operate with a single power supply: 1.8V ± 0.1V VDD and VDDQ. Available package: TFBGA-84Ball.

Features

- JEDEC Standard VDD/VDDQ = 1.8V±0.1V.
- All inputs and outputs are compatible with SSTL_18 interface.
- Fullydifferential clock inputs (CK, /CK) operation.
- Eight Banks
- Posted CAS
- Bust length: 4 and 8.
- Write Latency (WL) =Read Latency (RL) -1.
- Read Latency (RL) = Programmable Additive Latency (AL) + CAS Latency (CL)
- Bi-directional DifferentialData Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available.
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination (ODT)
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- RoHS Compliance
- Partial Array Self-Refresh (PASR)
- High Temperature Self-Refresh rate enable

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A301G1656CA6C	64M X 16	DDR2-667MHz 5-5-5	84Ball BGA, 8x12.5mm	Commercial
H2A301G1656CB6C	64M X 16	DDR2-800MHz 5-5-5	84Ball BGA, 8x12.5mm	Commercial
H2A301G1656CC6C	64M X 16	DDR2-1066MHz 7-7-7	84Ball BGA, 8x12.5mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

84-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	/UDQS/NU	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	/LDQS	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CLK	VDD
	CKE	/WE	K	/RAS	/CLK	ODT
BA2	BA0	BA1	L	/CAS	/CS	
	A10	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	RFU	R	RFU	RFU	

84-Ball FBGA – x16 Ball Descriptions

Type	Symbol	Description
Input	A[12:0]	**(Address)** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected
Input	BA[2:0]	**(Bank Select)** BA[2:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register, including MR,EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
Input	CK, CK#	**Clock:** CK and CK# are differential clock inputs. All address and control inp signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossin of CK and CK#.
Input	CKE	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, powerdown exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down.Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level after VDD is applied during first power-up. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, VREF must be maintained.
Input	CS#	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered high. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
Input	LDM, UDM, DM	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ[7:0] and UDM is DM for upper byte DQ[15:8].

Input	ODT	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ[15:0], LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; The ODT input will be ignored if disabled via the LOAD MODE command.
Input	/RAS , /CAS , /WE	**(Command Inputs)** /RAS , /CAS and /WE (along with /CS) define the command being entered.

I/O	DQ[15:0]	**Data input/output:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
I/O	DQS, DQS#	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
I/O	LDQS, LDQS#	**Data strobe for lower byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data.LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
I/O	UDQS, UDQS#	**Data strobe for upper byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data.UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
Supply	VDD	**Power Supply:** 1.8V ± 0.1V.
Supply	VDDQ	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
Supply	VDDL	**DLL power supply:**1.8V ± 0.1V.
Supply	VREF	SSTL_18 reference voltage (VDDQ/2).
Supply	VSS	Ground.
Supply	VSSDL	**(DLL Ground):** Isolated on the device from VSS and VSSQ.
Supply	VSSQ	**DQ ground:** Isolated on the device for improved noise immunity.
-	NC	**No connect:** These balls should be left unconnected
-	NU	**Not used:** If EMR(E10) = 0, A8 and E8 are UDQS# and LDQS#. If EMR(E10) = 1, then A8 and E8 are not used.
-	RFU	**Reserved for future use:** Row address bits A13, A14, and A15.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ +2.3		V
V_{DD}	Power Supply Voltage	-1.0 ~ +2.3		V
V_{DDQ}	Power Supply Voltage	-0.5 ~ +2.3		V
VDDL	DLL Power Supply Voltage	-0.5 ~ +2.3		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +85	°C
T_{STG}	Storage Temperature Range	-55 ~ +100		°C

Note: 1. VDD, VDDQ, and VDDL must be within 300mV of each other at all times; this is not required when power is ramping down.

2. VREF <= 0.6 x VDDQ; however, VREF may be >= VDDQ provided that VREF <= 300mV.

3. Voltage on any I/O may not exceed voltage on VDDQ.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.7	1.8	1.9	V
V_{DDL}	Power Supply for DLL Voltage	1.7	1.8	1.9	V
V_{DDQ}	Power Supply for I/O Voltage	1.7	1.8	1.9	V
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V
V_{TT}	I/O Termination Voltage	V_{REF} - 0.04	V_{REF}	VREF + 0.04	V
V_{ID}	DC Differential Input Voltage	0.25	-	VDDQ + 0.6	V
V_{IH}	Input Logic High Voltage	V_{REF} + 0.125	-	VDDQ + 0.3	V
V_{IL}	Input Logic Low Voltage	-0.3	-	VREF - 0.125	V

Input / Output Capacitance

Symbol	Parameters	Min.	Max.	Unit
C_{CK}	Input Capacitance , CLK and /CLK	1.0	2.0	pF
CD_{CK}	Input Capacitance delta , CLK and /CLK	-	0.25	pF
C_I	Input Capacitance, all other input-only pins	1.0	2.0	pF
CD_I	Input Capacitance delta, all other input-only pins	-	0.25	pF
C_{IO}	Input/output Capacitance, DQ, LDM, UDM, LDQS,/LDQS , UDQS, /UDQS	2.5	4.0	pF
CD_{IO}	Input/output Capacitance delta, DQ, LDM, UDM,LDQS, /LDQS , UDQS, /UDQS	-	0.5	pF

Recommended DC Operating Conditions

Symbol	Parameter & Test Conditions	1066MHz	800MHz	667MHz	Units	NOTES
		Max				
IDD0	**Operating Current - One Bank Active-Precharge** tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING;Databus inputs are SWITCHING.	90	80	75	mA	1,2,3, 4,5,6
IDD1	**Operating Current - One Bank Active-Read-Precharge** IOUT = 0 mA;BL = 4, CL = CL(IDD), AL = 0;tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD (IDD);CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING;Data bus inputs are SWITCHING.	100	95	90	mA	1,2,3, 4,5,6
IDD2P	**Precharge Power-Down Current** All banks idle;tCK = tCK(IDD); CKE is LOW;Other control and address inputs are STABLE; Data Bus inputs are FLOATING. (TCASE ≤ 85°C)	7	7	7	mA	1,2,3,4, 5,6,7
IDD2N	**Precharge Standby Current** All banks idle;tCK = tCK(IDD);CKE is HIGH, /CS is HIGH;Other control and address inputs are SWITCHING Data bus inputs are SWITCHING.	36	30	26	mA	1,2,3, 4,5,6
IDD2Q	**Precharge Quiet Standby Current** All banks idle;tCK = tCK(IDD);CKE is HIGH, /CS is HIGH; Other control and address inputs are STABLE; Data bus inputs are FLOATING.	30	26	26	mA	1,2,3, 4,5,6

IDD3PF	**Active Power Down Current** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address input are STABLE; Data bus inputs are FLOATING. (TCASE≤85°C)	Fast PDN Exit MRS(12) = 0	23	20	15	mA	1,2,3, 4,5,6
IDD3PS		Slow PDN Exit MRS(12) = 1	10	10	10	mA	1,2,3,4, 5,6,7
IDD3N	**Active Standby Current** All banks open; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		42	35	32	mA	1,2,3, 4,5,6
IDD4R	**Operating Burst Read Current** All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD),tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING;Data Bus inputs are SWITCHING.		180	150	125	mA	1,2,3, 4,5,6
IDD4W	**Operating Burst Write Current** All banks open, Continuous burst writes;BL = 4, CL = CL (IDD), AL = 0;tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address inputs are SWITCHING;Data Bus inputs are SWITCHING.		185	160	135	mA	1,2,3, 4,5,6
IDD5B	**Burst Refresh Current** tCK = tCK(IDD);Refresh command every tRFC(IDD) interval;CKE is HIGH, /CS is HIGH between valid commands;Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		160	150	145	mA	1,2,3, 4,5,6

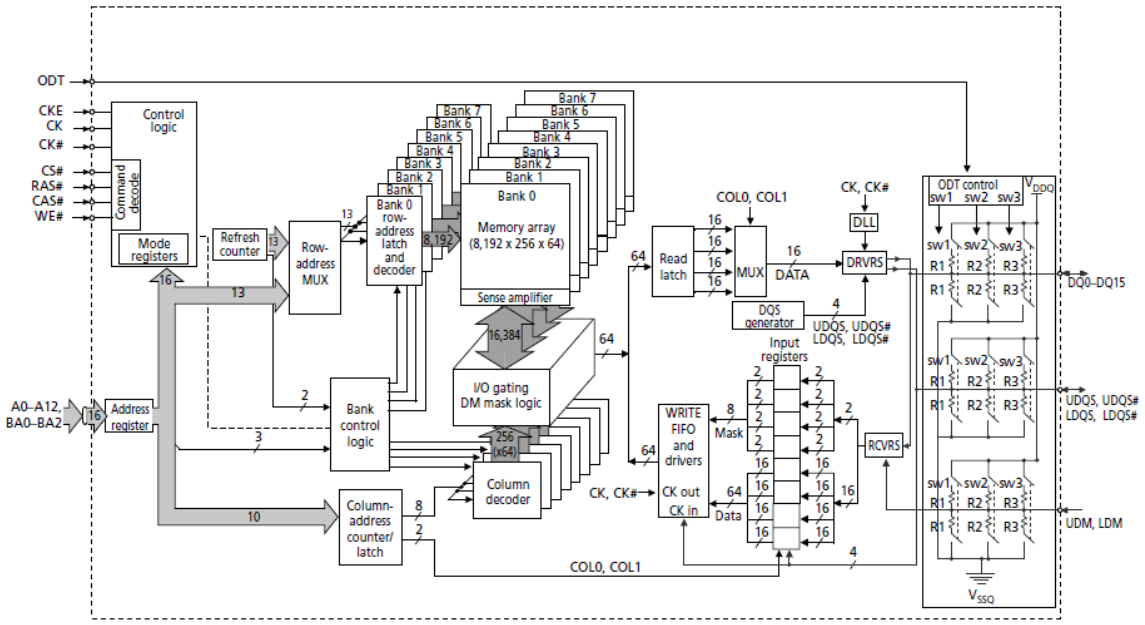
IDD6	**Self Refresh Current** CKE ≤ 0.2 V, external clock off, CLK and /CLK at 0 V;Other control and address inputs are FLOATING; Data bus inputs are FLOATING. (TCASE ≤ 85°C)	7	7	7	mA	1,2,3,4, 5,6,7
IDD7	**Operating Bank Interleave Read Current** All bank interleaving reads, IOU T = 0mA;BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD);tCK = tCK(IDD),tRC = tRC(IDD), tRRD =tRRD(IDD), tFAW= tFAW(IDD), tRCD = tRCD(IDD);CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are STABLE during deselects;Data Bus inputs are SWITCHING.	270	260	230	mA	1,2,3, 4,5,6

Note 1: VDD = 1.8 V ± 0.1V; VDDQ = 1.8 V ± 0.1V.
Note 2: IDD specifications are tested after the device is properly initialized.
Note 3: Input slew rate is specified by AC Parametric Test Condition.
Note 4: IDD parameters are specified with ODT disabled.
Note 5: Data Bus consists of DQ, LDM, UDM, LDQS, /LDQS , UDQS and /UDQS
Note 6: Definitions for IDD

LOW = Vin ≤ VIL (ac) (max)
HIGH = Vin ≥ VIH (ac) (min)
STABLE = inputs stable at a HIGH or LOW level
FLOATING = inputs at VREF = VDDQ/2
SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock)for DQ signals not including masks or strobes.

Note 7: The following IDD values must be derated (IDD limits increase), when TCASE ≥ 85°C IDD2P must be derated by 20%;IDD3P(slow) must be derated by 30% and IDD6 must be derated by 80%. (IDD6 will increase by this amount if TCASE < 85°C and the 2X refresh option is still enabled)

Block Diagram



CD Default Setting Table

Parameter	Min.	Typ.	Max.	Units
Output Impedance	-	-	-	Ω
Pull-up / Pull-down mismatch	0	-	4	Ω
Output Impedance step size for OCD calibration	0	-	1.5	Ω
Output Slew Rate	1.5	-	5.0	V/ns

AC Operating Test Conditions

Symbol	Parameter	Value	Units
VSWING (max.)	Input Signal Maximum Peak to Peak Swing	1.0	V
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns
VREF	Input Reference Level	0.5*VDDQ	V

AC Operating Test Conditions

Symbol	Parameter	Min.	Max.	Units
V_{ID}	AC Differential Input Voltage	0.5	VDDQ+0.3	V
V_{IX}	AC Differential Cross Point Input Voltage	0.5*VDDQ-0.175	0.5*VDDQ+0.175	V
V_{OX}	AC Differential Cross Point Output Voltage	0.5*VDDQ-0.125	0.5*VDDQ+0.125	V
V_{IH}	Input Logic High Voltage	VREF+0.25	-	V
V_{IH}	Input Logic High Voltage	VREF+0.20	-	V
V_{IL}	Input Logic High Voltage	-0.3	VREF-0.25	V
V_{IL}	Input Logic High Voltage	-0.3	VREF-0.20	V

AC Operating Test Characteristics

DDR2-1066MHz Speed Bins

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin		DDR2-1066MHz		Units	Notes
	CL-tRCD-tRP		7-7-7			
	Parameter		Min.	Max.		
t_{RCD}	Active to Read/Write Command Delay Time		13.125	-	ns	
t_{RP}	Precharge to Active Command Period		13.125	-	ns	
t_{RC}	Active to Ref/Active Command Period		58.125	-	ns	
t_{RAS}	Active to Precharge Command Period		40	70000	ns	
t_{RFC}	Auto Refresh to Active/Auto Refresh command period		127.5	-	ns	
t_{RAFI}	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*		3.9	µs	
		0°C ≤ TCASE ≤ 85°C	-	7.8	µs	
		85°C < TCASE ≤ 95°C	-	3.9	µs	
t_{CCD}	/CAS to /CAS command delay		2	-	nCK	
t_{CK} (AVG)	Average clock period	tCK(avg) @ CL=3	5.0	8.0	ns	
		tCK(avg) @ CL=4	3.75	8.0	ns	
		tCK(avg) @ CL=5	2.5	8.0	ns	
		tCK(avg) @ CL=6	2.5	8.0	ns	
		tCK(avg) @ CL=7	1.875	8.0	ns	
t_{CH} (AVG)	Average clock high pulse width		0.48	0.52	tCK(AVG)	
t_{CL} (AVG)	Average clock low pulse width		0.48	0.52	tCK(AVG)	
t_{AC}	DQ output access time from CLK/ /CLK		-350	350	ps	
t_{DQSCK}	DQS output access time from CLK / /CLK		-300	300	ps	
t_{DQSQ}	DQS-DQ skew for DQS & associated DQ signals		-	175	ps	
t_{CKE}	CKE minimum high and low pulse width		3		nCK	
t_{RRD}	Active to active command period for 2KB page size		10	-	ns	
t_{FAW}	Four Activate Window for 2KB page size		45	-	ns	
t_{WR}	Write recovery time		15	-	ns	
t_{DAL}	Auto-precharge write recovery + precharge time		tWR + tRP	-	nCK	
t_{WTR}	Internal Write to Read command delay		7.5	-	ns	
t_{RTP}	Internal Read to Precharge command delay		7.5	-	ns	

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	DDR2-1066MHz		Units	Notes
	CL-tRCD-tRP	7-7-7			
	Parameter	Min.	Max.		
t_{IH} (ref)	Address and control input hold time	325	-	ps	
t_{IPW}	Address and control input pulse width for each input	0.6	-	tCK(avg)	
t_{DQSS}	DQS latching rising transitions to associated clock edges	-0.25	0.25	tCK(avg)	
t_{DSS}	DQS falling edge to CLK setup time	0.2	-	tCK(avg)	
t_{DSH}	DQS falling edge hold time from CLK	0.2	-	tCK(avg)	
t_{DQSH}	DQS input high pulse width	0.35	-	tCK(avg)	
t_{DQSL}	DQS input low pulse width	0.35	-	tCK(avg)	

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	DDR2-1066MHz		Units	Notes
	CL-tRCD-tRP	7-7-7			
	Parameter	Min.	Max.		
t_{WPRE}	Write preamble	0.35	-	tCK(AVG)	
t_{WPST}	Write preamble	0.4	0.6	tCK(AVG)	
t_{RPRE}	Read preamble	0.9	1.1	tCK(AVG)	
t_{RPST}	Read preamble	0.4	0.6	tCK(AVG)	
tDS(base)	DQ and DM input setup time	0	-	ps	
tDH(base)	DQ and DM input hold time	75	-	ps	
t_{DS}(ref)	DQ and DM input setup time	200	-	ps	
t_{DH}(ref)	DQ and DM input hold time	200	-	ps	
t_{DIPW}	DQ and DM input pulse width for each input	0.35	-	tCK(AVG)	
t_{HZ}	Data-out high-impedance time from CLK/ /CLK	-	tAC,max	ps	
t_{LZ}(DQS)	DQS/ /DQS -low-impedance time from CLK/ /CLK	tAC,min	tAC,max	ps	
t_{LZ}(DQ)	DQ low-impedance time from CLK/ /CLK	2 x tAC,min	tAC,max	ps	
t_{HP}	Clock half pulse width	Min. (tCH(abs), tCL(abs))	-	ps	
t_{QHS}	Data hold skew factor	-	250	ps	
t_{QH}	DQ/DQS output hold time from DQS	tHP - tQHS	-	ps	
t_{XSNR}	Exit Self Refresh to a non-Read command	tRFC + 10	-	ns	
t_{XSRD}	Exit Self Refresh to a Read command	200	-	nCK	
t_{XP}	Exit precharge power down to any command	3	-	nCK	
t_{XARD}	Exit active power down to Read command	3	-	nCK	
t_{XARDS}	Exit active power down to Read command (slow exit, lower power)	10 - AL	-	nCK	
t_{AOND}	ODT turn-on delay	2	2	nCK	
t_{AON}	ODT turn-on	tAC,min	tAC,max + 2.575	ns	

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	DDR2-1066MHz		Units	Notes
	CL-tRCD-tRP	7-7-7			
	Parameter	Min.	Max.		
t_{AONPD}	ODT turn-on (Power Down mode)	tAC,min + 2	2 x tCK(avg) + tAC,max+1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	nCK	
t_{AOF}	ODT turn-off	tAC,min	tAC,max + 0.6	ns	
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	ns	
t_{ANPD}	ODT to power down Entry Latency	4	-	nCK	
t_{AXPD}	ODT Power Down Exit Latency	11		nCK	
t_{MRD}	Mode Register Set command cycle time	2	-	nCK	
t_{MOD}	MRS command to ODT update delay	12	0	ns	
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK(avg)+tIH	-	ns	

AC Operating Test Characteristics

DDR2-800MHz & DDR2-667MHz Speed Bins

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin		DDR2-800MHz		DDR2-667MHz		Units	Notes
	CL-tRCD-tRP		6-6-6		5-5-5			
	Parameter		Min.	Max.	Min.	Max.		
t_{RCD}	Active to Read/Write Command Delay Time		15	-	15	-	ns	
t_{RP}	Precharge to Active Command Period		15	-	15	-	ns	
t_{RC}	Active to Ref/Active Command Period		55	-	55	-	ns	
t_{RAS}	Active to Precharge Command Period		40	70000	40	70000	ns	
t_{RFC}	Auto Refresh to Active/Auto Refresh command period		127.5	-	127.5	-	ns	
t_{REFI}	Average periodic refresh Interval	-40°C≤TCASE ≤ 85°C*	-	3.9	-	3.9	µs	
		0°C < TCASE ≤ 85°C		7.8	-	7.8	µs	
		85°C < TCASE ≤ 95°C	-	3.9	-	3.9	µs	
t_{CCD}	/CAS to /CAS command delay		2	-	2	-	nCK	
t_{CK}(avg)	Average clock period	tCK(avg) @ CL=3	5	8	5	8	ns	
		tCK(avg) @ CL=4	3.75	8	3.75	8	ns	
		tCK(avg) @ CL=5	3.0	8	3	8	ns	
		tCK(avg) @ CL=6	2.5	8	-	-	ns	
t_{CH}(avg)	Average clock high pulse width		0.48	0.52	0.48	0.52	tCK (AVG)	
t_{CL}(avg)	Average clock low pulse width		0.48	0.52	0.48	0.52	tCK (AVG)	
t_{AC}	DQ output access time from CLK/ /CLK		-400	400	-450	450	ps	
t_{DQSCK}	DQS output access time from CLK / /CLK		-350	350	-400	400	ps	
t_{DQSQ}	DQS-DQ skew for DQS & associated DQ signals		-	200	-	240	ps	
t_{CKE}	CKE minimum high and low pulse width		3	-	3	-	nCK	
t_{RRD}	Active to active command period for 2KB page size		10	-	10	-	ns	
t_{FAW}	Four Activate Window for 2KB page size		45	-	50	-	ns	
t_{WR}	Write recovery time		15	-	15	-	ns	
t_{DAL}	Auto-precharge write recovery + precharge time		tWR + tRP	-	tWR + tRP	-	nCK	

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	DDR2-800MHz		DDR2-667MHz		Units	Notes
	CL-tRCD-tRP	5-5-5		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
t_{WTR}	Internal Write to Read command delay	7.5	-	7.5	-	ns	
t_{RTP}	Internal Read to Precharge command delay	7.5	-	7.5	-	ns	
t_{IS} (base)	Address and control input setup time	175	-	200	-	ps	
t_{IH} (base)	Address and control input hold time	250	-	275	-	ps	
t_{IS} (ref)	Address and control input setup time	375	-	400	-	ps	
t_{IH} (ref)	Address and control input hold time	375	-	400	-	ps	
t_{IPW}	Address and control input pulse width for each input	0.6	-	0.6	-	tCK (AVG)	
t_{DQSS}	DQS latching rising transitions to associated clock edges	-0.25	0.25	-0.25	0.25	tCK (AVG)	
t_{DSS}	DQS falling edge to CLK setup time	0.2	-	0.2	-	tCK (AVG)	
t_{DSH}	DQS falling edge hold time from CLK	0.2	-	0.2	-	tCK (AVG)	
t_{DQSH}	DQS input high pulse width	0.35	-	0.35	-	tCK (AVG)	
t_{DQSL}	DQS input low pulse width	0.35	-	0.35	-	tCK (AVG)	

* -40°C ≤ TCASE ≤ 85°C is for 25I grade only.

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	DDR2-800MHz		DDR2-667MHz		Units	Notes
	CL-tRCD-tRP	5-5-5		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
t_{WPRE}	Write preamble	0.35	-	0.35	-	tCK (AVG)	
t_{WPST}	Write postamble	0.4	0.6	0.4	0.6	tCK (AVG)	
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	tCK (AVG)	
t_{RPST}	Read postamble	0.4	0.6	0.4	0.6	tCK (AVG)	
t_{DS}(base)	DQ and DM input setup time	50	-	100	-	ps	
t_{DH}(base)	DQ and DM input hold time	125	-	175	-	ps	
t_{DS}(ref)	DQ and DM input setup time	250	-	300	-	ps	
t_{DH}(ref)	DQ and DM input hold time	250	-	300	-	ps	
t_{DIPW}	DQ and DM input pulse width for each input	0.35	-	0.35	-	tCK (AVG)	
t_{HZ}	Data-out high-impedance time from CLK/ /CLK	-	tAC,max	-	tAC,max	ps	
t_{LZ}(DQS)	DQS/ /DQS -low-impedance time from CLK/ /CLK	tAC,min	tAC,max	tAC,min	tAC,max	ps	
t_{LZ}(DQ)	DQ low-impedance time from CLK/ /CLK	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	ps	
t_{HP}	Clock half pulse width	Min. (tCH(abs), tCL(abs))		Min. (tCH(abs), tCL(abs))		ps	
t_{QHS}	Data hold skew factor	-	300	-	340	ps	
t_{QH}	DQ/DQS output hold time from DQS	tHP-tQHS	-	tHP-tQHS	-	ps	
t_{XSNR}	Exit Self Refresh to a non-Read command	tRFC+10	-	tRFC+10	-	ns	
t_{XSRD}	Exit Self Refresh to a Read command	200	-	200	-	nCK	

AC Operating Test Characteristics

VDD/VDDQ = 1.8V±0.1V

Symbol	Speed Bin	DDR2-800MHz		DDR2-667MHz		Units	Notes
	CL-tRCD-tRP	5-5-5		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
t_{XP}	Exit precharge power down to any command	2	-	2	-	nCK	
t_{XARD}	Exit active power down to Read command	2	-	2	-	nCK	
t_{XARDS}	Exit active power down to Read command (slow exit, lower power)	8 - AL	-	7 - AL	-	nCK	
t_{AOND}	ODT turn-on delay	2	2	2	2	nCK	
t_{AON}	ODT turn-on	tAC,min	tAC,max+ 0.6	tAC,min	tAC,max+ 0.7	ns	
t_{AONPD}	ODT turn-on (Power Down mode)	tAC,min + 2	2 x tCK(avg)+ tAC,max+ 1	tAC,min + 2	2 x tCK(avg)+ tAC,max+ 1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	nCK	
t_{AOF}	ODT turn-off	tAC,min	tAC,max+ 0.6	tAC,min	tAC,max+ 0.6	ns	
t_{AOFPD}	ODT turn-off (Power Down mode)	tAC,min + 2	2xtCK (avg)+tAC, max+1	tAC,min + 2	2xtCK (avg)+tAC, max+1	ns	
t_{ANPD}	ODT to power down Entry Latency	3	-	3	-	nCK	
t_{AXPD}	ODT Power Down Exit Latency	8		8		nCK	
t_{MRD}	Mode Register Set command cycle time	2	-	2	-	nCK	
t_{MOD}	MRS command to ODT update delay	12	-	12	-	ns	
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK (avg)+tIH	-	tIS+tCK (avg)+tIH	-	ns	

Notes:

1. All voltages are referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the operation of the device are warranted for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Outputs measured with equivalent load.
4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.0V in the test environment, and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0 V/ns for signals in the range between VIL(AC) and VIH(AC). Slew rates other than 1.0 V/ns may require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
7. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, or system reset condition. SSC allows for small deviations in operating frequency, provided the SSC guidelines are satisfied.
8. The clock's tCK (AVG) is the average clock over any 200 consecutive clocks and tCK (AVG) MIN is the smallest clock rate allowed (except for a deviation due to allowed clock jitter). Input clock jitter is allowed provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
9. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range 8–60 kHz with an additional one percent tCK (AVG); however, the spread spectrum may not use a clock rate below tCK (AVG) MIN or above tCK (AVG) MAX.
10. MIN (tCL, tCH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; tCH (AVG) and tCL (AVG) must be met with or without clock jitter and with or without duty cycle jitter. tCH (AVG) and tCL (AVG) are the average of any 200 consecutive CK falling edges. tCH limits may be exceeded if the duty cycle jitter is small enough that the absolute half period limits (tCH [ABS], tCL [ABS]) are not violated.
11. tHP (MIN) is the lesser of tCL and tCH actually applied to the device CK and CK# inputs; thus, tHP (MIN) >= the lesser of tCL (ABS) MIN and tCH (ABS) MIN.
12. The period jitter (tJITper) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less those than noted in the table (DLL locked).
13. The half-period jitter (tJITdty) applies to either the high pulse of clock or the low pulse of clock; however, the two cumulatively can not exceed tJITper.
14. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next. JEDEC specifies
tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent
less than those noted in the table (DLL locked).
15. The cumulative jitter error (tERRnper), where n is 2, 3, 4, 5, 6–10, or 11–50 is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
16. JEDEC specifies using tERR6–10per when derating clock-related output timing. Axeme requires less derating by allowing tERR5per to be used.
17. This parameter is not referenced to a specific voltage level but is specified when the device output is no longer driving (tRPST) or beginning to drive (tRPRE).

18. The inputs to the DRAM must be aligned to the associated clock, that is, the actual clock that latches it in. However, the input timing (in ns) references to the tCK (AVG) when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the tCK (AVG) rather than tCK: tIPW, tDIPW, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, and tWPRE.
19. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting tERR5per (MAX): tAC (MIN), tDQSCK (MIN), tLZDQS (MIN), tLZDQ (MIN), tAON (MIN); while the following parameters are required to be derated by subtracting tERR5per (MIN): tAC (MAX), tDQSCK (MAX), tHZ (MAX), tLZDQS (MAX), tLZDQ (MAX), tAON (MAX). The parameter tRPRE (MIN) is derated by subtracting tJITper (MAX), while tRPRE (MAX), is derated by subtracting tJITper (MIN). The parameter tRPST (MIN) is derated by subtracting tJITdty (MAX), while tRPST (MAX), is derated by subtracting tJITdty (MIN). Output timings that require tERR5per derating can be observed to have offsets relative to the clock; however, the total window will not degrade.
20. When DQS is used single-ended, the minimum limit is reduced by 100ps.
21. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (tHZ) or begins driving (tLZ).
22. tLZ (MIN) will prevail over a tDQSCK (MIN) + tRPRE (MAX) condition.
23. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
24. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on tDQSS.
25. The intent of the “Don’t Care” state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above VIH[DC]min), then it must not transition LOW (below VIH[DC]) prior to tDQSH (MIN).
26. Referenced to each output group: x4 = DQS with DQ[3:0]; x8 = DQS with DQ[7:0]; x16 = LDQS with DQ[7:0]; and UDQS with DQ[15:8].
27. The data valid window is derived by achieving other specifications: tHP (tCK/2), tDQSQ, and tQH (tQH = tHP - tQHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
28. tQH = tHP - tQHS; the worst case tQH would be the lesser of tCL (ABS) MAX or tCH (ABS) MAX times tCK (ABS) MIN - tQHS. Minimizing the amount of tCH (AVG) offset and value of tJITdty will provide a larger tQH, which in turn will provide a larger valid data out window.
29. This maximum value is derived from the referenced test load. tHZ (MAX) will prevail over tDQSCK (MAX) + tRPST (MAX) condition.
30. The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew rate of 2 V/ns (1 V/ns for each signal). There are two sets of values listed: tDSa, tDHa and tDSb, tDHb. The tDSa, tDHa values (for reference only) are equivalent to the baseline values of tDSb, tDHb at VREF when the slew rate is 2 V/ns, differentially. The baseline values, tDSb, tDHb, are the JEDEC-defined values, referenced from the logic trip points. tDSb is referenced from VIH(AC) for a rising signal and VIL(AC) for a falling signal, while tDHb is referenced from VIL(DC) for a rising signal and VIH(DC) for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated by adding the values. If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended and the baseline values must be derated using. Single-ended DQS data timing

is referenced at DQS crossing VREF.

31. VIL/VIH DDR2 overshoot/undershoot. See AC Overshoot/Undershoot Specification.

32. For each input signal—not the group collectively.

33. There are two sets of values listed for command/address: tISa, tIHa and tISb, tIHb. The tISa, tIHa values (for reference only) are equivalent to the baseline values of tISb, tIHb at VREF when the slew rate is 1 V/ns. The baseline values, tISb, tIHb, are the JEDEC-defined values, referenced from the logic trip points. tISb is referenced from VIH(AC) for a rising signal and VIL(AC) for a falling signal, while tIHb is referenced from VIL(DC) for a rising signal and VIH(DC) for a falling signal. If the command/address slew rate is not equal to 1 V/ns, then the baseline values must be derated by adding the values.

34. This is applicable to READ cycles only. WRITE cycles generally require additional time due to tWR during auto precharge.

35. READs and WRITEs with auto precharge are allowed to be issued before tRAS (MIN) is satisfied because tRAS lockout feature is supported in DDR2 SDRAM.

36. When a single-bank PRECHARGE command is issued, tRP timing applies. tRPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks open. For 8-bank devices (>=1Gb), tRPA (MIN) = tRP (MIN) + tCK (AVG) lists tRP [MIN] + tCK [AVG] MIN).

37. This parameter has a two clock minimum requirement at any tCK.

38. The tFAW (MIN) parameter applies to all 8-bank DDR2 devices. No more than four bank-ACTIVATE commands may be issued in a given tFAW (MIN) period. tRRD (MIN) restriction still applies.

39. The minimum internal READ-to-PRECHARGE time. This is the time from which the last 4-bit prefetch begins to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when tRTP/(2 × tCK) > 1, such as frequencies faster than 533 MHz when tRTP = 7.5ns. If tRTP/(2 × tCK) <= 1, then equation AL + BL/2 applies. tRAS (MIN) has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until tRAS (MIN) has been satisfied.

40. tDAL = (nWR) + (tRP/tCK). Each of these terms, if not already an integer, should be rounded up to the next integer. tCK refers to the application clock period; nWR refers to the tWR parameter stored in the MR9–MR11. For example, -37E at tCK = 3.75ns with tWR programmed to four clocks would have tDAL = 4 + (15ns/3.75ns) clocks = 4 + (4) clocks = 8 clocks.

41. The refresh period is 64ms (commercial) or 32ms (industrial and automotive). This equates to an average refresh rate of 7.8125µs (commercial) or 3.9607µs (industrial and automotive). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms (commercial) or 32ms (industrial and automotive). The JEDEC tRFC MAX of 70,000ns is not required as bursting of AUTO REFRESH commands is allowed.

42. tDELAY is calculated from tIS + tCK + tIH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.

43. tISXR is equal to tIS and is used for CKE setup time during self refresh exit.

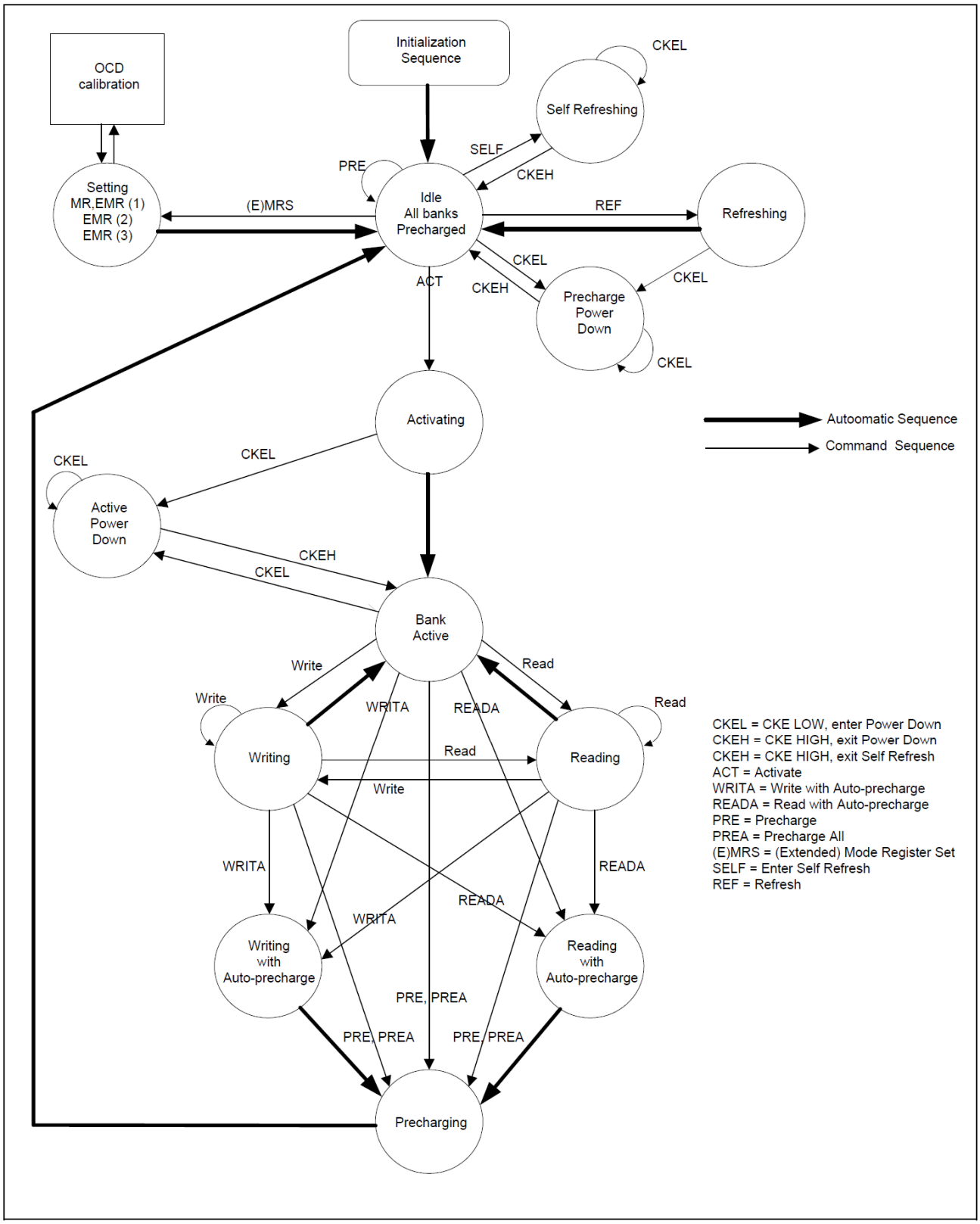
44. tCKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 × tCK + tIH.

45. The half-clock of tAOFD's 2.5 tCK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, tAOFD would actually be 2.5 - 0.03, or 2.47, for tAOF (MIN) and 2.5 + 0.03, or 2.53, for tAOF (MAX).

46. ODT turn-on time tAON (MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turnon time tAON (MAX) is when the ODT resistance is fully on. Both are measured from tAOND.

47. ODT turn-off time tAOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time tAOF (MAX) is when the bus is in High-Z. Both are measured from tAOFD.
48. Half-clock output parameters must be derated by the actual tERR5per and tJITdty when input clock jitter is present; this will result in each parameter becoming larger. The parameter tAOF (MIN) is required to be derated by subtracting both tERR5per (MAX) and tJITdty (MAX). The parameter tAOF (MAX) is required to be derated by subtracting both tERR5per (MIN) and tJITdty (MIN).
49. The -187E maximum limit is 2 × tCK + tAC (MAX) + 1000 but it will likely be 3 x tCK + tAC (MAX) + 1000 in the future.
50. Should use 8 tCK for backward compatibility.
51. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

Simplified State Diagram



Command Truth Table

Function	CKE		CS#	RAS#	CAS#	WE#	BA2–BA0	An–A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
LOAD MODE	H	H	L	L	L	L	BA	OP code			4, 6
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH exit	L	H	H	X	X	X	X	X	X	X	4, 7
			L	H	H	H					
Single bank PRECHARGE	H	H	L	L	H	L	BA	X	L	X	6
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank ACTIVATE	H	H	L	L	H	H	BA	Row address			4
WRITE	H	H	L	H	L	L	BA	Column address	L	Column address	4, 5, 6, 8
WRITE with auto precharge	H	H	L	H	L	L	BA	Column address	H	Column address	4, 5, 6, 8
READ	H	H	L	H	L	H	BA	Column address	L	Column address	4, 5, 6, 8
READ with auto precharge	H	H	L	H	L	H	BA	Column address	H	Column address	4, 5, 6, 8
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
Power-down entry	H	L	H	X	X	X	X	X	X	X	9
			L	H	H	H					
Power-down exit	L	H	H	X	X	X	X	X	X	X	9
			L	H	H	H					

Note1: All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.

Note2: The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.

Note3: "X" means "H or L" (but a defined logic level) for valid IDD measurements.

Note4: BA2 is only applicable for densities >= 1Gb.

Note5: An n is the most significant address bit for a given density and configuration. Some larger address bits may be "Don't Care" during column addressing, depending on density and configuration

Note6: Bank addresses (BA) determine which bank is to be operated upon. BA during a LOAD MODE command selects which mode register is programmed.

Note7: SELF REFRESH exit is asynchronous.

Note8: Burst reads or writes at BL = 4 cannot be terminated or interrupted.

Note9: The power-down mode does not perform any REFRESH operations. The duration of power-down is limited by the refresh requirements outlined in the AC parametric section.

Current State Bank n – Command to Bank n

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVATE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row active	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst)	8
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	9
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst)	8, 10
	L	L	H	L	PRECHARGE (start PRECHARGE)	9
Write (auto pre-charge disa-bled)	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start new WRITE burst)	8
	L	L	H	L	PRECHARGE (start PRECHARGE)	9

Note1: This table applies when CKEn - 1 was HIGH and CKEn is HIGH and after tXSNR has been met (if the previous state was self refresh).

Note2: This table is bank-specific, except where noted (the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.

Note3: Current state definitions:

Idle: The bank has been precharged, tRP has been met, and any READ burst is complete.

Row active: A row in the bank has been activated, and tRCD has been met. No data bursts/ accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated.

Write: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.

Note4: The following states must not be interrupted by a command issued to the same bank. Issue DESELECT or NOP commands, or allowable commands to the other bank, on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table.

Precharge: Starts with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank will be in the idle state.

Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. After tRP is met, the bank will be in the idle state.

Row activate: Starts with registration of an ACTIVATE command and ends when tRCD is met. After tRCD is met, the bank will be in the row active state.

Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. After tRP is met, the bank will be in the idle state.

Note5: The following states must not be interrupted by any executable command (DESELECT or NOP commands must be applied on each positive clock edge during these states):

Refresh: Starts with registration of a REFRESH command and ends when tRFC is met. After tRFC is met, the DDR2 SDRAM will be in the all banks idle state.

Accessing mode register: Starts with registration of the LOAD MODE command and ends when tMRD has been met. After tMRD is met, the DDR2 SDRAM will be in the all banks idle state.

Precharge all: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. After tRP is met,

all banks will be in the idle state.

Note6: All states and sequences not shown are illegal or reserved.

Note7: Not bank-specific; requires that all banks are idle and bursts are not in progress.

Note8: READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.

Note9: May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.

Note10: A WRITE command may be applied after the completion of the READ burst.

Current State Bank n – Command to Bank m

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank *m*	
Row active, active, or precharge	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 9, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	

Note1: This table applies when CKEn - 1 was HIGH and CKEn is HIGH and after tXSNR has been met (if the previous state was self refresh).

Note2: This table describes an alternate bank operation, except where noted (the current state is for bank n and the commands shown are those allowed to be issued to bank m, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

Note3: Current state definitions:

Idle: The bank has been precharged, tRP has been met, and any READ burst is complete.

Row active: A row in the bank has been activated, and tRCD has been met. No data bursts/ accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated.

Write: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.

Read with auto precharge enabled/ Write with auto precharge enabled:

The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For WRITE with auto precharge, the precharge period begins when tWR ends, with tWR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (contention between read data and write data must be avoided).

Note4: REFRESH and LOAD MODE commands may only be issued when all banks are idle.

Note5: Not used.

Note6: All states and sequences not shown are illegal or reserved.

Note7: READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.

Note8: A WRITE command may be applied after the completion of the READ burst.

Note9: Requires appropriate DM.

Note10: The number of clock cycles required to meet tWTR is either two or tWTR/tCK, whichever is greater

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Applying power; if CKE is maintained below 0.2 × VDDQ, outputs remain disabled. To guarantee RTT (ODT resistance) is off, VREF must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined; I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DDR2 SDRAM device latch-up). VTT is not applied directly to the device; however, tVTD should be >=0 to avoid device latch-up. At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as VDD, VDDL, VDDQ, VREF, and VTT are between their minimum and maximum values.

A. Single power source: The VDD voltage ramp from 300mV to VDD,min must take no longer than 200ms; during the VDD voltage ramp, |VDD - VDDQ| <= 0.3V. Once supply voltage ramping is complete (when VDDQ crosses VDD,min).

- VDD, VDDL, and VDDQ are driven from a single power converter output
- VTT is limited to 0.95V MAX
- VREF tracks VDDQ/2; VREF must be within ±0.3V with respect to VDDQ/2 during supply ramp time; does not need to be satisfied when ramping power down
- VDDQ >= VREF at all times

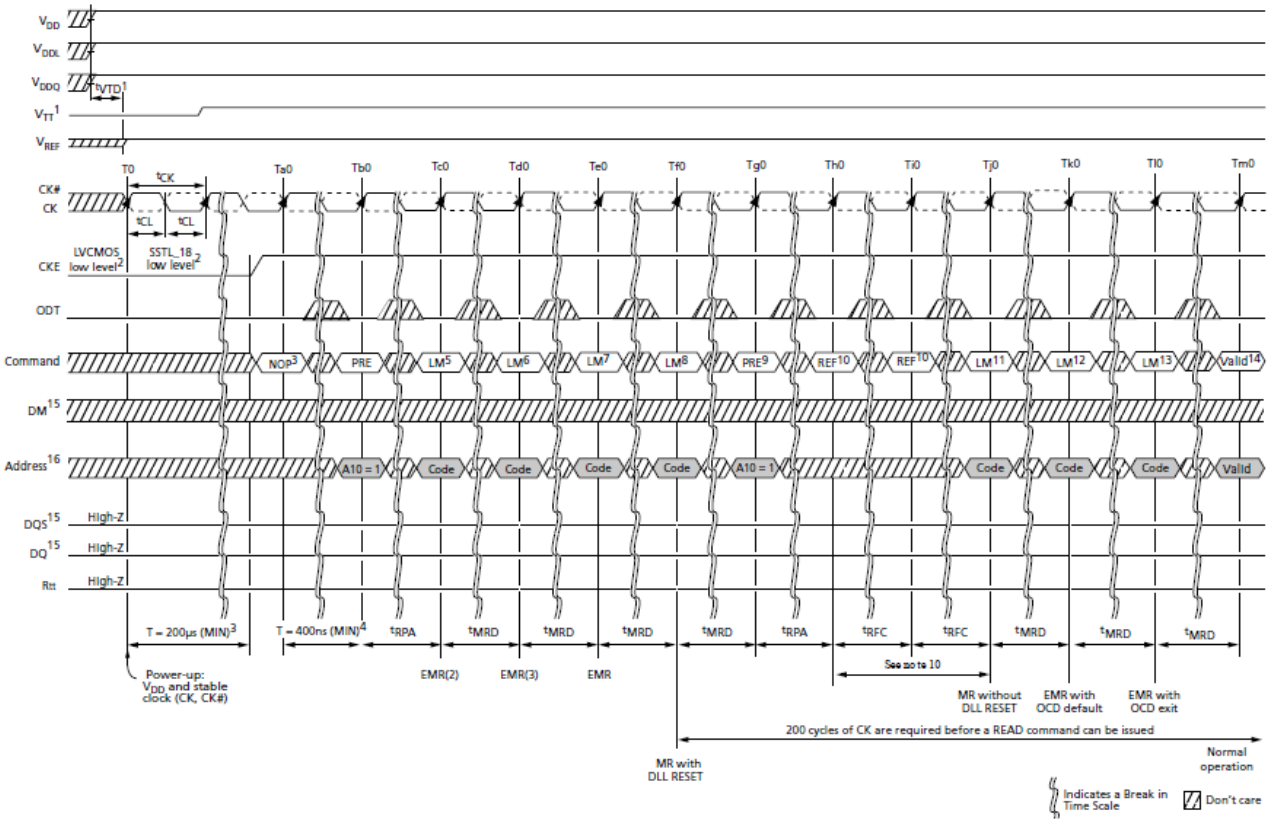
B. Multiple power sources: VDD >= VDDL >= VDDQ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (VDDQ crosses VDD,min). Once supply voltage ramping is complete.

- Apply VDD and VDDL before or at the same time as VDDQ; VDD/VDDL voltage ramp time must be <= 200ms from when VDD ramps from 300mV to VDD,min
- Apply VDDQ before or at the same time as VTT; the VDDQ voltage ramp time from when VDD,min is achieved to when VDDQ,min is achieved must be <= 500ms; while VDD is ramping, current can be supplied from VDD through the device to VDDQ
- VREF must track VDDQ/2; VREF must be within ±0.3V with respect to VDDQ/2 during supply ramp time; VDDQ >= VREF must be met at all times; does not need to be satisfied when ramping power down
- Apply VTT; the VTT voltage ramp time from when VDDQ,min is achieved to when VTT,min is achieved must be no greater than 500ms

2. CKE requires LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to VREF being stable. After state T0, CKE is required to have SSTL_18 input levels. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
3. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
4. Wait a minimum of 400ns then issue a PRECHARGE ALL command.
5. Issue a LOAD MODE command to the EMR(2). To issue an EMR(2) command, provide LOW to BA0, and provide HIGH to BA1; set register E7 to “0” or “1” to select appropriate self refresh rate; remaining EMR(2) bits must be “0”
6. Issue a LOAD MODE command to the EMR(3). To issue an EMR(3) command, provide HIGH to BA0 and BA1; remaining EMR(3) bits must be “0.” Extended Mode Register 3 (EMR3) for all EMR(3) requirements.
7. Issue a LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0; provide HIGH to BA0; bits E7, E8, and E9 can be set to “0” or “1;” recommends setting them to “0;” remaining EMR bits must be “0.” Extended Mode Register (EMR) for all EMR requirements.
8. Issue a LOAD MODE command to the MR for DLL RESET. 200 cycles of clock input is required to lock the DLL. To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1 and BA0; CKE must be HIGH the entire time the DLL is resetting; remaining MR bits must be “0.” Mode Register (MR) for all MR requirements.
9. Issue a precharge all command.

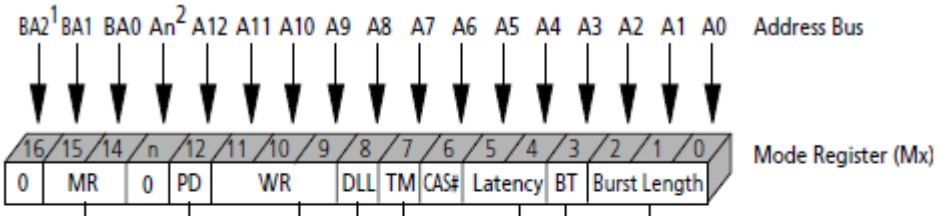
10. Issue 2 or more Auto Refresh commands.
11. Issue a LOAD MODE command to the MR with LOW to A8 to initialize device operation (that is, to program operating parameters without resetting the DLL). To access the MR, set BA0 and BA1 LOW; remaining MR bits must be set to desired settings. Mode Register (MR) for all MR requirements.
12. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to “1,” and then setting all other desired parameters. To access the EMR, set BA0 HIGH and BA1 LOW (see Extended Mode Register (EMR) for all EMR requirements.
13. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to “0,” and then setting all other desired parameters. To access the extended mode registers, EMR, set BA0 HIGH and BA1 LOW for all EMR requirements.
14. The DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at Tf0.
15. DM represents DM for the x4, x8 configurations and UDM, LDM for the x16 configuration; DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16); DQ represents DQ[3:0] for x4, DQ[7:0] for x8 and DQ[15:0] for x16.
16. A10 = PRECHARGE ALL, CODE = desired values for mode registers (bank addresses are required to be decoded).

Reset and Power up initialization sequence



Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR2 SDRAM.
This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and power-down mode. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables must be programmed when the command is issued. The MR is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power (except for bit M8, which is self-clearing).
Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.
The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time tMRD before initiating any subsequent operations such as an ACTIVATE command. Violating either of these requirements will result in an unspecified operation.



M12	PD Mode
0	Fast exit (normal)
1	Slow exit (low power)

M7	Mode
0	Normal
1	Test

M8	DLL Reset
0	No
1	Yes

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency (CL)
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

M15	M14	Mode Register Definition
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

Note1: M16 (BA2) is only applicable for densities >=1Gb, reserved for future use, and must be programmed to “0.”

Note2: Mode bits (Mn) with corresponding address balls (An) greater than M12 (A12) are reserved for future use and must be programmed to “0.”

Note3: Not all listed WR and CL options are supported in any individual speed grade.

Burst Type

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	000	0123	0123
	001	1230	1032
	010	2301	2301
	011	3012	3210
8	000	01234567	01234567
	001	12305674	10325476
	010	23016745	23016745
	011	30127456	32107654
	100	45670123	45670123
	101	56741230	54761032
	110	67452301	67452301
	111	74563012	76543210

Write Recovery

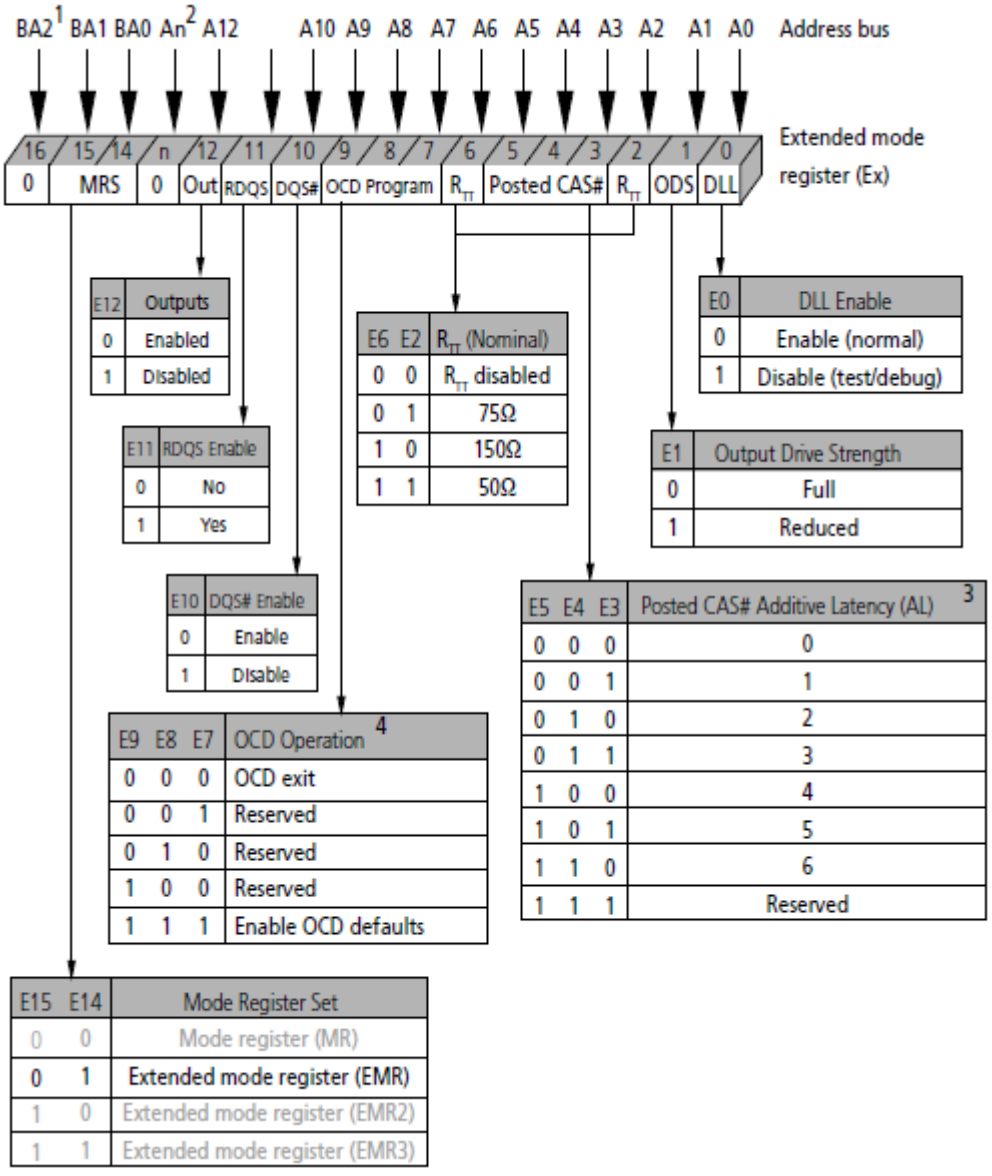
Write recovery (WR) time is defined by bits M9–M11.
The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation.During WRITE with auto precharge operation, the DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of WRITE with auto precharge. WR values of 2, 3, 4, 5, 6, 7, or 8 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing tWR (in nanoseconds) by tCK (in nanoseconds) and rounding up a noninteger value to the next integer; WR (cycles) = tWR (ns)/tCK (ns). Reserved states should not be used as an unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12. PD mode enables the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode. When bit M12 = 0, standard active PD mode, or “fast-exit” active PD mode, is enabled. The tXARD parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.
When bit M12 = 1, a lower-power active PD mode, or “slow-exit” active PD mode, is enabled. The tXARDS parameter is used for slow-exit active PD exit timing. The DLL can be enabled but “frozen” during active PD mode because the exit-to-READ command timing is relaxed. The power difference expected between IDD3P normal and IDD3P lowpower mode is defined in the DDR2 IDD Specifications and Conditions table.

Extend Mode Register EMR

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ondie termination (ODT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. The EMR is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly. The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.



E12	Outputs
0	Enabled
1	Disabled

E11	RDQS Enable
0	No
1	Yes

E10	DQS# Enable
0	Enable
1	Disable

E9	E8	E7	OCD Operation [4]
0	0	0	OCD exit
0	0	1	Reserved
0	1	0	Reserved
1	0	0	Reserved
1	1	1	Enable OCD defaults

E15	E14	Mode Register Set
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

E6	E2	R_{TT} (Nominal)
0	0	R_{TT} disabled
0	1	75Ω
1	0	150Ω
1	1	50Ω

E0	DLL Enable
0	Enable (normal)
1	Disable (test/debug)

E1	Output Drive Strength
0	Full
1	Reduced

E5	E4	E3	Posted CAS# Additive Latency (AL) [3]
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

Note1: E16 (BA2) is only applicable for densities >=1Gb, reserved for future use, and must be programmed to 0.

Note2: Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to 0.

Note3: Not all listed AL options are supported in any individual speed grade.

Note4: As detailed in the Initialization section notes, during initialization of the OCD operation, all three bits must be set to 1 for the OCD default state, then set to 0 before initialization is finished.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LM command. These specifications are applicable when the DLL is enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the LM command. The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation. Anytime the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters. Anytime the DLL is disabled and the device is operated below 25 MHz, any AUTO REFRESH command should be followed by a PRECHARGE ALL command.

Output Drive Strength

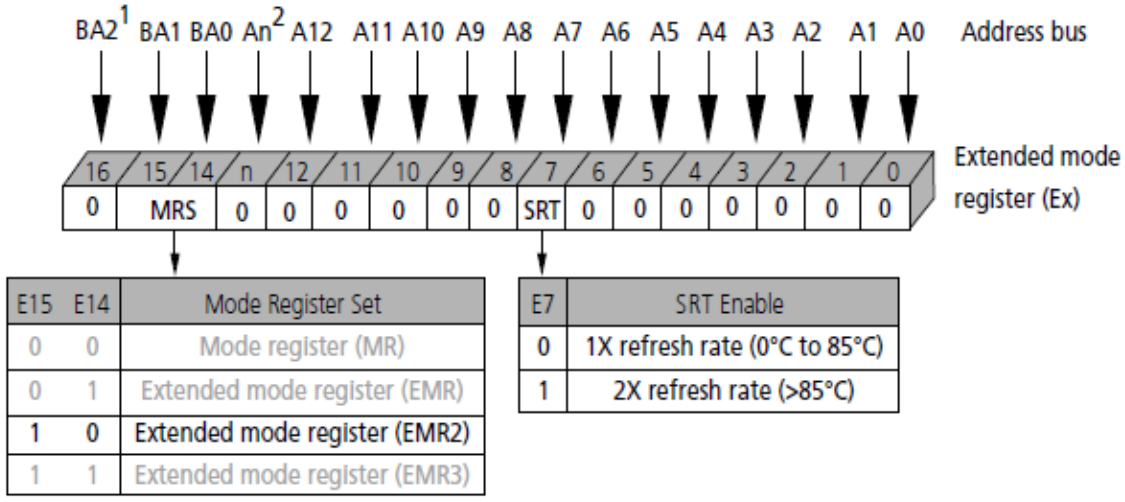
The output drive strength is defined by bit E1. The normal drive strength for all outputs is specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 45 to 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-topoint environments.

Output Eable/Disable

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 38. When enabled (E12 = 0), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during IDD characterization of read current.

Extend Mode Register2 EMR2

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, except for E7, which is used in commercial or high-temperature operations. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly. Bit E7 (A7) must be programmed as 1 to provide a faster refresh rate on IT and AT devices if TC exceeds 85°C. EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.



E15	E14	Mode Register Set
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

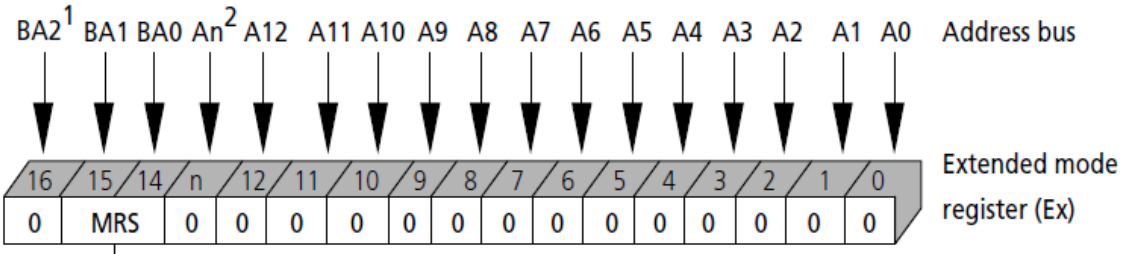
E7	SRT Enable
0	1X refresh rate (0°C to 85°C)
1	2X refresh rate (>85°C)

Note1: E16 (BA2) is only applicable for densities >=1Gb, reserved for future use, and must be programmed to 0.

Note2: Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to 0.

Extend Mode Register3 EMR3

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly. EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.



E15	E14	Mode Register Set
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

Note1: E16 (BA2) is only applicable for densities ..1Gb, is reserved for future use, and must be programmed to 0.

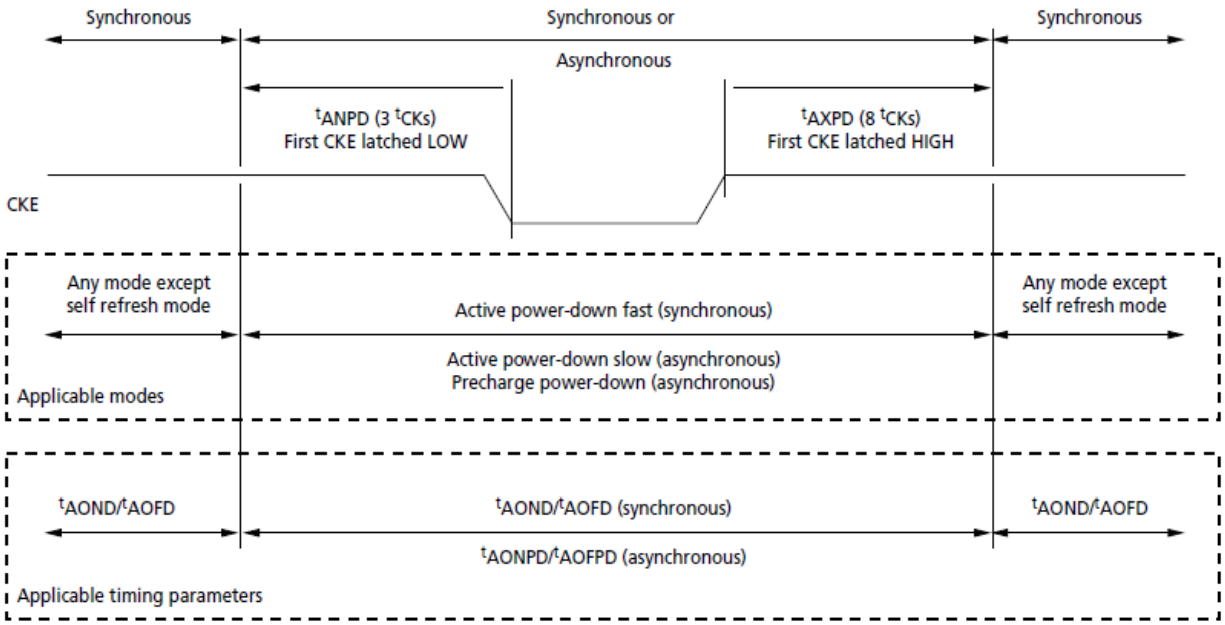
Note2: Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to 0.

On-Die Termination (ODT)

ODT effective resistance, RTT(EFF), is defined by bits E2 and E6 of the EMR. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. RTT effective resistance values of 50Ω,75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/ LDQS#, DM, and UDM/LDM signal. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off sw1, sw2, or sw3. The ODT effective resistance value is selected by enabling switch sw1, which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω(RTT2 [EFF] = R2/2). Similarly, if sw2 is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω(RTT2[EFF] = R2/2). Switch sw3 enables R1 values of 100Ω, enabling effective resistance of 50Ω. Reserved states should not be used, as an unknown operation or incompatibility with future versions may result. The ODT control ball is used to determine when RTT(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation.

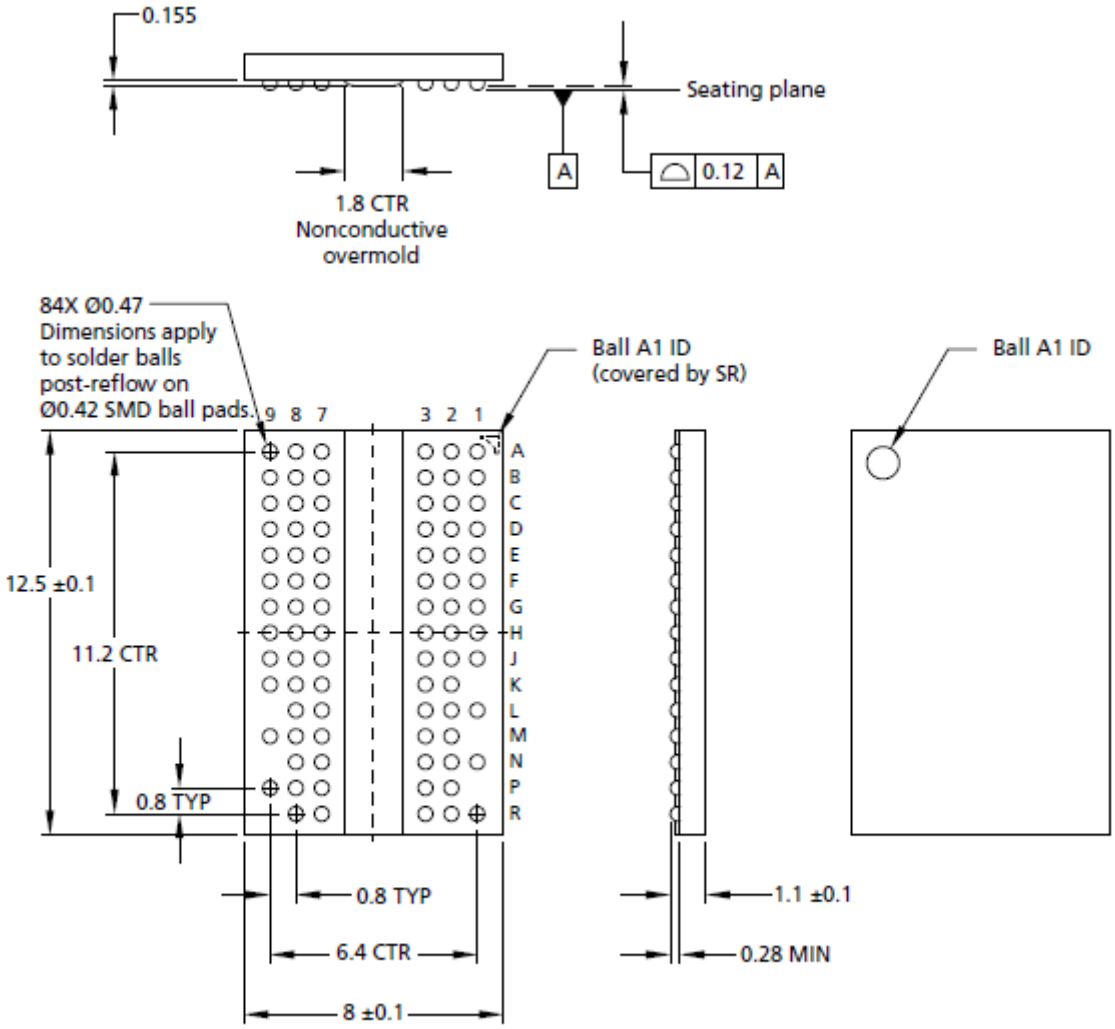
ODT must be turned off prior to entering self refresh mode. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until the EMR command is issued. This will enable the ODT feature, at which point the ODT ball will determine the RTT(EFF) value. Anytime the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled for ODT timing diagrams).

ODT Timing for Entering and Exiting Power-Down Mode



Package Description: 84Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	July. 2019	Rico Yang	N/A
1.0	First SPEC. release.	July. 2019	Rico Yang	N/A