1G-Bit 3.3V NAND FLASH MEMORY

Descriptions

Offered in 128Mx8bit, the H7A11G21F1CX is a 1G-bit NAND Flash Memory with spare 32M-bit. The device is offered in 3.3V VCC. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 400us on the (2K+64)Byte page and an erase operation can be performed in typical 4.5ms on a (128K+4K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The H7A11G21F1CX is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable app. lications requiring non-volatility..

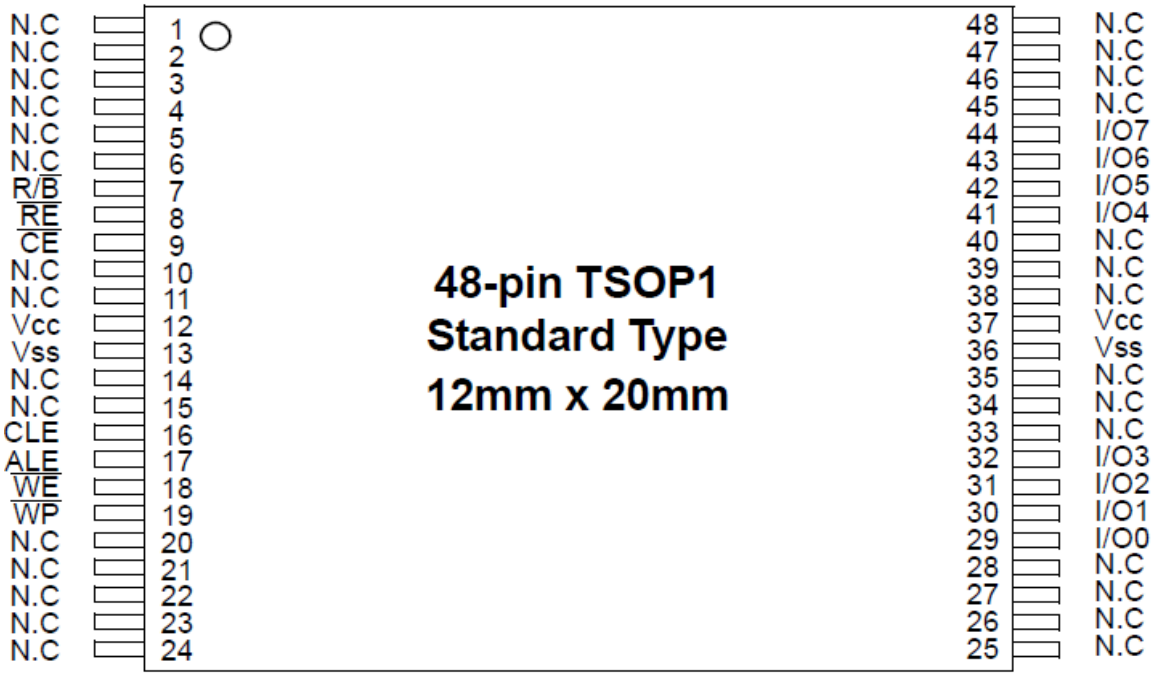
Features

- **Basic Features**
  - Density : 1Gbit
  - Vcc : 3.3V(2.7V to 3.6V)
  - Bus width : x8
  - Operating temperature
    Commercial: 0˚C to 70˚C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - Memory Cell Array : (128M + 4M) x 8bit
  - Page size : (2K + 64) Byte
  - Data Register : (2K + 64) x 8bit
  - Block Erase :(128K + 4K) Byte
- **Automatic Program and Erase**
  - Page Program :(2K + 64) Byte
- **Page Read Operation**
  - Random Read : 25us(Max.)
  - Serial Access : 25ns(Min.)
  - Data Transfer Rate : SDR 20Mhz(40Mbps)
- **Fast Write Cycle Time**
  - Page Program time : 400us(Typ.)
  - Block Erase Time : 4.5ms(Typ.)
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
  - Program/Erase Lockout During Power Transitions
- **Command Driven Operation**
- **Unique ID for Copyright Protection**
- **Package:**
  - 48 - Pin TSOP1 (12 x 20/0.5 mm pitch)
  - Pb-Free, Halogen-Free Package

Ordering Information

Part No	Density	Organization	Package	Grade
H7A11G21F1CX	1G-bit/128M-byte	X8	48-Pin TSOP1 12x20mm	Commercial

Pin Assignment



48-pin TSOP1

Pin Description (Simplified)

48-pin TSOP1,12x20mm		
Pin Name	**I/O**	**Function**
#WP	Input	Write Protect
ALE	Input	Address Latch Enable
#CE	Input	Chip Enable
#WE	Input	Write Enable
RY#BY	Output	Ready/Busy Output
#RE	Input	Read Enable
CLE	Input	Command Latch Enable
I/O[0-7]	Input / Output	Data Input / Output (x8)
V_{cc}	Supply	Device Power Supply
V_{SS}	Supply	Ground
N.C	-	Not Connect

Note: Connect all VCC and VSS pins of each device to common power supply outputs.

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Voltage on any pin relative to VSS	V_{cc}	-0.6 ~ 4.6	V
	V_{in}	-0.6 ~ 4.6	V
	$V_{I/O}$	-0.6 to Vcc +0.3 (< 4.6V)	V
Storage Temperature	T_{STG}	-65 ~ 150	˚C
Temperature Under Bias	T_{BIAS}	-10 ~125	˚C
Short circuit output current	I_{os}	5	mA

Note 1: Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.

Note 2: Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

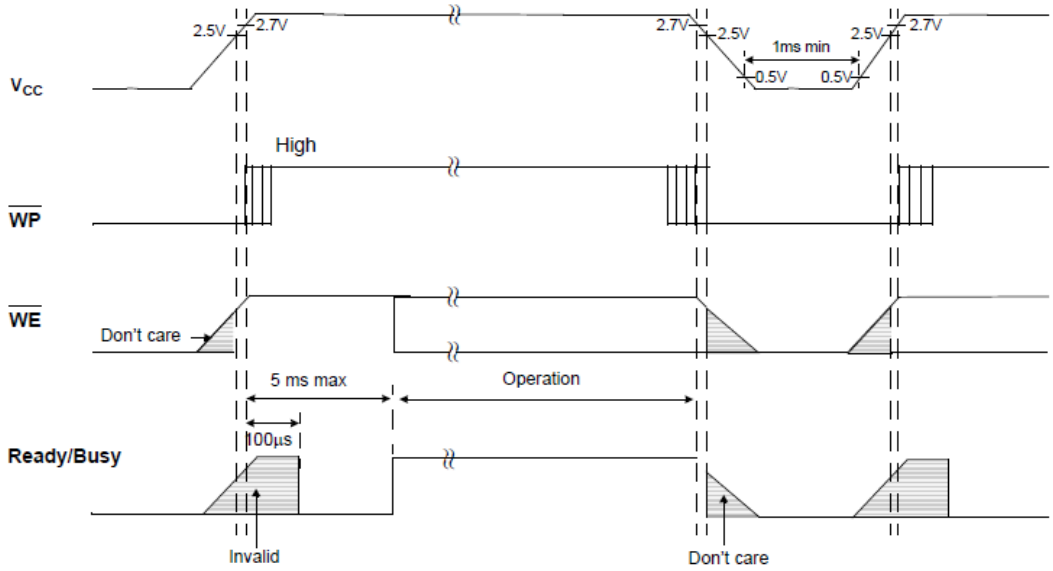
Note 3: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Ranges

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	Vcc	2.7	3.3	3.6	V
Ground Supply Voltage	Vss	0	0	0	V
Ambient Temperature, Operating	Ta	0	-	70	˚C

Data Protection & Device Power-up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions.
An internal voltage detector disables all functions whenever VCC is below about 2V(3.3V device).
#WP pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down.
A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown below. The two step command sequence for program/erase provides additional software protection.



AC Waveforms for Power Transition

DC Characteristics

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	

Page Read Access Operation Current	Icc1	tRC= 25ns
		#CE=VIL
		IOUT=0mA
			-	15	30	mA

Program current	Icc2	-	-	15	30	mA
Erase current	Icc3	-	-	15	30	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	70	uA
Input leakage current	ILI	VIN= 0V to Vcc(max)	-	-	+/-10	uA
Output leakage current	ILO	VOUT=0V to Vcc(max)	-	-	+/-10	uA
Input high voltage(1)	VIH	-	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage(1)	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage	VOH	IOH=-400µA	2.4	-	-	V
Output low voltage	VOL	IOL=2.1mA	-	-	0.4	V
Output low current	IOL(RY/#BY)	VOL=0.4V	8	10	-	mA

Note 1: VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20ns or less.

Note 2: Typical value is measured at VCC=3.3V, TA=25°C. Not 100% tested..

AC Measurement Conditions

Parameter	Symbol	Spec.		Unit
		MIN	Max	
Input Capacitance(1), (2)	CIN	-	8	pF
Input/Output Capacitance(1), (2)	CIO	-	8	pF
Input Rise and Fall Times	-	-	5	ns
Input Pulse Level	-	0 to VCC		V
Input/Output timing Level	-	Vcc/2		V
Output load	-	1TTL GATE and CL=50pF		-

Note 1: Capacitance is periodically sampled and not 100% tested.

Note 2: Test conditions TA=25'C, f=1MHz, VIL/VIN=0V

Read / Program / Erase Characteristics

Parameter	Symbol	Spec.			Unit
		MIN	Typ.	MAX	
Data Transfer from Cell to Register	tR	-		25	us
Program Time	tPROG	-	400	900	us
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	tBEARS	-	4.5	16	ms

Note: 1. Typical value is measured at VCC=3.3V, TA=25'C. Not 100% tested.

Note: 2. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V VCC and 25'C temperature.

AC Timing Parameters Table

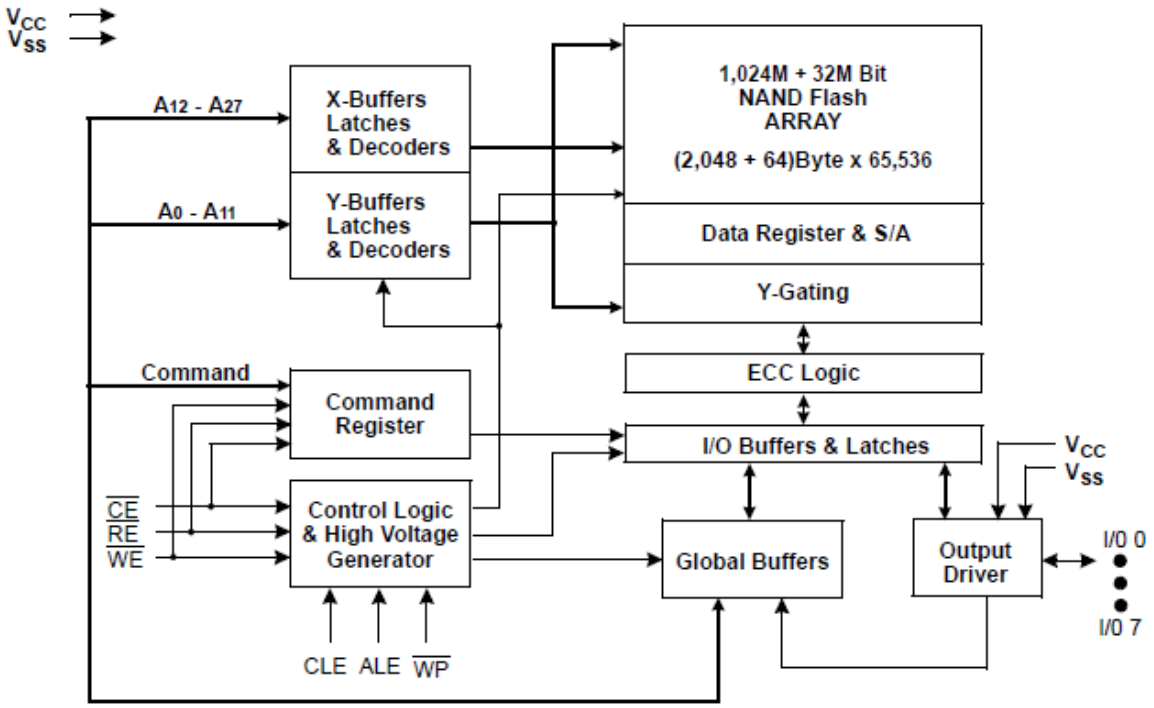
Parameter	Symbol	Spec.		Unit
		MIN	MAX	
CLE Setup Time(1)	tCLS	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE Setup Time(1)	tCS	20	-	ns
CE Hold Time	tCH	5	-	ns
WE Pulse Width	tWP	12	-	ns
ALE Setup Time(1)	tALS	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time(1)	tDS	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE High Hold Time	tWH	10	-	ns
Address to Data Loading Time(2)	tADL	100	-	ns
ALE to RE Delay	tAR	10	-	ns
CLE to RE Delay	tCLR	10	-	ns
Ready to RE Low	tRR	20	-	ns
RE Pulse Width	tRP	12	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	25	-	ns
RE Access Time	tREA	-	20	ns
CE Access Time	tCEA	-	25	ns
RE High to Output Hi-Z	tRHZ	-	100	ns
CE High to Output Hi-Z	tCHZ	-	30	ns
CE High to ALE or CLE Don't Care	tCSD	0	-	ns
RE High to Output Hold	tRHOH	15	-	ns
Data Hold Time after CE Disable	tCOH	15	-	ns
RE High Hold Time	tREH	10	-	ns
Output Hi-Z to RE Low	tIR	0	-	ns
RE High to WE Low	tRHW	100	-	ns
WE High to RE Low	tWHR	60	-	ns
Device Resetting Time (Read/Program/Erase)(1)	tRST	-	5/10/500	us

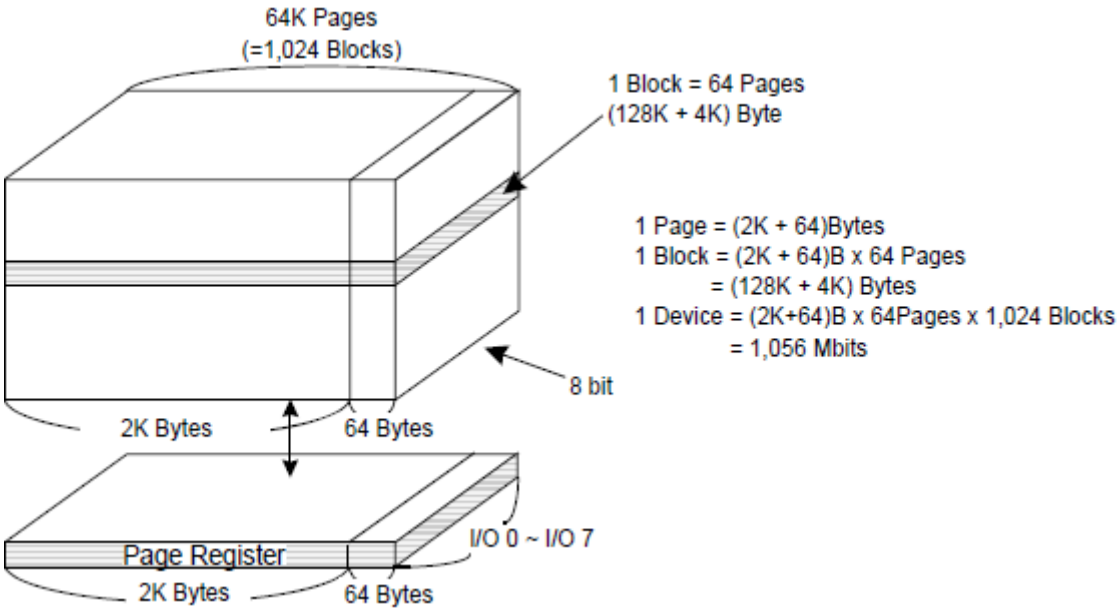
Note 1: The transition of the corresponding control pins must occur only once while #WE is held low.

Note 2: tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.

Note 3: If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

Block Diagram and Array Organization





	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27

Note : * L must be set to "Low".

* The device ignores any additional input of address cycles than required.

Mode Selection Table

Mode		CLE	ALE	#CE	#WE	#RE	#WP
Read Mode	Command input	H	L	L	⎍	H	X
	Address input(4 cycles)	L	H	L	⎍	H	X
Write Mode	Command input	H	L	L	⎍	H	H
	Address input(4 cycles)	L	H	L	⎍	H	H
Data input		L	L	L	⎍	H	H
Data output		L	L	L	H	⎍	X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X*	X	X	X	L
Standby		X	X	H	X	X	0V/ Vcc

Note 1: X* can be VIL or VIH.

Note 2: #WP should be biased to CMOS HIGH or LOW for standby.

Command Sets

Command	1st Cycle	2nd Cycle	Acceptable during busy
PAGE READ	00h	30h	
READ for COPY BACK	00h	35h	
READ ID	90h	-	
RESET	FFh	-	Yes
PAGE PROGRAM	80h	10h	
PROGRAM for COPY BACK	85h	10h	
BLOCK ERASE	60h	D0h	
RANDOM DATA INPUT(1)	85h	-	
RANDOM DATA OUTPUT(1)	05h	E0h	
READ STATUS	70h	-	Yes
ECC READ STATUS	7Ah		

Note 1: RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.

Note 2: Any commands that are not in the above table are considered as undefined and are prohibited as inputs.

Valid Block

Parameter	Symbol	Min	Max	Unit
H7A11G21F1CX	Nvb	1004	1024	blocks

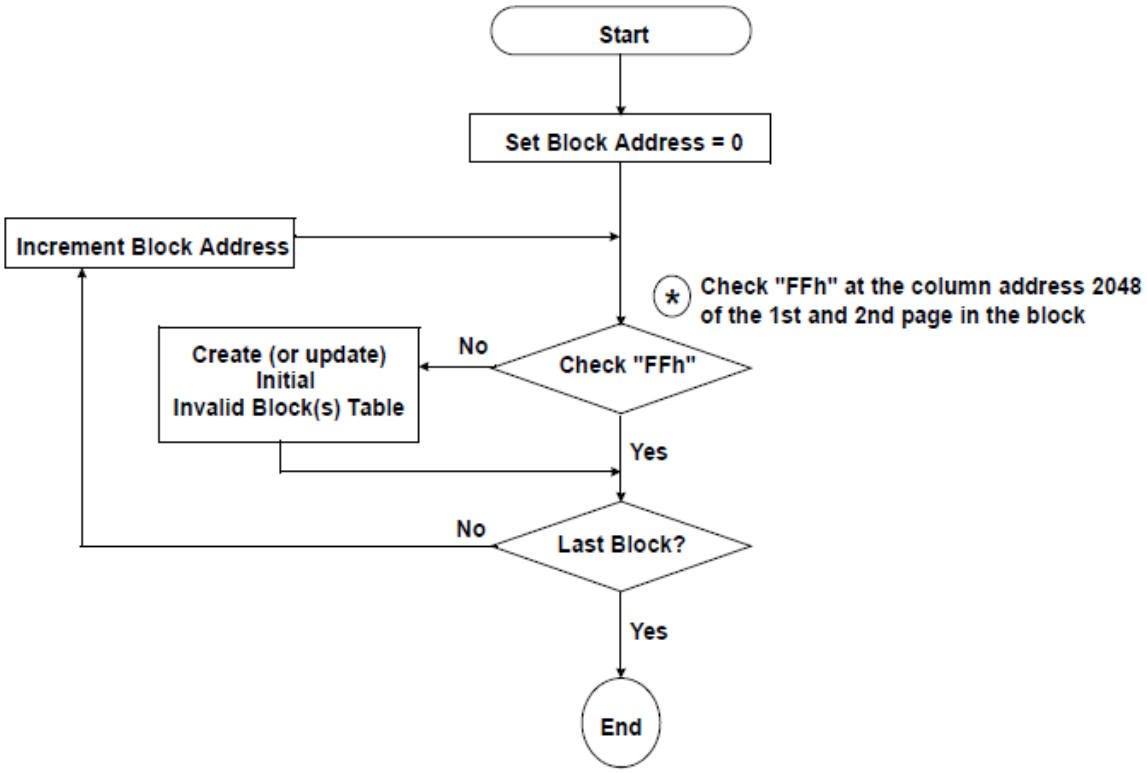
Note: The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks

Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Axeme. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

Identifying Initial Invalid Blocks

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Axeme makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Below). Any intentional erasure of the original initial invalid block information is prohibited.

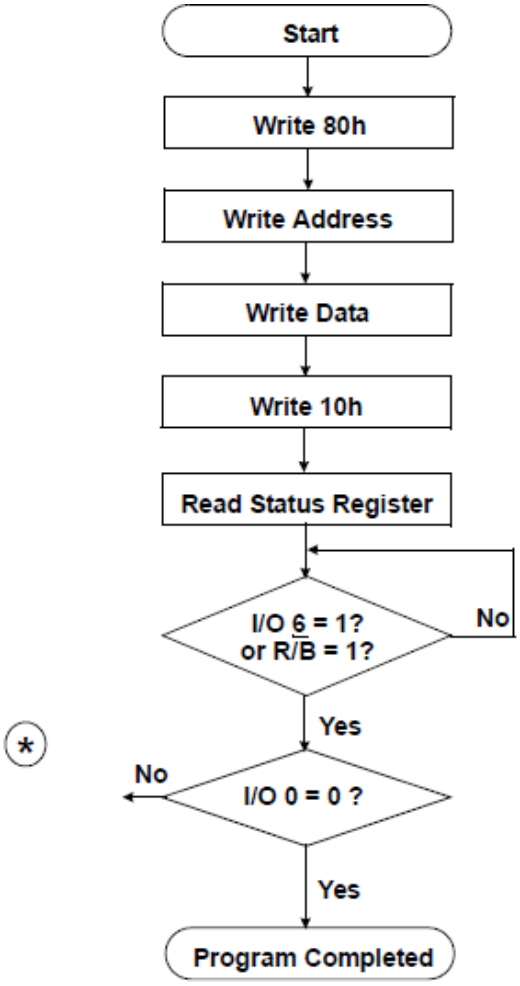


flow chart to create initial invalid block table

Error in operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

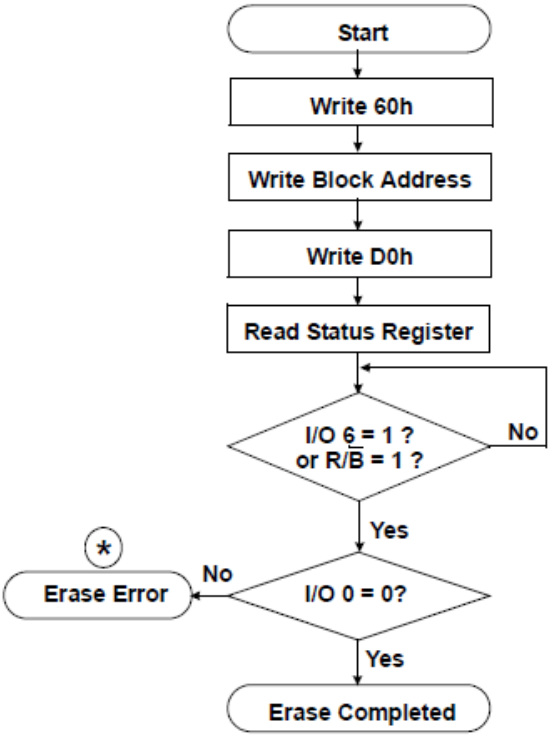
Failure Mode		Detection and countermeasure procedure
Write	Erase Failure	Status read after erase → Block Replacement
	Program Failure	Status read after program → Block Replacement
Read	Single bit Failure	Verify ECC → ECC correction



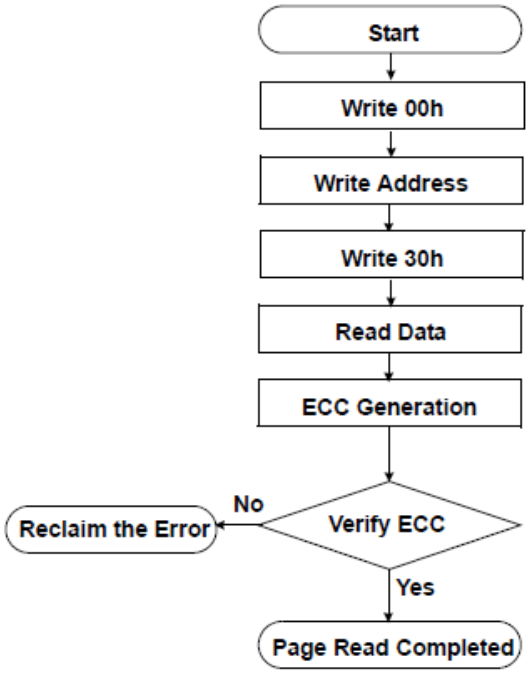
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Program Flow Chart

Erase Flow Chart

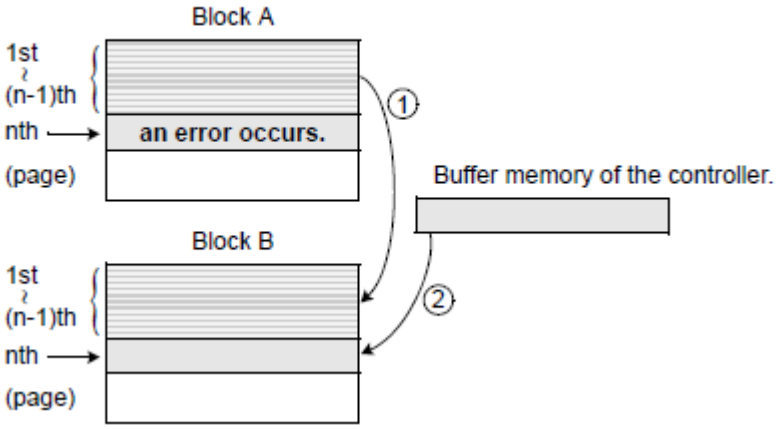


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



Step 1: When an error happens in the nth page of the Block 'A' during erase or program operation.

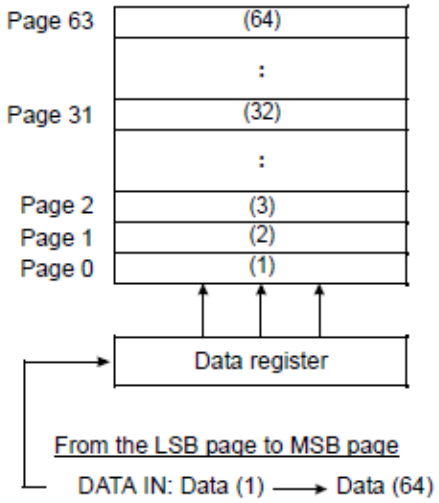
Step 2: Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')

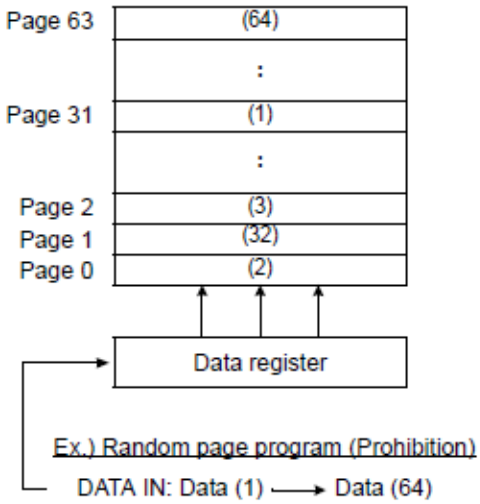
Step 3: Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.

Step 4: Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing in program operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed.Therefore, LSB doesn't need to be page 0.





I/O	DATA	ADDRESS			
I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2
I/O 0 ~ I/O 7	2112 Byte	A0 ~ A7	A8 ~ A11	A12 ~ A19	A20 ~ A27

Page Read Operation

Page read is initiated by writing 00h-30h to the command register along with four address cycles. After initial power up, 00h command is latched. Therefore only four address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

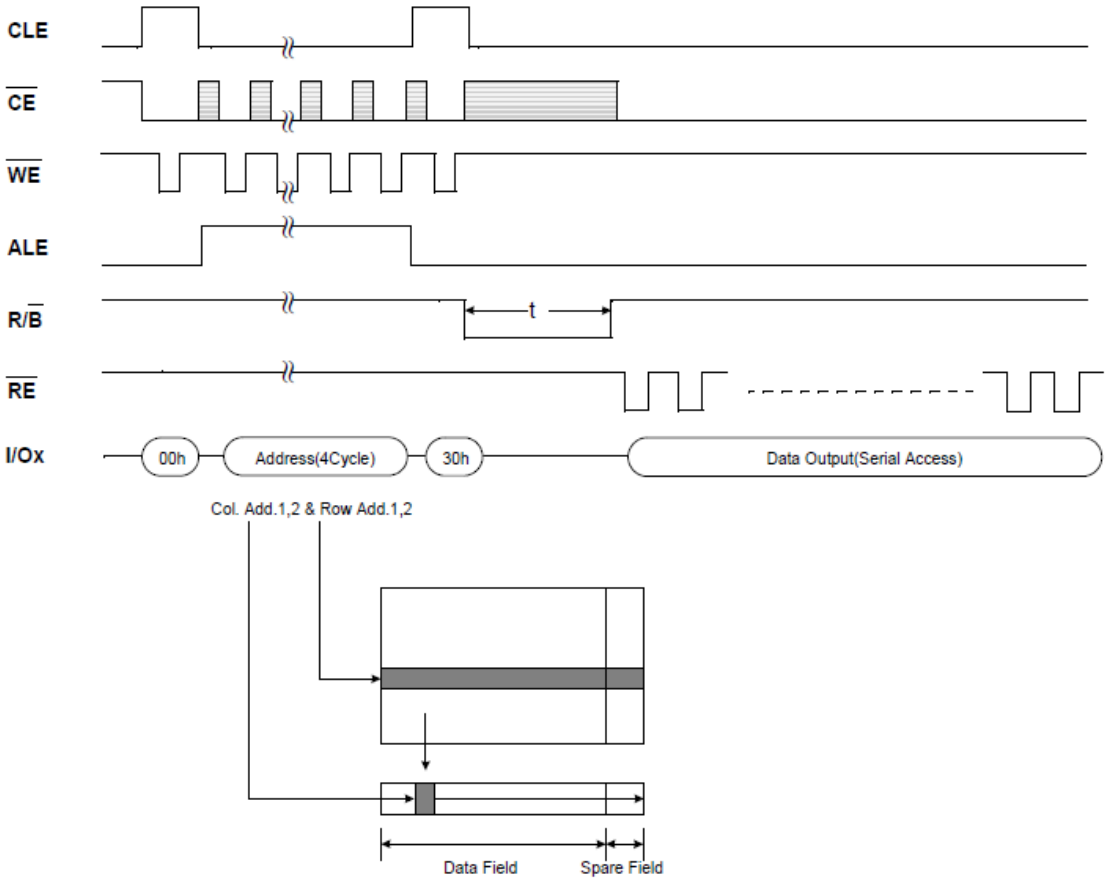


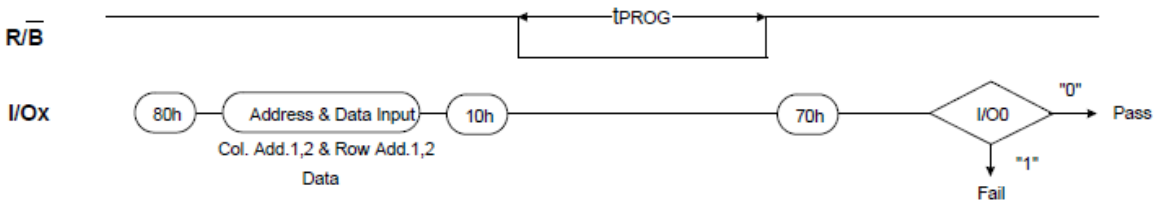
Figure 8. Page Read Sequence

Page Program Operation

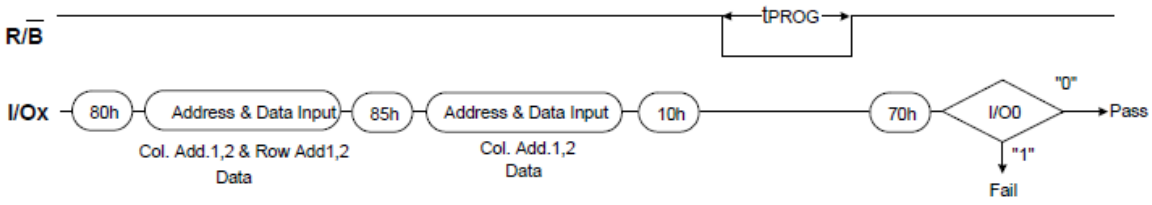
The device is programmed basically on a page basis, and each page shall be programmed only once before being erased.The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command(10h) initiates the programming process.

Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.



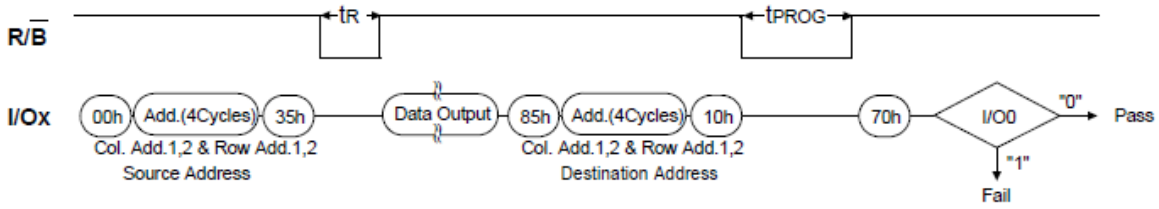
Page Program Sequence



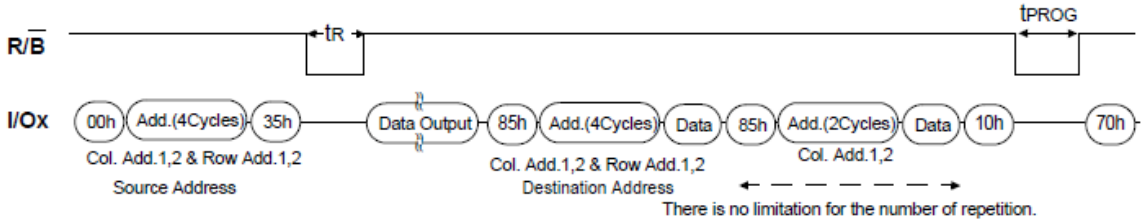
Program Operation with Random Data Input Sequence

Copy-Back Program Operation

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register.



Copy-Back Program Sequence

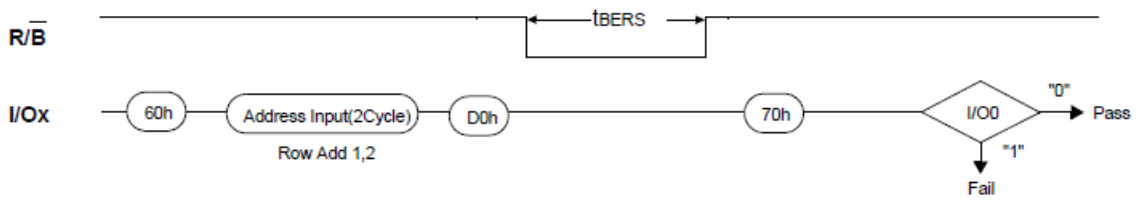


Copy-Back Program with Random Data Input Sequence

Block Erase Operation

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A18 to A27 is valid while A12 to A17 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.



Read Status

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to below Table for specific Status Register definitions. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles

I/O	Page Program	Block Erase	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared
I/O 2	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Normal or uncorrectable / Recommended to rewrite	Chip Read Status Normal or uncorrectable : 0 Recommended to rewrite : 1
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :

1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

ECC Read Status

Using the ECC Read Status function, the Error Correction Status can be identified.
ECC is performed on the NAND Flash main and spare areas.
The ECC Read Status function also shows the number of errors in a sector as identified from a ECC check during a read operation.

7	6	5	4	3	2	1	I/O0
Sector Information				ECC Status			

ECC Status

I/O3 to I/O0	ECC Status
0000	No Error
0001	1bit error (Correctable)
0010	2bit error (Correctable)
0011	3bit error (Correctable)
0100	4bit error (Correctable)
Others	Reserved

Sector Information

I/O7 to I/O4	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Others	Reserved

ECC Sector Information

ECC is generated by internal ECC logic during program operation.
During Read operation, the device automatically executes ECC. After read operation is executed, read status command can be issued to identify the read status the read status remains unmodified until other valid commands are executed.

2KByte Page Assignment

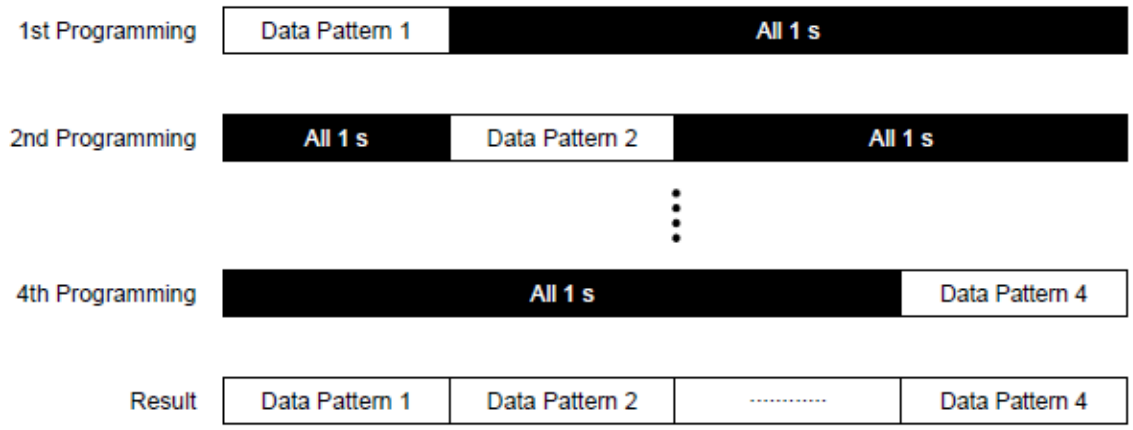
1'st Main	2'nd Main	3'rd Main	4'th Main	1'st Spare	2'nd Spare	3'rd Spare	4'th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Definition of 528Byte Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field
1'st Sector	0 ~ 511	2,048 ~ 2,063
2'nd Sector	512 ~ 1,023	2,064 ~ 2,079
3'rd Sector	1,024 ~ 1,535	2,080 ~ 2,095
4'th Sector	1,536 ~ 2,047	2,096 ~ 2,111

NOTE :
1) The Internal ECC manages all data of Main area and Spare area.
2) A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

Partial Page Program Information



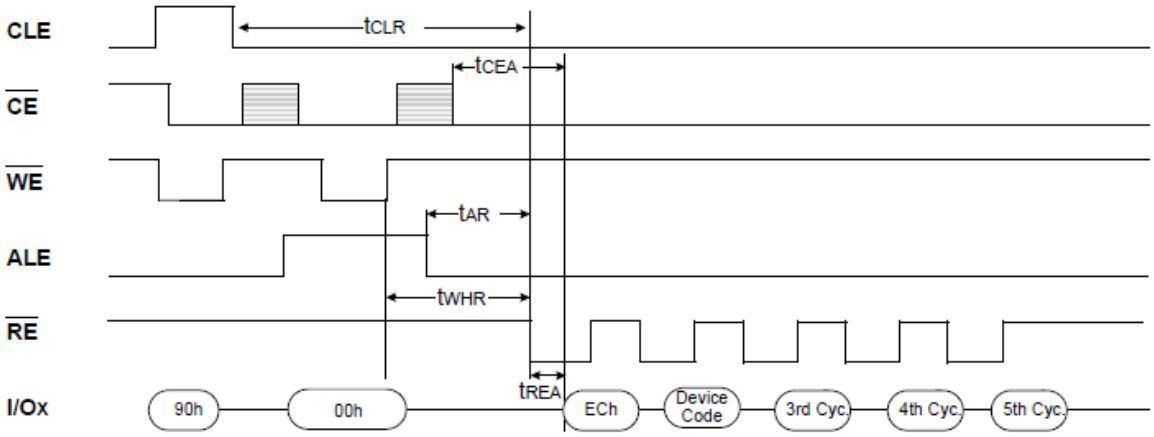
NOTE :

1) A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

Read ID

00h Address ID Definition

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.



00h Address ID Cycle

Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
F1h	00h	95h	42h

00 Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc
4th Byte	Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum
5th Byte	Plane Number, Plane Size

3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

4th ID Data

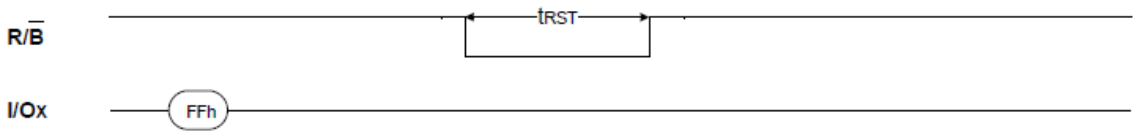
	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Redundant Area Size (byte/512byte)	8 16					0 1	
Organization	x8 x16		0 1				
Serial Access Minimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		

5th ID Data

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1	I/O0
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			
Proccess	21nm 1ynm reserved reserved				0 1 0 1	1 0 0 1
Reserved		0			0	0

Reset Operation

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written.

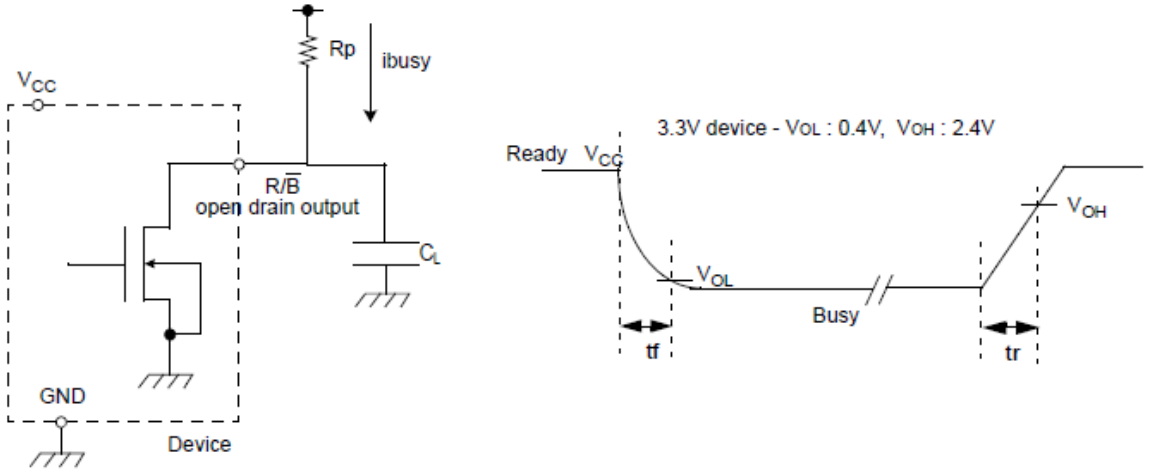


Device Status

	After Power-up	After Reset
Operation mode Mode	00h Command is latched	Waiting for next command

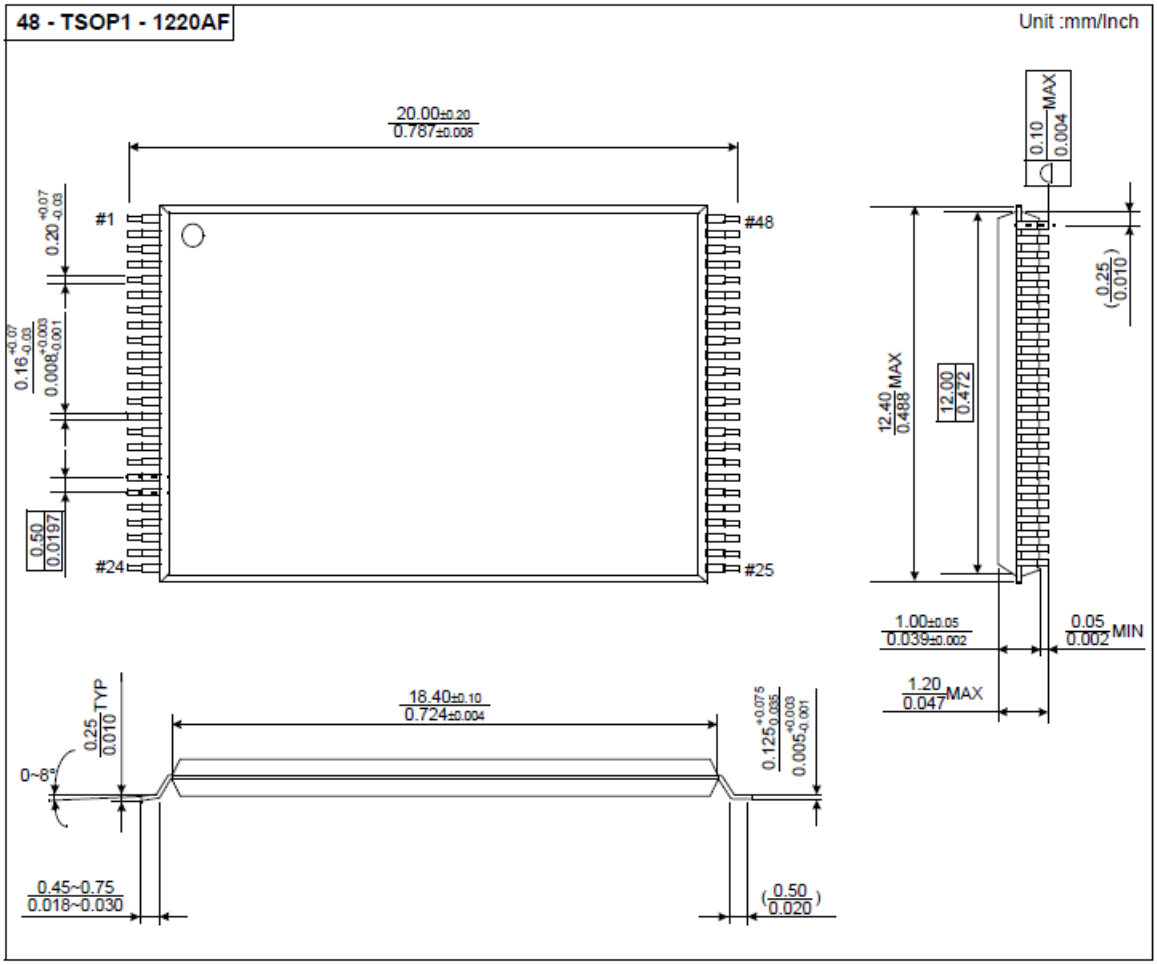
Ready/ Busy

The device has a R/ $\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/ $\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/ $\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/ $\overline{B}$) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference char. Its value can be determined by the following guidance.



Package Description

TSOP 48-pin 12x20mm



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2018	Rico Yang	N/A
1.0	First SPEC. Release.	Aug. 2018	Rico Yang	N/A