32Gb (128Mx8Banks×32)
Low Power DDR4 SDRAM

Descriptions

H2AB32G32D6C uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. Each command uses one clock cycle,during which command information is transferred on both the positive and negative edge of the clock. To achieve high-speed operation,our H2AB32G32D6C SDRAM adopt 16n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the H2AB32G32D6C effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal SDRAM core and eight corresponding n-bit wide,one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the H2AB32G32D6C are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For H2AB32G32D6C devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Features

- Bidirectional, data strobe (DQS,/DQS) is transmitted/ received with data, to be used in capturing data at the receiver
- Differential clock inputs (CK and /CK)
- Differential data strobe (DQS and /DQS)
- Commands & addresses entered on both positive & negative CK edge; data and data mask referenced to both edges of DQS
- Eight internal banks for concurrent operation
- Data mask (DM) for write data
- Programmable Burst Lengths: 16,32
- Burst type: Sequential or interleave
- Programmable RL (Read latency) & WL (Write latency)
- Clock Stop capability during idle period
- Auto Pre-charge for each burst access
- Configurable Drive Strength (DS)
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR)
- Deep Power Down Mode (DPD)
- VDD2/VDDCA/VDDQ= 1.06~1.17V; VDD1= 1.70~1.95V

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2AB32G32D6CIAAC	1024M X 32	LP DDR4-2400	200Ball BGA,10x14.5mm	Commercial
H2AB32G32D6CKAAC	1024M X 32	LP DDR4-3200		Commercial

Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			ZQ1	V_{DD2}	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMI0_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	ZQ2	V_{SS}
H	V_{DD2}	CA0_A	CS1_A	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	V_{SS}	CKE0_A	CKE1_A			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	CS2_A			CKE2_A	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	CS2_B			CKE2_B	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	CKE1_B			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	CS1_B	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_c_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_c_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_t_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	DNU	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

Top View (ball down)

DDR4_A (Channel A) DDR4_B (Channel B) ZQ, ODT_CA, RESET Supply Ground

200-Ball FBGA

Pin Description (Simplified)

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE1_A, CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals,input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B,CS1_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to VSS (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU		Do not use: Must be grounded or left floating.
NC		No connect: Not internally connected.

Absolute Maximum Rating

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Voltage on any ball relative to VSS	-0.4 ~ 1.5	V
V_{DD1}	VDD1 supply voltage relative to VSS	-0.4 ~ 2.1	V
V_{DD2}	VDD2 supply voltage relative to VSS	-0.4 ~ 1.5	V
V_{DDQ}	VDDQ supply voltage relative to VSS	-0.4 ~ 1.5	V
T_{STG}	Storage Temperature (plastic)	-55 ~ 125	˚C

Note 1: For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.

Note 2: Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Units
C_{CK}	Input capacitance, CK_t and CK_c	0.5	0.9	pF
C_{DCK}	Input capacitance delta, CK_t and CK_c	0	0.09	pF
C_{I}	I Input capacitance, all other input-only pins	0.5	0.9	pF
C_{DI}	Input capacitance delta, all other input-only pins	-0.1	0.1	pF
C_{IO}	Input/output capacitance, DQ, DMI, DQS_t, DQS_c	0.7	1.3	pF
C_{DDQS}	Input/output capacitance delta, DQS_t, DQS_c	0	0.1	pF
C_{DIO}	Input/output capacitance delta, DQ, DMI	-0.1	0.1	pF
C_{ZQ}	Input/output capacitance, ZQ pin	0	5.0	pF

Note 1: This parameter is not subject to production testing. It is verified by design and characterization.

Note 2: Absolute value of CKCK_t – CKCK_c

Note 3: CI applies to CS, CKE, RESET_n, and CA[5:0].

Note 4: CDI = CI – 0.5 × (CCK_t + CKCK_c); it does not apply to CKE, RESET_n, or ODT(ca).

Note 5: DMI loading matches DQ and DQS.

Note 6: MR3 I/O configuration for pull-up/pull-down drive strength OP[5:0] = 000000b (RZQ/7).

Note 7: Absolute value of CDQS_t and CDQS_c.

Note 8: CDIO = CIO – 0.5 × (CDQS_t + CDQS_c) in byte-lane.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V
V_{DD2}	Core Supply voltage 2	1.06	1.10	1.17	V
V_{DDQ}	I/O buffer power	1.06	1.10	1.17	V

Notes: 1. VDD1 uses significantly less power than VDD2.

Notes: 2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

Notes: 3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

DC Characteristics

(IDD Specifications; VDD2, VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V)

Symbol		Supply	Data Rate	Unit
			3200	
IDD0	IDD01	VDD1	7	mA
	IDD02	VDD2	80	
	IDD0Q	VDDQ	1.5	
IDD2P	IDD2P1	VDD1	2	mA
	IDD2P2	VDD2	3.5	
	IDD2PQ	VDDQ	1.5	
IDD2PS	IDD2PS1	VDD1	2	mA
	IDD2PS2	VDD2	3.5	
	IDD2PSQ	VDDQ	1.5	
IDD2N	IDD2N1	VDD1	2	mA
	IDD2N2	VDD2	45	
	IDD2NQ	VDDQ	1.5	
IDD2NS	IDD2NS1	VDD1	2	mA
	IDD2NS2	VDD2	25	
	IDD2NSQ	VDDQ	1.5	
IDD3P	IDD3P1	VDD1	2	mA
	IDD3P2	VDD2	10	
	IDD3PQ	VDDQ	1.5	
DD3PS	IDD3PS1	VDD1	2	mA
	IDD3PS2	VDD2	10	
	IDD3PSQ	VDDQ	1.5	
IDD3N	IDD3N1	VDD1	4	mA
	IDD3N2	VDD2	57	
	IDD3NQ	VDDQ	1.5	
IDD3NS	IDD3NS1	VDD1	4	mA
	IDD3NS2	VDD2	40	
	IDD3NSQ	VDDQ	1.5	
IDD4R	IDD4R1	VDD1	5	mA
	IDD4R2	VDD2	450	
	IDD4RQ	VDDQ	270	
IDD4W	IDD4W1	VDD1	5	mA
	IDD4W2	VDD2	350	
	IDD4WQ	VDDQ	100	

DC Characteristics(Continued)

(IDD Specifications; VDD2, VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V)

Symbol		Supply	Speed	Unit
			3200	
IDD5	IDD51	VDD1	20	mA
	IDD52	VDD2	170	
	IDD5Q	VDDQ	1.5	
IDD5AB	IDD5AB1	VDD1	4	mA
	IDD5AB2	VDD2	60	
	IDD5ABQ	VDDQ	1.5	
IDD5PB	IDD5PB1	VDD1	4	mA
	IDD5PB2	VDD2	60	
	IDD5PBQ	VDDQ	1.5	

Notes: 1. IDD values reflect dual-channel operation with the same pattern for each channel.

Notes: 2. Published IDD values except ID4RQ are the maximum of the distribution of the arithmetic mean. Refer to another note for IDD4RQ.

Notes: 1. IDD4RQ value is reference only. Typical value. DBI Disabled, VOH = VDDQ/3, Tc = 25°C

IDD6 Partial Array Self-refresh current; VDD2,VDDQ= 1.06~1.17V, VDD1 = 1.70~1.95V

PASR	Supply	Temp.		Unit
		25°C	85°C	
Full Array	VDD1	0.4	2.2	mA
	VDD2	0.7	7	
	VDDQ	0.1	1.5	

Notes: 1. IDD values reflect dual-channel operation with the same pattern for each channel.

Notes: 2. IDD6 25°C is the typical, and IDD6 85°C is the maximum of the distribution of the arithmetic mean.

Single-Ended AC and DC Output Levels – ODT Enable

VOH Level	Rx Termination (Nom)	VOH(DC) Accuracy			Unit
		Min.	Typ.	Max.	
VDDQ/3	RZQ/1 (240Ω)	0.9	1.0	1.1	VOH
	RZQ/2 (120Ω)				
	RZQ/3 (80Ω)				
	RZQ/4 (60Ω)				
	RZQ/5 (48Ω)				
	RZQ/6 (40Ω)				
VDDQ/2.5	RZQ/1 (240Ω)	0.85	1.0	1.15	
	RZQ/2 (120Ω)				
	RZQ/3 (80Ω)				

Note 1: VOH is the calibration comparison point. The output driver calibrates to the VOH level ±10%.

Note 2: Rx termination values must be set using the MRW command before ZQCal.

Note 3: ZQCal is valid for any Rx termination value given the same VOH level. If the VOH level is changed, ZQCal must be retrained.

Differential Output Slew Rate

Parameter	Symbol	Value		Unit
		Min.	Max.	
Differential output slew rate (VOH = VDDQ/3)	SRQdiff	7	18	V/ns

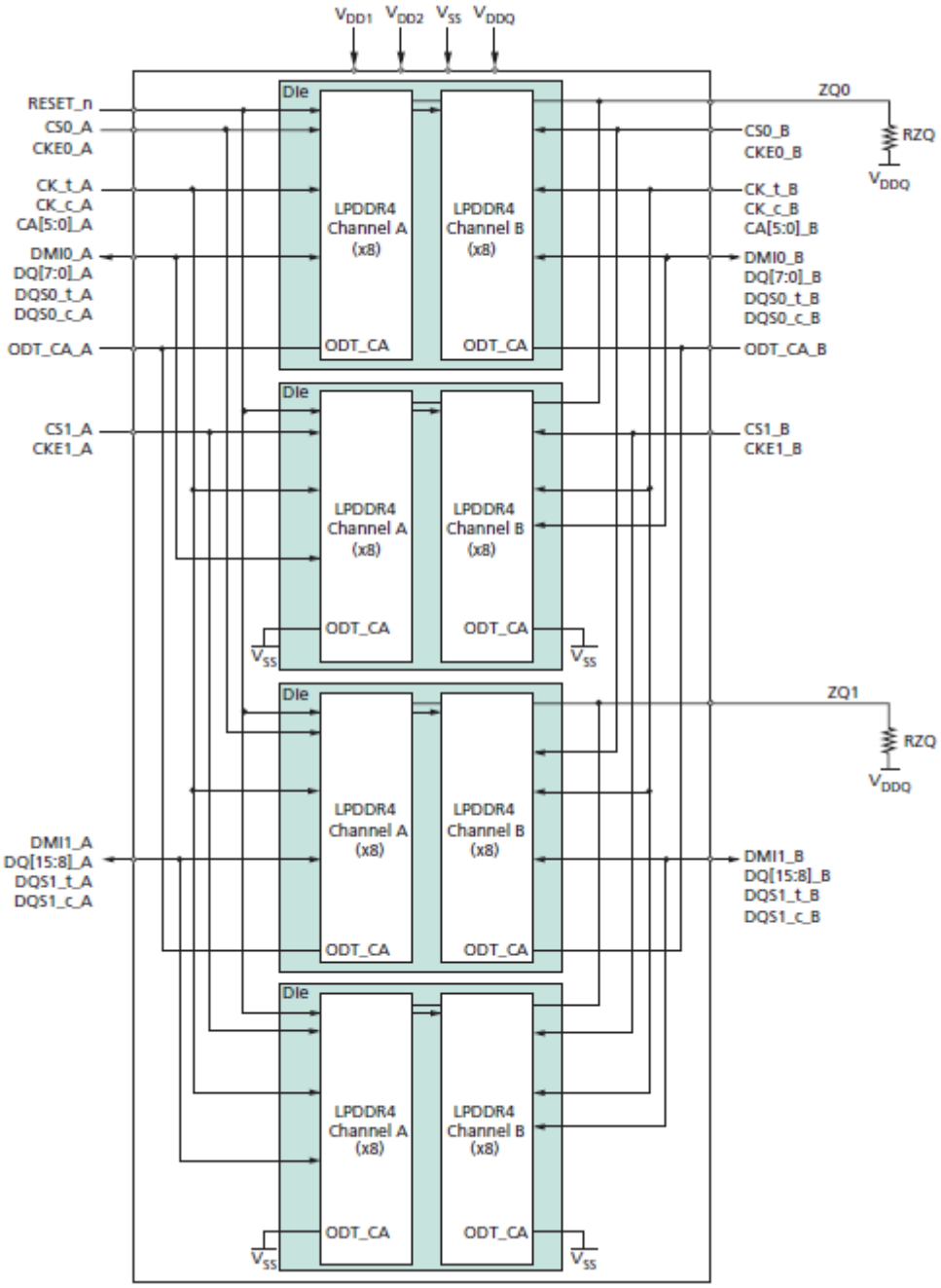
Note 1: SR = Slew rate; Q = Query output; se = Differential signal

Note 2: Measured with output reference load.

Note 3: The output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2 × VOH(DC) and VOH(AC) = 0.8 × VOH(DC).

Note 4: Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.

Block Diagram – Quad-Die, Dual-Channel Package



AC Characteristics

(V_{DD2}, V_{DDQ}, V_{DDCA} =1.06~1.17V, V_{DD1} =1.70~1.95V)

Symbol	Parameter	Min/Max	Data Rate		Unit
			2400	3200	
Clock Timing					
$t_{CK(avg)}$	Average clock period	Min	840	625	ps
		Max	100	100	ns
$t_{CH(avg)}$	Average HIGH pulse width	Min	0.46	0.46	$t_{CK(avg)}$
		Max	0.54	0.54	$t_{CK(avg)}$
$t_{CL(avg)}$	Average LOW pulse width	Min	0.46	0.46	$t_{CK(avg)}$
		Max	0.54	0.54	$t_{CK(avg)}$
$t_{CK(abs)}$	Absolute clock period	Min	$t_{CK(avg)}$ MIN + $t_{JIT(per)}$ MIN		ps
$t_{CH(abs)}$	Absolute clock HIGH pulse width	Min	0.43	0.43	$t_{CK(avg)}$
		Max	0.57	0.57	$t_{CK(avg)}$
$t_{CL(abs)}$	Absolute clock LOW pulse width	Min	0.43	0.43	$t_{CK(avg)}$
		Max	0.57	0.57	$t_{CK(avg)}$
$t_{JIT(per)}$, allowed	Clock period jitter	Min	-	-40	ps
		Max	-	40	ps
$t_{JIT(cc)}$, allowed	Maximum clock jitter between two consecutive clock cycles (with clock period jitter)	Max	-	80	ps

AC Characteristics (Continued)

(V_{DD2}, V_{DDQ}, V_{DDCA} =1.06~1.17V, V_{DD1} =1.70~1.95V)

Symbol	Parameter	Min/ Max	Data Rate		Unit
			2400	3200	
ZQ Calibration Parameters					
tZQCAL	ZQCAL START to ZQCAL LATCH command interval	Min	1		us
tZQLAT	ZQCAL LATCH to next valid command interval	Min	MAX(30ns, 8nCK)		ns
tZQRESET	ZQCAL RESET to next valid command interval	Min	MAX(50ns, 3nCK)		ns
READ Parameters					
tDQSCK	DQS output access time from CK	Min	1500		ps
		Max	3500		ps
tDQSCK_VOLT	DQS output access time from CK_t/CK_c – voltage variation	Max	7		ps/mV
tDQSCK_TEMP	DQS output access time from CK_t/CK_c – temperature variation	Max	4		ps°/C
tDQSCK_rank2rank	CK to DQS rank to rank variation	Max	1.0		ns
tDQSQ	DQS-DQ skew	Max	0.18		UI
tQH	DQ output hold time total from DQS_t, DQS_c	Min	Min (tQSH, tQSL)		ps
tRPRE	READ preamble	Min	1.8		tCK(avg)
tRPST	READ postamble	Min	0.4		tCK(avg)
tLZ(DQS)	DQS Low-Z from clock	Min	(RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200ps		ps
tLZ(DQ)	DQ Low-Z from clock	Min	(RL x tCK) + tDQSCK(Min) - 200ps		ps
tHZ(DQS)	DQS High-Z from clock	Min	(RL x tCK) + tDQSCK(Max)+(BL/2 x tCK) + (tRPST(Max) x tCK) - 100ps		ps
tHZ(DQ)	DQ High-Z from clock	Max	t(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps		ps
tQW_total	Data output valid window time total, per pin	Min	0.73	0.68	UI
tDQSQ_DBI	DQS_t, DQS_c to DQ skew total, per group, per access	Max	0.18		UI
tQH_DBI	DQ output hold time total from DQS_t, DQS_c	Min	MIN(tQSH_DBI, tQSL_DBI)		ps
tQW_total_DBI	Data output valid window time total, per pin	Min	0.73	0.68	UI
tQSL	DQS_t, DQS_c differential output LOW time	Min	tCL(abs) – 0.05		tCK(avg)
tQSH	DQS_t, DQS_c differential output HIGH time	Min	tCH(abs) – 0.05		tCK(avg)
tQSL-DBI	DQS_t, DQS_c differential output LOW time	Min	tCL(abs) – 0.045		tCK(avg)
tQSH-DBI	DQS_t, DQS_c differential output HIGH time	Min	tCH(abs) – 0.045		tCK(avg)

AC Characteristics (Continued)

(V_{DD2}, V_{DDQ}, V_{DDCA} =1.06~1.17V, V_{DD1} =1.70~1.95V)

Symbol	Parameter	Min/ Max	Data Rate		Unit
			2400	3200	
CKE Input Parameters					
tCKE	CKE minimum pulse width(HIGH and LOW pulse width)	Min	Max(7.5ns, 4nCK)		ns
tCMDCKE	Delay from valid command to CKE input LOW	Min	Max(1.75ns, 3nCK)		ns
tCKELCK	Valid clock requirement after CKE input LOW	Min	MAX(5ns, 5nCK)		ns
tCSCKE	Valid CS requirement before CKE input LOW	Min	1.75		ns
tCKELCS	Valid CS requirement after CKE input LOW	Min	MAX(5ns, 5nCK)		ns
tCKCKEH	Valid Clock requirement before CKE Input HIGH	Min	MAX(1.75ns, 3nCK)		ns
tXP	Exit power-down to next valid command delay	Min	MAX(7.5ns, 5nCK)		ns
tCSCKEH	Valid CS requirement before CKE input HIGH	Min	1.75		ns
tCKEHCS	Valid CS requirement after CKE input HIGH	Min	MAX(7.5ns, 5nCK)		ns
tMRWCKEL	Valid clock and CS requirement after CKE input LOW after MRW command	Min	MAX(14ns, 10nCK)		ns
tZQCKE	Valid clock and CS requirement after CKE input LOW after ZQ calibration start command	Min	MAX(1.75ns, 3nCK)		ns
Command Address Input Parameters					
tcIVW	Command/address valid window	Min	0.3		tCK(avg)
tcIPW	Address and control input pulse width	Min	0.6		tCK(avg)
Boot Parameters (10–55 MHz)					
tCKb	Clock cycle time	Max	100		ns
		Min	18		ns
tDQSCKb	DQS output data access time from CK	Min	1		ns
		Max	10		ns
tDQSQb	Data strobe edge to output data edge	Max	1.2		ns
Mode Register Parameters					
tMRW	MODE REGISTER WRITE command period	Min	MAX(10ns, 10nCK)		ns
tMRR	MODE REGISTER READ command period	Min	8		tCK(avg)
tMRRI	Additional time after tXP has expired until MRR command may be issued	Min	tRCD(min) + 3nCK		ns
tSDO	Delay from MRW command to DQS driven out	Max	MAX(12nCK, 20ns)		ns

AC Characteristics (Continued)

(V_{DD2}, V_{DDQ}, V_{DDCA} =1.06~1.17V, V_{DD1} =1.70~1.95V)

Symbol	Parameter	Min/Max	Data Rate		Unit
			2400	3200	
Core Parameters					
RL-A	READ latency (DBI disabled)	Min	22	28	tCK(avg)
RL-B	READ latency (DBI enabled))	Min	25	32	tCK(avg)
WL-A	WRITE latency (Set A)	Min	11	14	tCK(avg)
WL-B	WRITE latency (Set B)	Min	20	26	tCK(avg)
tRC	ACTIVATE-to-ACTIVATE command period	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge		ns
tSR	Minimum self refresh time (entry to exit)	Min	MAX(15ns, 3nCK)		ns
tXSR	Self refresh exit to next valid command delay	Min	MAX(tRFCab + 7.5ns, 2nCK)		ns
tCCD	CAS-to-CAS delay	Min	8		tCK(avg)
tCCDMW	CAS-to-CAS delay masked write	Min	32		tCK(avg)
tRTP	Internal READ to PRECHARGE command delay	Min	Max (7.5ns, 8nCK)		ns
tRCD	RAS-to-CAS delay	Min	Max (18ns, 4nCK)		ns
tRPpb	Row precharge time (single bank)	Min	Max (18ns, 3nCK)		ns
tRPpab	Row precharge time (all banks)	Min	Max (21ns, 3nCK)		ns
tRAS	Row active time	Min	Max (42ns, 3nCK)		ns
		Max	MIN(9 × tREFI × Refresh Rate1, 70.2)		us
tWR	WRITE recovery time	Min	Max (18ns, 4nCK)		ns
tWTR	WRITE-to- READ command delay	Min	Max (10ns, 8nCK)		ns
tRRD	Active bank A to active bank B	Min	Max (10ns, 4nCK)		ns
tPPD	Precharge-to-precharge delay	Min	4		tCK(avg)
tFAW	Four-bank activate window	Min	40		ns
tESCKE	Delay from SRE command to CKE input LOW	Min	MAX(1.75ns, 3nCK)		-

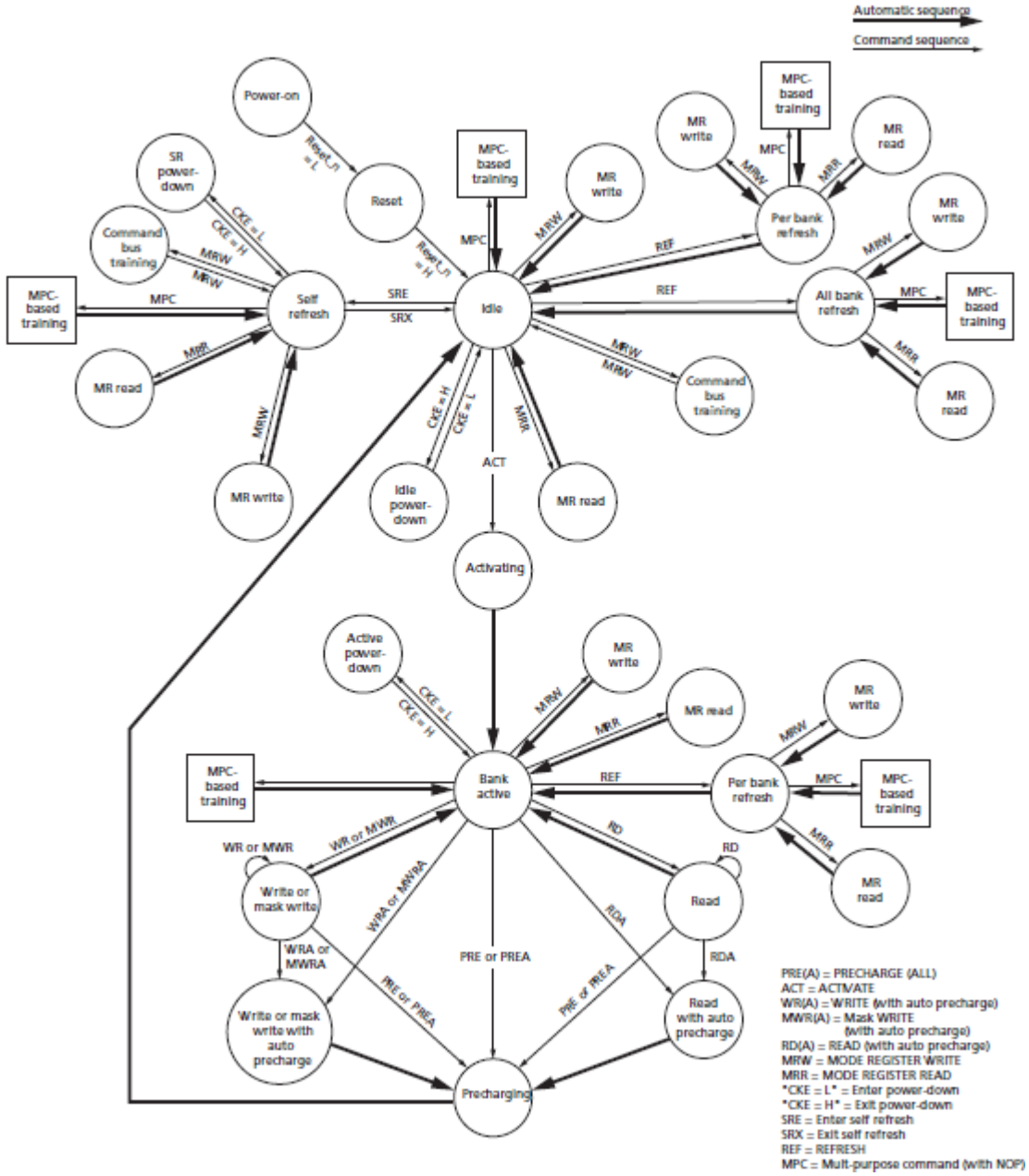
AC Characteristics (Continued)

(V_{DD2}, V_{DDQ}, V_{DDCA} =1.06~1.17V, V_{DD1} =1.70~1.95V)

Symbol	Parameter	Min/Max	Data Rate		Unit
			2400	3200	
CA Training Parameters					
tCKELCK	Valid clock requirement after CKE Input LOW	Min	MAX(5ns, 5nCK)		tCK
tDStrain	Data setup for VREF training mode	Min	2		ns
tDHtrain	Data hold for VREF training mode	Min	2		ns
tADR	Asynchronous data read y	Max	20		ns
tCACD	CA BUS TRAINING command-to-command delay	Min	RU(tADR/tCK)		tCK
tDQSCKE	Valid strobe requirement before CKE LOW	Max	10		ns
tCAENT	First CA BUS TRAINING command following CKE LOW	Min	250		ns
tVREFca_LONG	VREF step time – multiple steps	Max	250		ns
tVREFca_SHORT	VREF step time – one step	Max	80		ns
tCKPRECS	Valid clock requirement before CS HIGH	Min	2tCK + tXP		-
tCKPSTCS	Valid clock requirement after CS HIGH	Min	MAX(7.5ns, 5nCK)		-
tCS_VREF	Minimum delay from CS to DQS toggle in command bus training	Min	2		tCK
tCKEHDQS	Minimum delay from CKE HIGH to strobe High-Z	Min	10		ns
tMRZ	CA bus training CKE HIGH to DQ tri-state	Min	1.5		ns
tCKELODTon	ODT turn-on latency from CKE	Min	20		ns
tCKEHODToff	ODT turn-off latency from CKE	Min	20		ns
Write Voltage and Timing					
TdIVW_total	Rx timing window total at VdIVW voltage levels	Max	0.22	0.25	UI
TdIVW_1-bit	Rx timing window 1-bit toggle (at VdIVW voltage levels)	Max	TBD		UI

TdIPW	DQ and DMI input pulse width (at VCENT_DQ)	Min	0.45	UI
tDQS2DQ	DQ-to-DQS offset	Min	200	ps
		Max	800	
tDQDQ	DQ-to-DQ offset	Max	30	ps
tDQS2DQ_temp	DQ-to-DQS offset temperature variation	Max	0.6	ps/°C
tDQS2DQ_volt	DQ-to-DQS offset voltage variation	Max	33	ps/50mV
tDQSS	WRITE command to first DQS transition	Min	0.75	tCK(avg)
		Max	1.25	
tDQSH	DQS input HIGH-level width	-	0.4	tCK(avg)
tDQSL	DQS input LOW-level width	Min	0.4	tCK(avg)
tDSS	DQS falling edge to CK setup time	Min	0.2	tCK(avg)
tDSH	DQS falling edge from CK hold time	Min	0.2	tCK(avg)
tWPST	Write postamble	Min	0.4 (or 1.4 if extra postamble is programmed in MR)	tCK(avg)
tWPRE	Write preamble	Min	1.8	tCK(avg)
Temperature Derating Parameters				
tDQSCKd	DQS output access time from CK_t/CK_c (derated)	Max	3600	ps
tRCDd	RAS-to-CAS delay (derated)	Min	tRCD + 1.875	ns
tRCd	ACTIVATE-to-ACTIVATE command period (same bank, derated)	Min	tRC + 3.75	ns
tRASd	Row active time (derated)	Min	tRAS + 1.875	ns
tRPd	Row precharge time (derated)	Min	tRP + 1.875	ns
tRRD	Active bank A to active bank B (derated)	Min	tRRD + 1.875	ns

Simplified State Diagram



Command Truth Table

Command	CS	CA0	CA1	CA2	CA3	CA4	CA5
MRW-1	H	L	H	H	L	L	OP7
	L	MA0	MA1	MA2	MA3	MA4	MA5
MRW-2	H	L	H	H	L	H	OP6
	L	OP0	OP1	OP2	OP3	OP4	OP5
MRR-1	H	L	H	H	H	L	V
	L	MA0	MA1	MA2	MA3	MA4	MA5
REFRESH (all/per bank)	H	L	L	L	H	L	AB
	L	BA0	BA1	BA2	V	V	V
ENTER SELF REFRESH	H	L	L	L	H	H	V
	L	V					
ACTIVATE-1	H	H	L	R12	R13	R14	R15
	L	BA0	BA1	BA2	V	R10	R11
ACTIVATE-2	H	H	H	R6	R7	R8	R9
	L	R0	R1	R2	R3	R4	R5
WRITE-1	H	L	L	H	L	L	BL
	L	BA0	BA1	BA2	V	C9	AP
EXIT SELF REFRESH	H	L	L	H	L	H	V
	L	V					
MASK WRITE-1	H	L	L	H	H	L	BL
	L	BA0	BA1	BA2	V	C9	AP
RFU	H	L	L	H	H	H	V
	L	V					
RFU	H	L	H	L	H	L	V
	L	V					
RFU	H	L	H	L	H	H	V
	L	V					
READ-1	H	L	H	L	L	L	BL
	L	BA0	BA1	BA2	V	C9	AP
CAS-2 (WRITE-2,MASKED WRITE-2,READ-2, MRR-2,MPC (except NOP)	H	L	H	L	L	H	C8
	L	C2	C3	C4	C5	C6	C7
PRECHARGE (all/per bank)	H	L	L	L	L	H	AB
	L	BA0	BA1	BA2	V	V	V
MPC (TRAIN, NOP)	H	L	L	L	L	L	OP6
	L	OP0	OP1	OP2	OP3	OP4	OP5
DESELECT	L	X					

Note 1: All commands except for DESELECT are two clock cycles and are defined by the current state of CS and CA[5:0] at the rising edge of the clock. DESELECT command is one clock cycle and is not latched by the device.

Note 2: V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, and CA[5:0] can be floated.

Note 3: Bank addresses BA[2:0] determine which bank is to be operated upon.

Note 4: AB HIGH during PRECHARGE or REFRESH commands indicate the command must be applied to all

banks, and the bank addresses are "Don't Care."

Note 5: MASK WRITE-1 command only supports BL16. For MASK WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).

Note 6: AP HIGH during a WRITE-1, MASK WRITE-1, or READ-1 command indicates that an auto precharge will occur to the bank the command is operating on. AP LOW indicates that no auto precharge will occur and the bank will remain open upon completion of the command.

Note 7: When enabled in the mode register, BL HIGH during a WRITE-1, MASK-WRITE-1, or READ-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOW during one of these commands indicates the burst length should be set on-the-fly to BL = 16. If on-the-fly burst length is not enabled in the mode register, this bit should be driven to a valid level and is ignored by the device.

Note 8: For CAS-2 commands (WRITE-2, MASK WRITE-2, READ-2, MRR-2, or MPC (only write FIFO, read FIFO and read DQ calibration), C[1:0] are not transmitted on the CA [5:0] bus and are assumed to be zero. Note that for CAS-2 WRITE-2 or CAS-2 MASK WRITE-2 command,C[3:2] must be driven LOW.

Note 9: WRITE-1, MASK-WRITE-1, READ-1, MODE REGISTER READ-1, or MPC (only write FIFO,read FIFO, and read DQ calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. WRITE-1, MASK WRITE-1, READ-1, MRR-1, or MPC (only write FIFO, read FIFO, and read DQ calibration) command must be issued first before issuing CAS-2 command. MPC (only Start and Stop DQS Oscillator, Start and Latch ZQ Calibration) commands do not require CAS-2 command;they require two additional DES or NOP commands consecutively before issuing any other commands.

Note 10: The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutively without any other command between them. The ACTIVATE-1 command must be issued prior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.

Note 11: The MRW-1 command must be followed by the MRW-2 command consecutively without any other command between them. The MRW-1 command must be issued prior to the MRW-2 command.

Note 12: The MRR-1 command must be followed by the CAS-2 command consecutively without any other commands between them. The MRR-1 command must be issued prior to the CAS-2 command.

Note 13: The MPC command for READ or WRITE training operations must be followed by the CAS-2 command consecutively without any other commands between them. The MPC command must be issued prior to the CAS-2 command.

IDD Measurement Conditions

Switching for CA Input Signals

CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	H	H	H	H	H	H	H	H
CS	L	L	L	L	L	L	L	L
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H

Notes 1: LOW = VIN ≤ VIL(DC) MAX, HIGH = VIN ≥ VIH(DC) MIN, STABLE = Inputs are stable at a HIGH or LOW level

Notes 2: CS must always be driven LOW.

Notes 3: 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

Notes 4: The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

CA Pattern for IDD4R

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes 1: BA[2:0] = 010; CA[9:4] = 000000 OR 111111; Burst order CA[3:2] = 00 or 11.

Notes 2: CA pins are kept LOW with DES CMD to reduce ODT current.

CA Pattern for IDD4W

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes 1: BA[2:0] = 010; CA[9:4] = 000000 or 111111
Notes 2: No burst ordering
Notes 3: CA pins are kept LOW with DES CMD to reduce ODT current

Data Pattern for IDD4W(DBI off)

DBI Off Case										
	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4

BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	0	2
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	0	0	0	6
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	0	0	0	6
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	0	2
BL31	0	0	0	0	1	1	1	1	0	4
# of 1s	16	16	16	16	16	16	16	16		

Notes 1: Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming.

Data Pattern for IDD4R(DBI off)

DBI Off Case										
	DQ7	**DQ6**	**DQ5**	**DQ4**	**DQ3**	**DQ2**	**DQ1**	**DQ0**	**DBI**	**# of 1s**
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	0	2
BL21	0	0	0	0	1	1	1	1	0	4

BL22	1	1	1	1	1	1	0	0	0	6
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	0	0	0	6
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	0	2
BL31	0	0	0	0	1	1	1	1	0	4
# of 1s	16	16	16	16	16	16	16	16		

Notes 1: Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming.

Power-up, initialization

To ensure proper functionality for power-up and reset initialization, default values for the MR settings are provided in the table below.

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set A is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, *n*RTP = 8
*n*WR	MR1 OP[6:4]	000b	*n*WR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
$V_{REF(CA)}$ setting	MR12 OP[6]	1b	$V_{REF(CA)}$ range[1] is enabled
$V_{REF(CA)}$ value	MR12 OP[5:0]	001101b	Range1: 27.2% of V_{DD2}
$V_{REF(DQ)}$ setting	MR14 OP[6]	1b	$V_{REF(DQ)}$ range[1] enabled
$V_{REF(DQ)}$ value	MR14 OP[5:0]	001101b	Range1: 27.2% of V_{DDQ}

The following sequence must be used to power up the device. Unless specified otherwise,this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

Voltage Ramp

1.While applying power (after Ta), RESET_n should be held LOW (≤0.2 × VDD2), and all other inputs must be between VIL,min and VIH,max. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the table below. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

Notes 1: Ta is the point when any power supply first reaches 300mV.

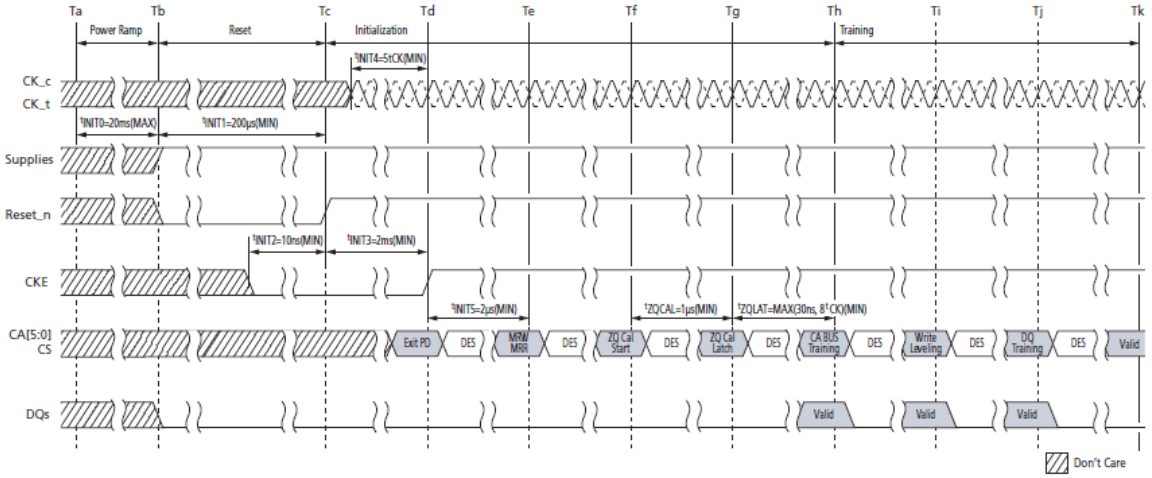
Notes 2: Noted conditions apply between Ta and power-down (controlled or uncontrolled).

Notes 3: Tb is the point at which all supply and reference voltages are within their defined operating ranges.

Notes 4: Power ramp duration tINIT0 (Tb–Ta) must not exceed 20ms.

Notes 5: The voltage difference between any VSS and VSSQ must not exceed 100mV

2. Following completion of the of the voltage ramp (Tb), RESET_n must be held LOW for tINIT1. DQ, DMI, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.
3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care."



Mode Registers

Mode Register Assignment and Definition

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	CATR	RFU	RFU	RZQI		RFU		REF	Go to MR0
1	01h	Device feature 1	W	RD-PST	*n*WR (for AP)			RD-PRE	WR-PRE	BL		Go to MR1
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL			Go to MR2
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL	Go to MR3
4	04h	Refresh and training	R /W	TUF	Thermal offset		PPRE	SR Abort	Refresh rate			Go to MR4
5	05h	Basic config-1	R	LPDDR4 Manufacturer ID								Go to MR5
6	06h	Basic config-2	R	Revision ID1								Go to MR6
7	07h	Basic config-3	R	Revision ID2								Go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		Go to MR8
9	09h	Test mode	W	Vendor-specific test mode								Go to MR9
10	0Ah	I/O calibration	W	RFU							ZQ RST	Go to MR10
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT			Go to MR11
12	0Ch	$V_{REF(CA)}$	R/W	RFU	VR_{CA}	$V_{REF(CA)}$						Go to MR12
13	0Dh	Register control	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT	Go to MR13
14	0Eh	$V_{REF(DQ)}$	R/W	RFU	VR_{DQ}	$V_{REF(DQ)}$						Go to MR14
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration								Go to MR15
16	10h	PASR_Bank	W	PASR bank mask								Go to MR16
17	11h	PASR_Seg	W	PASR segment mask								Go to MR17
18	12h	IT-LSB	R	DQS oscillator count – LSB								Go to MR18
19	13h	IT-MSB	R	DQS oscillator count – MSB								Go to MR19
20	14h	DQI-UB	W	Upper-byte invert register for DQ calibration								Go to MR20
21	15h	Vendor use	W	RFU								Go to MR21

Mode Register Assignments(continued)

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
22	16h	ODT feature 2	W	RFU		ODTD-CA	ODTE-CS	ODTE-CK	SoC ODT			Go to MR22
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting								Go to MR23
24	18h	TRR control	R/W	TRR Mode	TRR bank address			Unltd MAC	MAC value			Go to MR24
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0	Go to MR25
26–31	1Ah~1Fh	–	–	Reserved for future use								
32	20h	DQ calibration pattern A	W	See DQ Calibration section								Go to MR32
33–39	21h≈27h	Do not use	–	Do not use								
40	28h	DQ calibration pattern B	W	See DQ Calibration section								Go to MR40
41–47	29h≈2Fh	Do not use	–	Do not use								
48–63	30h≈3Fh	Reserved	–	Reserved for future use								

Notes 1: RFU bits must be set to 0 during MRW commands.

Notes 2: RFU bits are read as 0 during MRR commands.

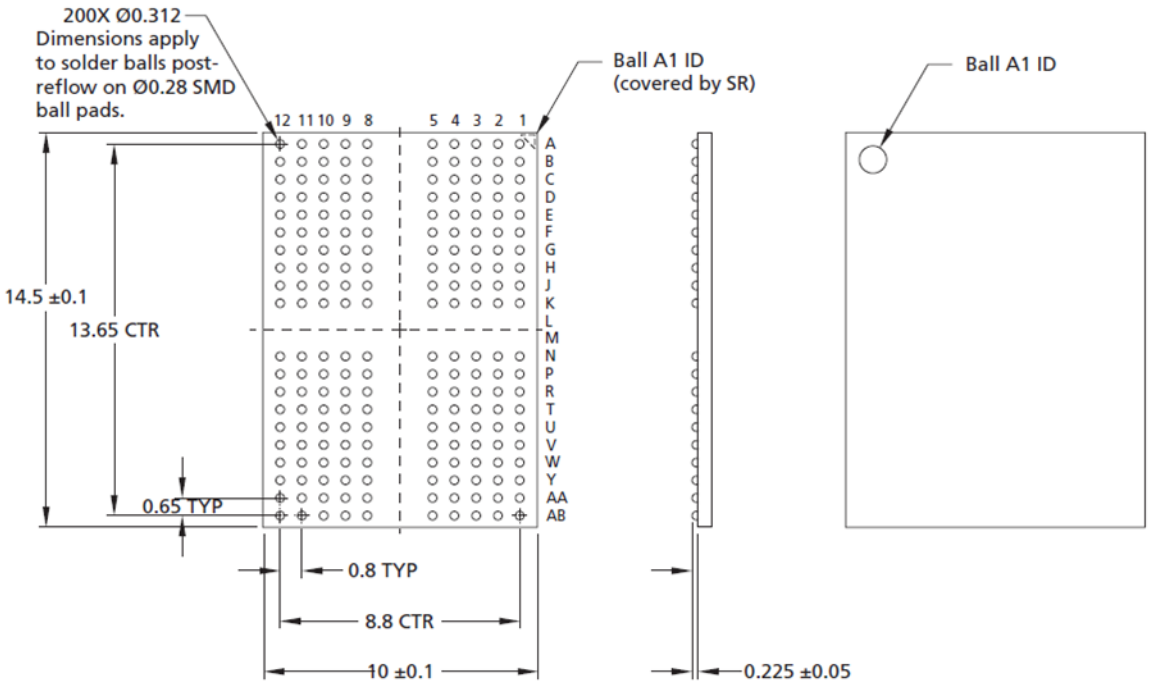
Notes 3: All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.

Notes 4: RFU mode registers must not be written.

Notes 5: Writes to read-only registers will not affect the functionality of the device.

Package Description

200-ball FBGA 10x14.5mm



Notes:
1. All dimensions are in millimeters.
2. The package height does not include room temperature warpage.

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Feb. 2018	Maven Hsu	N/A
1.0	First SPEC. release.	Feb. 2018	Maven Hsu	N/A