4Gb (32Mx8Banksx16) DDR3 SDRAM

Descriptions

The H2A404G1666N is a high speed Double Date Rate 3 (DDR3) Synchronous DRAM fabricated with ultra high performance CMOS process containing 4G bits which organized as 32Mbits x 8 banks by 16 bits.
This synchronous device achieves high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin (DDR3-1866) for general applications.
The chip is designed to comply with the following key DDR3 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) On Die Termination (4) programmable driver strength data,(5) seamless BL4 access. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks
(CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional differential data strobes
(DQS and /DQS) in a source synchronous fashion.
The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style.

Features

- JEDEC Standard VDD/VDDQ = +1.5V ± 0.075V
- Operating temperature:
  - Normal operating temperature: TC = 0~85°C
  - Extended temperature: TC = 85~95°C
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 800/933MHz
- Differential Clock, CK & CK#
- Bidirectional differential data strobe –DQS & DQS#.
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- Write Leveling
- ZQ Calibration
- RoHS compliant
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- Average Refresh Period
  7.8us @ 0˚C ≦TC≦ +85˚C
  3.9us at 85˚C < Tcase ≦ 95°C
- 96-ball 7.5 x 13.5 x 1.2mm FBGA package
  - Pb and Halogen Free

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A404G1666NFYC	256M X 16	DDR3-1600Mhz (11-11-11)	96Ball BGA, 7.5x13.5mm	Commercial
H2A404G1666NGYC	256M X 16	DDR3-1866Mhz (13-13-13)	96Ball BGA, 7.5x13.5mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDDQ	DQ13	DQ15	A	DQ12	VDDQ	VSS
VSSQ	VDD	VSS	B	/UDQS	DQ14	VSSQ
VDDQ	DQ11	DQ9	C	UDQS	DQ10	VDDQ
VSSQ	VDDQ	UDM	D	DQ8	VSSQ	VDD
VSS	VSSQ	DQ0	E	LDM	VSSQ	VDDQ
VDDQ	DQ2	LDQS	F	DQ1	DQ3	VSSQ
VSSQ	DQ6	/LDQS	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	H	DQ7	DQ5	VDDQ
NC	VSS	/RAS	J	CK	VSS	NC
ODT	VDD	/CAS	K	/CK	VDD	CKE
NC	/CS	/WE	L	A10/AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12 , /BC	BA1	VDD
VSS	A5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	/RESET	A13	T	A14	A8	VSS

96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
J7,K7	CK,/CK	**(System Clock)** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK . Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
L2	/CS	**(Chip Select)** All commands are masked when CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
K9	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self- refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including self-refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self -refresh.
N3,P7,P3,N2, P8,P2,R8,R2, T8,R3,L7,R7, N7	A0~A9,A10(AP), A11,A12(/BC),	**(Address)** Provided the row address (RA0 – RA12) for active commands and the column address (CA0-CA9) and auto precharge bit for read/write commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). The address inputs also provide the op-code during Mode Register Set commands. A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
M2,N8,M3	BA0,BA1,BA2	**(Bank Address)** BA0 – BA2 define to which bank an active, read, write or precharge command is being applied. Bank address also determines if the mode register is to be accessed during a MRS cycle.
K1	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enable ODT is applied to each DQ,DQS, DQS DMU and DML signal. The ODT pin will be ignored if the Mo Register MR1 is programmed to disable ODT.

C7,B7,F3,G3	DQSU, /DQSU, DQSL, /DQSL	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQSL, and DQSU are paired with differential signals /DQSU and /DQSL respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
J3,K3,L3	/RAS,	**(Command Inputs)** /RAS , /CAS & /WE (along with /CS) define the command being entered.
D3,E7	DMU,DML	**(Input Data Mask)** DMU & DML are input mask signal for write data. Input data is masked when DMU or DML are sampled HIGH coincident with that input data during a write access. DMU & DML is sampled on both edges of DQSU & DQML respectively.
D7,C3,C8,C2, A7,A2,B8,A3	DQU0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
E3,F7,F2,F8, H3,H8,G2,H7	DQL0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
B2,D9,G7,K2,K9,N1, N9,R1,R9/A9,B3,E1, G8,J2,J8,M1,M9,P1, P9,T1,T9	VDD,VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
A1,A8,C1,C9,D2, E9,F1,H2,H9 /B1, B9,D1,D8,E2,E8, F9,G1,G9	VDDQ, VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
L8	ZQ	**(ZQ Calibration)** Reference pin for ZQ calibration

T2	/RESET	**(Active Low Asynchronous Reset)** Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
H1	VREFDQ	**(Reference Voltage)** Reference voltage for DQ
M8	VREFCA	**(Reference Voltage)** Reference voltage for CA
J1,J9,L1,L9, M7,T3,T7	NC	**(No Connection)** No internal electrical connection is present.

Note: Input pins only BA0-BA2, A0-A12, /RAS , /CAS , /WE , /CS , CKE, ODT and /RESET do not supply termination.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.4 ~ +1.8		V
V_{DD}	Power Supply Voltage	-0.4 ~ +1.8		V
V_{DDQ}	Power Supply Voltage	-0.4 ~ +1.8		V
T_{OP}	Operating Temperature Range	Comercial	0 ~ +85	°C
T_{STG}	Storage Temperature Range	-55 ~ +100		°C

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Power Supply for I/O Voltage	1.425	1.5	1.575	V

Input / Output Capacitance

Symbol	Parameters	Min.	Max.	Unit
CIO	Input/output capacitance, (DQ, DM, DQS, DQS#)	1.4	2.3	pF
CCK	Input capacitance, CK and CK#	0.8	1.4	pF
CDCK	Input capacitance delta, CK and CK#	0	0.15	pF
CDDQS	Input/output capacitance delta, DQS and DQS#	0	0.15	pF
CI	Input capacitance, (CTRL, ADD, CMD input-only pins)	0.75	1.3	pF
CDI_CTRL	Input capacitance delta, (All CTRL input-only pins)	-0.4	0.2	pF
CDI_ADD_CMD	Input capacitance delta, (All ADD, CMD input-only pins)	-0.4	0.4	pF
CDIO	Input/output capacitance delta, (DQ, DM, DQS, DQS#)	-0.5	0.3	pF
CZQ	Input/output capacitance of ZQ pin	-	3	pF

Recommended DC Operating Conditions

Symbol	Parameter & Test Conditions	1866	1600	Units
		Max		
IDD0	Operating One Bank Active-Precharge Current CKE: High; External clock: On; BL: 8*1; AL: 0; CS#: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...;Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	59	57	mA
IDD1	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; BL: 8*1, 5; AL:0; CS#: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	84	81	mA
IDD2P0	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; BL: 8*1; AL: 0; CS#: stable at 1; Command, Address, Ban Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all bank closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0; Pecharge Power Down Mode: Slow Exit.*3	8	8	mA
IDD2N	Precharge Standby Current CKE: High; External clock: On; BL: 8*1; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	26	24	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; BL: 8*1; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	26	24	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; BL: 8*1; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0	28	26	mA
IDD3N	Active Standby Current CKE: High; External clock: On; BL: 8*1; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	40	38	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; BL: 8*1, 5; AL: 0; CS#: High between RD; Command, Address, Bank Address Inputs: partially toggling; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; tput Buffer and RTT: Enable in Mode Registers*2; ODT Signal: stable at 0.	165	155	mA

IDD4W	Operating Burst Write Current CKE: High; External clock: On; BL: 8*1; AL: 0; CS#: High between WR; Command, Address, Bank Address Inputs: partially toggling; DM: stable at 0; Bank Activity: all bank open. Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at HIGH	165	155	mA

IDD5B	Burst Refresh Current CKE: High; External clock: On; BL: 8*1; AL: 0; CS#: High between tREF; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: REF command every tRFC; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	242	235	mA
IDD6	Self Refresh Current: Self-Refresh Temperature Range (SRT): Normal*4; CKE: Low; External clock: Off; CK and CK#: LOW; BL: 8*1; AL: 0; CS#, Command, Address, Bank Address, Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: MID-LEVEL	12	12	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; BL: 8*1, 5; AL: CL-1; CS#: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; DM:stable at 0; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	200	190	mA
IDD8	RESET Low Current RESET: LOW; External clock: Off; CK and CK#: LOW; CKE: FLOATING; CS#, Command, Address, Bank Address, Data IO: FLOATING; ODT Signal: FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW fo at least 1ms.	IDD2P +2mA	IDD2P +2mA	mA

Note 1: Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B.

Note 2: Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B;RTT_Wr enable: set MR2 A[10,9] = 10B.

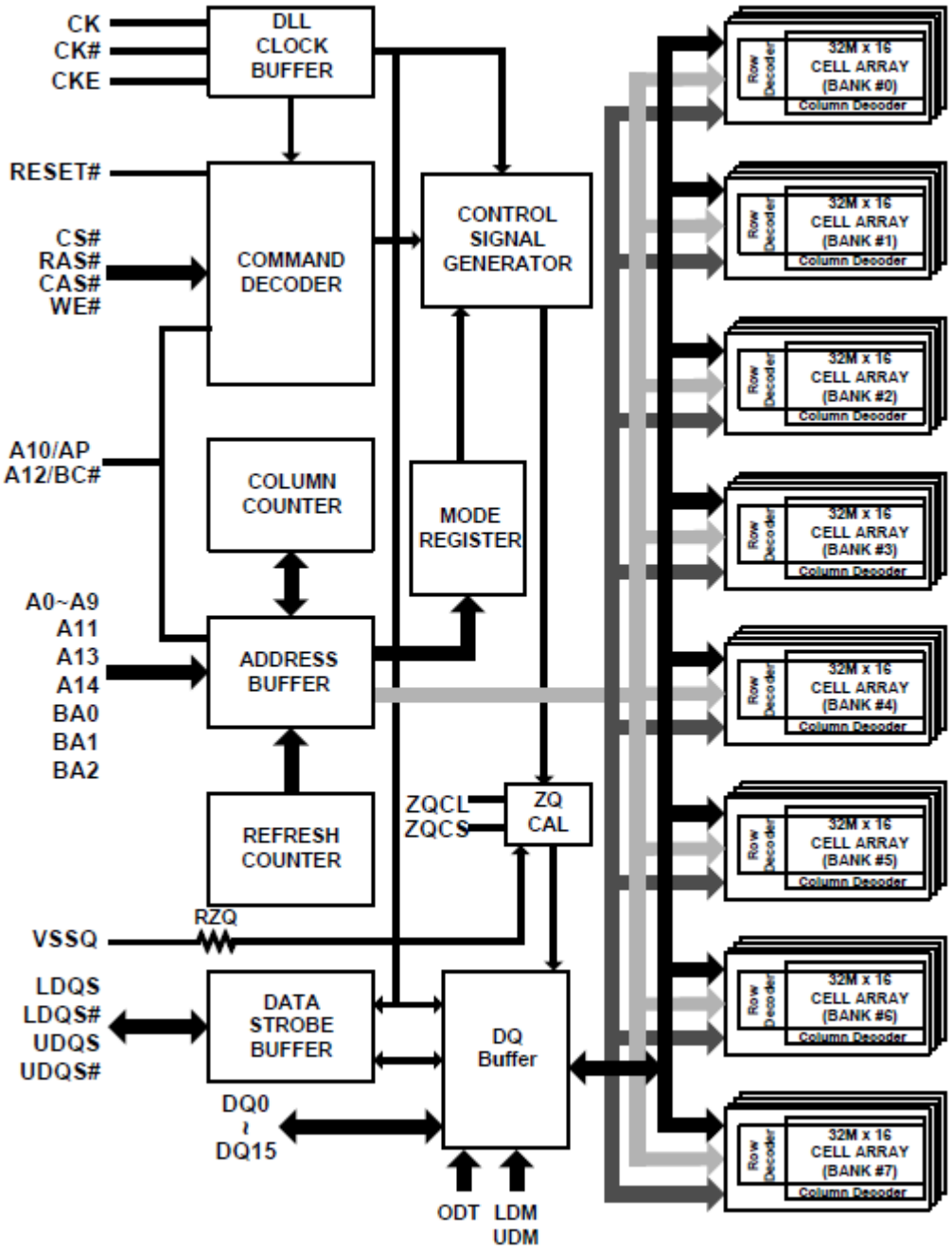
Note 3: Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit.

Note 4: Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range.

Note 5: Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B.

Note 6: Supporting 0 - 85 °C with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options. However, for applications operating in Extended Temperature 85°C ~ 95°C, some optional spec are required.

Block Diagram



AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Parameter		1866		1600		Units	Notes
			Min.	Max.	Min.	Max.		
tAA	Internal read command to first data		13.91	20	13.75	20	ns	
tRCD	ACT to internal read or write delay time		13.91	-	13.75	-	ns	
tRP	PRE command period		13.91	-	13.75	-	ns	
tRC	ACT to ACT or REF command period		47.91	-	48.75	-	ns	
tRAS	ACTIVE to PRECHARGE command period		34	9 x tREFI	35	9 x tREFI	ns	
tCK(avg)	Average clock period	CL=5, CWL=5	3.0	3.3	3.0	3.3	ns	33
		CL=6, CWL=5	2.5	3.3	2.5	3.3	ns	33
		CL=7, CWL=6	1.875	<2.5	1.875	<2.5	ns	33
		CL=8, CWL=6	1.875	<2.5	1.875	<2.5	ns	33
		CL=9, CWL=7	1.5	<1.875	1.5	<1.875	ns	33
		CL=10, CWL=7	1.5	<1.875	1.5	<1.875	ns	33
		CL=11, CWL=8	1.25	<1.5	1.25	<1.5	ns	33
		CL=12, CWL=8	1.25	<1.5	-	-	ns	33
		CL=13, CWL=9	1.07	<1.25	-	-	ns	33
tCK (DLL_OFF)	Minimum Clock Cycle Time (DLL off mode)		8	-	8	-	ns	6
tCH(avg)	Average clock HIGH pulse width		0.47	0.53	0.47	0.53	tck	
tCL(avg)	Average Clock LOW pulse width		0.47	0.53	0.47	0.53	tck	
tDQSQ	DQS, DQS# to DQ skew, per group, per access		-	85	-	100	ps	13
tQH	DQ output hold time from DQS, DQS#		0.38	-	0.38	-	tck	13
tLZ(DQ)	DQ low-impedance time from CK, CK#		-390	195	-450	225	ps	13,14
tHZ(DQ)	DQ high impedance time from CK, CK#		-	195	-	225	ps	13,14
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels		-	-	10	-	ps	17
tDS(base) AC135	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels		68	-	-	-	ps	17
tDH(base) DC100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels		70	-	45	-	ps	17
tDIPW	DQ and DM Input pulse width for each input		320	-	360	-	ps	

tRPRE	DQS,DQS# differential READ Preamble	0.9	-	0.9	-	tck	13,19
tRPST	DQS, DQS# differential READ Postamble	0.3	-	0.3	-	tck	11,13
tQSH	DQS, DQS# differential output high time	0.4	-	0.4	-	tck	13
tQSL	DQS, DQS# differential output low time	0.4	-	0.4	-	tck	13
tWPRE	DQS, DQS# differential WRITE Preamble	0.9	-	0.9	-	tck	1
tWPST	DQS, DQS# differential WRITE Postamble	0.3	-	0.3	-	tck	1
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-195	195	-225	225	ps	13
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-390	195	-450	225	ps	13,14
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	195	-	225	ps	13,14
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	0.45	0.55	tck	29.31
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	0.45	0.55	tck	30,31
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	-0.27	0.27	tck	
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	0.18	-	tck	32
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	0.18	-	tck	32
tDLLK	DLL locking time	512	-	512	-	tck	
tRTP	Internal READ Command to PRECHARGE Command delay	max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tck	
tWTR	Delay from start of internal write transaction to internal read command	max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tck	18
tWR	WRITE recovery time	15	-	15	-	ns	18
tMRD	Mode Register Set command cycle time	4	-	4	-	tck	
tMOD	Mode Register Set command update delay	max (12tCK, 15ns)	-	max (12tCK, 15ns)	-	tck	
tCCD	CAS# to CAS# command delay	4	-	4	-	tck	
tDAL(min)	Auto precharge write recovery + prechargetime	WR + tRP		WR + tRP		tck	
tMPRR	Multi-Purpose Register Recovery Time	1	-	1	-	tck	22

tRRD	ACTIVE to ACTIVE command period	max (4tCK, 6ns)	-	max (4tCK, 7.5ns)	-	tck	
tFAW	Four activate window	35	-	40	-	ns	
tIS(base) AC175	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	-	-	45	-	ps	16
tIS(base) AC150		-	-	170	-	ps	16,27
tIS(base) AC135		65	-	-	-	ps	
tIS(base) AC125		150	-	-	-	ps	
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	100	-	120	-	ps	16
tIPW	Control and Address Input pulse width for each input	535	-	560	-	ps	28
tZQinit	Power-up and RESET calibration time	512	-	512	-	tck	
tZQoper	Normal operation Full calibration time	256	-	256	-	tck	
tZQCS	Normal operation Short calibration time	64	-	64	-	tck	23
tXPR	Exit Reset from CKE HIGH to a valid command	max (5tCK, tRFC(min) + 10ns)	-	max (5tCK, tRFC(min) + 10ns)	-	tck	
tXS	Exit Self Refresh to commands not requiring a locked DLL	max (5tCK, tRFC(min) + 10ns)	-	max (5tCK, tRFC(min) + 10ns)	-	tck	
tXSDLL	Exit Self Refresh to commands requiring a locked DLL	tDLLK(min)	-	tDLLK(min)	-	tck	
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tck	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	max (5tCK, 10 ns)	-	max (5tCK, 10 ns)	-	tck	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	max (5tCK, 10 ns)	-	max (5tCK, 10 ns)	-	tck	
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max (3tCK, 6 ns)	-	max (3tCK, 6 ns)	-	tck	

tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a lockedDLL	max (10tCK, 24 ns)	-	max (10tCK, 24 ns)	-	tck	2
tCKE	CKE minimum pulse width	max (3tCK, 5 ns)	-	max (3tCK, 5 ns)	-	tck	
tCPDED	Command pass disable delay	2	-	1	-	tck	
tPD	Power Down Entry to Exit Timing	tCKE (min)	9 x tREFI	tCKE (min)	9 x tREFI		15
tACTPDEN	Timing of ACT command to Power Down entry	1	-	1	-	tck	20
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	1	-	tck	20
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	RL+4+1	-	tck	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL+4+ (tWR/tCK)	-	WL+4+ (tWR/tCK)	-	tck	9
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS,BC4OTF)	WL+4+WR +1	-	WL+4+W R+1	-	tck	10
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL+2+ (tWR/tCK)	-	WL+2+ (tWR/tCK)	-	tck	9
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL+2+WR +1	-	WL+2+W R+1	-	tck	10
tREFPDEN	Timing of REF command to Power Down entry	1	-	1	-	tck	20,21
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	tMOD(min)	-		
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2		WL - 2 = CWL + AL - 2		tck	
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2		WL - 2 = CWL + AL - 2		tck	
ODTH4	ODT high time without write command or with write command and BC4	4	-	4	-	tck	
ODTH8	ODT high time with Write command and BL8	6	-	6	-	tck	
tAONPD	Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	2	8.5	2	8.5	ns	
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	2	8.5	ns	

tAON	RTT turn-on	-195	195	-225	225	ps	7
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tck	8
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	tck	
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	40	-	tck	3
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	25	-	tck	3
tWLS	Write leveling setup time from rising CK,CK# crossing to rising DQS, DQS# crossing	140	-	165	-	ps	
tWLH	Write leveling hold time from rising DQS,DQS# crossing to rising CK, CK# crossing	140	-	165	-	ps	
tWLO	Write leveling output delay	0	7.5	0	7.5	ns	
tWLOE	Write leveling output error	0	2	0	2	ns	
tRFC	REF command to ACT or REF command time	260	-	260	-	ns	
tREFI	Average periodic refresh interval 0°C to 85°C	-	7.8	-	7.8	us	
tREFI	Average periodic refresh interval 85°C to 95°C	-	3.9	-	3.9	us	

Note 1. Actual value dependant upon measurement level.

Note 2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

Note 3. The max values are system dependent.

Note 4. WR as programmed in mode register.

Note 5. Value must be rounded-up to next higher integer value.

Note 6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

Note 7. For definition of RTT turn-on time tAON See “Timing Parameters”.

Note 8. For definition of RTT turn-off time tAOF See “Timing Parameters”.

Note 9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

Note 10. WR in clock cycles as programmed in MR0.

Note 11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship”.

Note 12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.

Note 13. Value is only valid for RON34.

Note 14. Single ended signal parameter.

Note 15. tREFI depends on TOPER.

Note 16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC)

= VRefCA(DC). See “Address / Command Setup, Hold and Derating”.

Note 17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See “Data Setup, Hold and Slew Rate Derating”.

Note 18. Start of internal write transaction is defined as follows:

- For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.

- For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.

- For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

Note 19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See “Clock to Data Strobe Relationship”.

Note 20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

Note 21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See “Power-Down clarifications-Case 2”.

Note 22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

Note 23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage

(Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

ZQCorrection/(TSens × Tdriftrate) + (VSens × Vdriftrate)

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

0.5/(1.5 × 1) + (0.15 × 15) = 0.133(~128ms)

Note 24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

Note 25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

Note 26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Note 27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

Note 28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).

Note 29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.

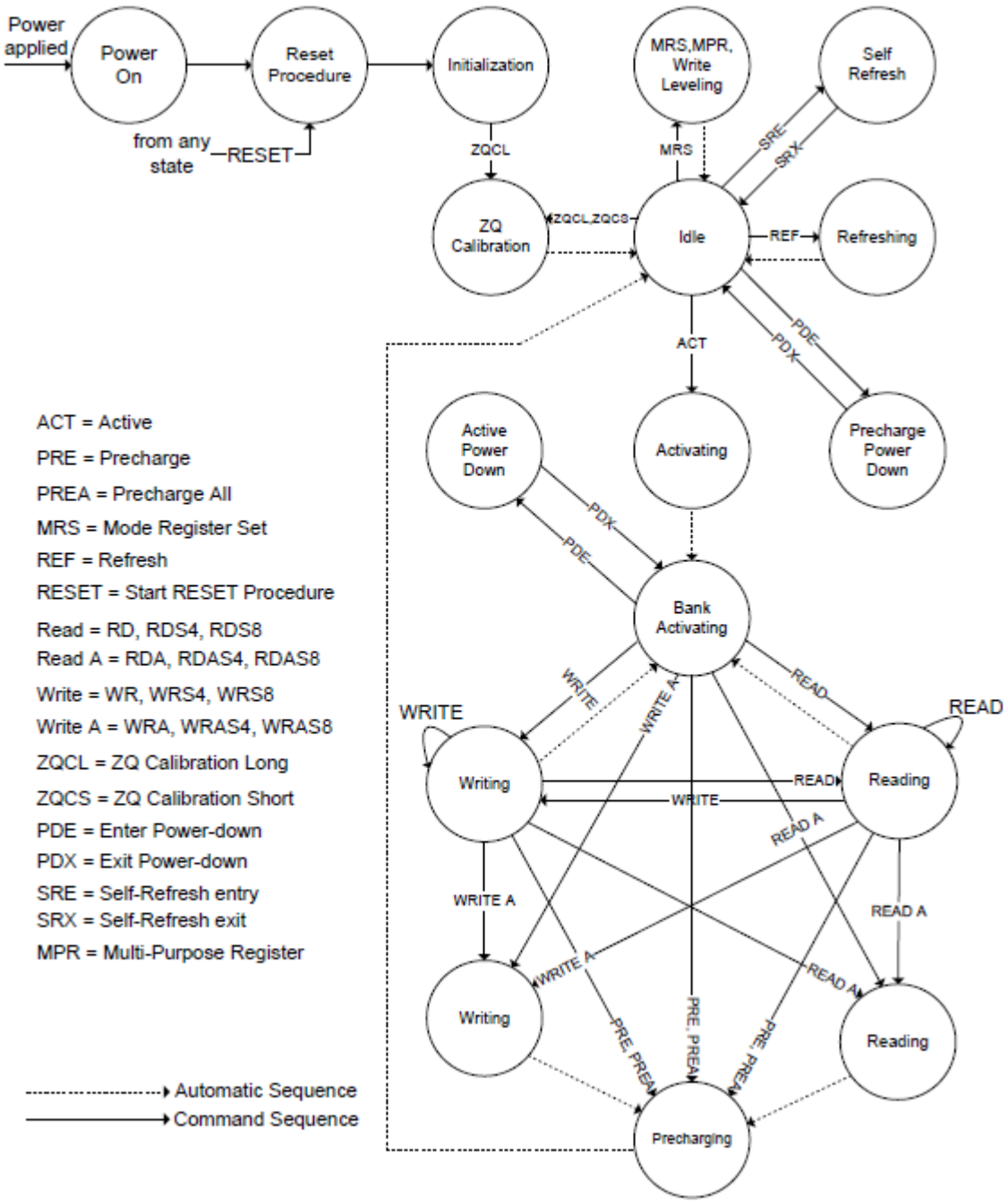
Note 30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.

Note 31. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

Note 32. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

Note 33. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.

Simplified State Diagram



Command Truth Table(Note(1),(2))

Command	State	CKEn-1[3]	CKEn	DM	BA0-2	A10/AP	A0-9, 11, 13-14	A12/BC#	CS#	RAS#	CAS#	WE#
BankActivate	Idle[4]	H	H	X	V	Row address			L	L	H	H
Single Bank Precharge	Any	H	H	X	V	L	V	V	L	L	H	L
All Banks Precharge	Any	H	H	X	V	H	V	V	L	L	H	L
Write (Fixed BL8 or BC4)	Active[4]	H	H	X	V	L	V	V	L	H	L	L
Write (BC4, on the fly)	Active[4]	H	H	X	V	L	V	L	L	H	L	L
Write (BL8, on the fly)	Active[4]	H	H	X	V	L	V	H	L	H	L	L
Write with Autoprecharge (Fixed BL8 or BC4)	Active[4]	H	H	X	V	H	V	V	L	H	L	L
Write with Autoprecharge (BC4, on the fly)	Active[4]	H	H	X	V	H	V	L	L	H	L	L
Write with Autoprecharge (BL8, on the fly)	Active[4]	H	H	X	V	H	V	H	L	H	L	L
Read (Fixed BL8 or BC4)	Active[4]	H	H	X	V	L	V	V	L	H	L	H
Read (BC4, on the fly)	Active[4]	H	H	X	V	L	V	L	L	H	L	H
Read (BL8, on the fly)	Active[4]	H	H	X	V	L	V	H	L	H	L	H
Read with Autoprecharge (Fixed BL8 or BC4)	Active[4]	H	H	X	V	H	V	V	L	H	L	H
Read with Autoprecharge (BC4, on the fly)	Active[4]	H	H	X	V	H	V	L	L	H	L	H
Read with Autoprecharge (BL8, on the fly)	Active[4]	H	H	X	V	H	V	H	L	H	L	H
(Extended) Mode Register Set	Idle	H	H	X	V	OP code			L	L	L	L
No-Operation	Any	H	H	X	V	V	V	V	L	H	H	H
Device Deselect	Any	H	H	X	X	X	X	X	H	X	X	X
Refresh	Idle	H	H	X	V	V	V	V	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	V	V	V	V	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Entry	Idle	H	L	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Exit	Any	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Input Mask Enable[5]	Active	H	X	H	X	X	X	X	X	X	X	X
ZQ Calibration Long	Idle	H	H	X	X	H	X	X	L	H	H	L
ZQ Calibration Short	Idle	H	H	X	X	L	X	X	L	H	H	L

Note1: V=Valid data, X=Don't Care, L=Low level, H=High level

Note2: CKEn signal is input level when commands are provided.

CKEn-1 signal is input level one clock cycle before the commands are provided.

Note3: These are states of bank designated by BA signal.

Note4: LDM and UDM can be enabled respectively.

Power up and Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). /RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled “Low” anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
- Vref tracks VDDQ/2. OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also,a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted.Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=max (tXS ; 5 x tCK)

6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)

7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)

8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and BA2).

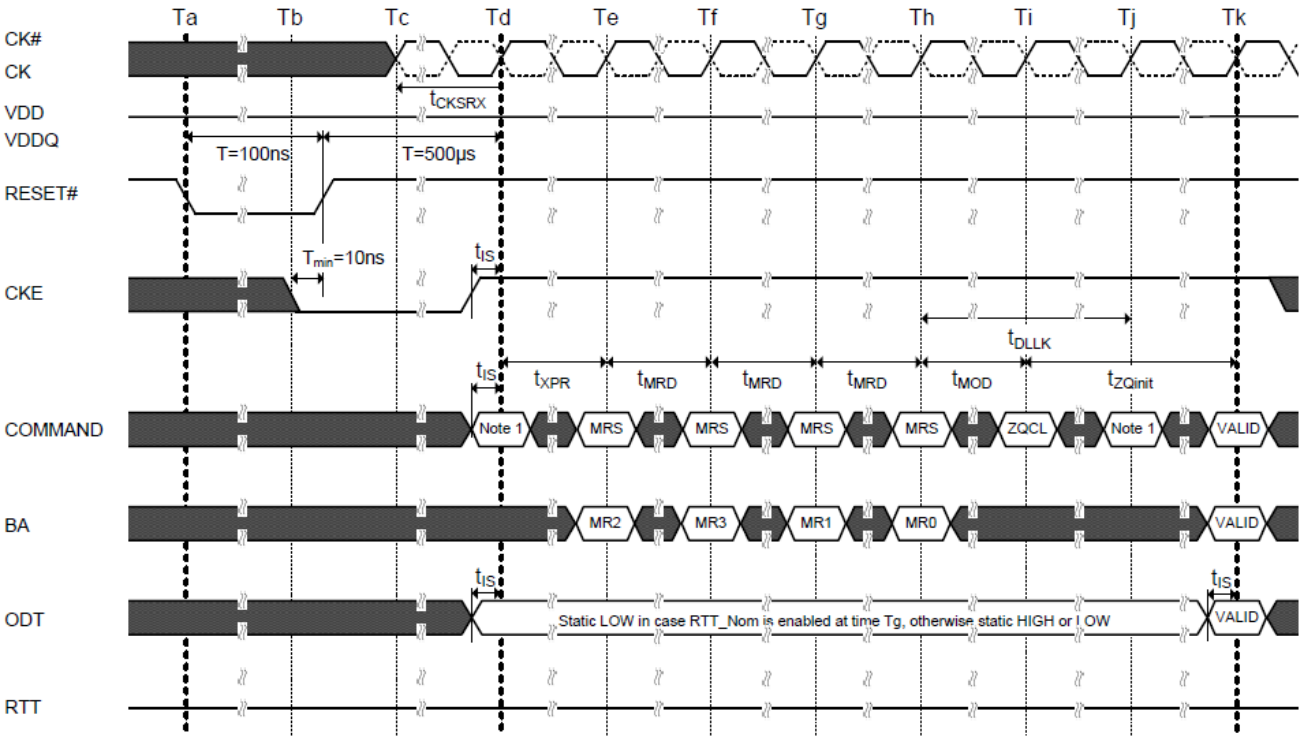
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-BA2).

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.

12. The DDR3 SDRAM is now ready for normal operation.

Reset and Power up initialization sequence



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK Don't Care

Mode Register Definition

Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 DRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

BA2	BA1	BA0	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0[*1]	0	0	0[*1]	0[*1]	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL		Mode Register (0)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A11	A10	A9	WR (cycles)
0	0	0	16[*2]
0	0	1	5[*2]
0	1	0	6[*2]
0	1	1	7[*2]
1	0	0	8[*2]
1	0	1	10[*2]
1	1	0	12[*2]
1	1	1	14[*2]

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	Reserved
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

A8	DLL Reset
0	No
1	Yes

Note1: Reserved for future use and must be set to 0 when programming the MR

Note2: WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer WRmin [cycles] =Roundup (tWR / tCK). The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Burst Type and Burst Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

CAS Latency

The CAS Latency is defined by MR0 (bit A2, A4~A6) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

Write Recovery

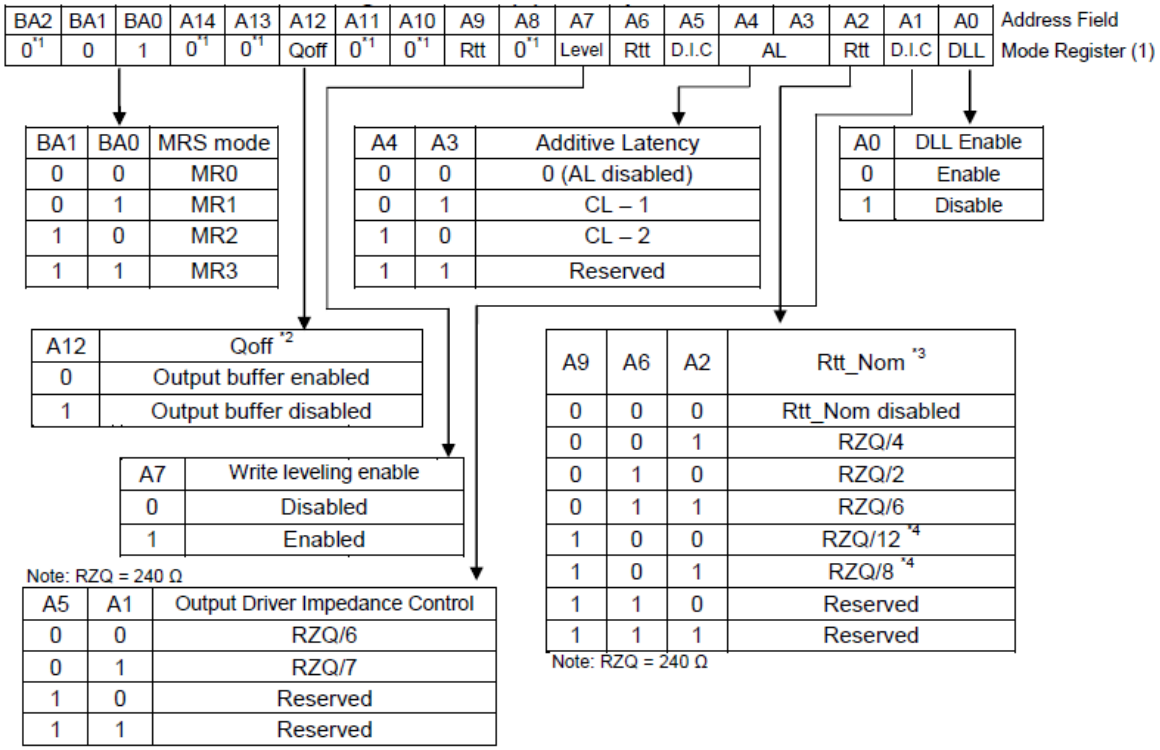
The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer: WR min [cycles] = Roundup (tWR [ns]/tCK [ns]). The WR must be programmed to be equal or larger than tWR (min).

Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.



BA2	BA1	BA0	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*1	0	1	0*1	0*1	Qoff	0*1	0*1	Rtt	0*1	Level	Rtt	D.I.C	AL		Rtt	D.I.C	DLL	Address Field / Mode Register (1)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL – 1
1	0	CL – 2
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled

A7	Write leveling enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom *3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12 *4
1	0	1	RZQ/8 *4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240 Ω

Note: RZQ = 240 Ω

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Note1: Reserved for future use and must be set to 0 when programming the MR.

Note2: Outputs disabled - DQs, DQSs, DQS#s.

Note3: In Write leveling Mode (MR1 [bit7] = 1) with MR1 [bit12] =1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1 [bit7] = 1) with MR1 [bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

Note4: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enable upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0, 0}, to disable Dynamic ODT externally

Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bit A1 and A5) as shown in MR1 definition figure.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in MR.

Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support ‘write leveling’ in DDR3 SDRAM to compensate for skew.

Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit 12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to ‘0’.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below

BA2	BA1	BA0	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*1	1	0	0*1				Rtt_WR		0*1	SRT	0*1	CWL			0*1			Address Field / Mode Register (2)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg)≧2.5ns)
0	0	1	6 (2.5ns＞tCK(avg)≧1.875ns)
0	1	0	7 (1.875ns＞tCK(avg)≧1.5ns)
0	1	1	8 (1.5ns＞tCK(avg)≧1.25ns)
1	0	0	9 (1.25ns＞tCK(avg)≧1.07ns)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A10	A9	RTT_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

Note1: Reserved for future use and must be set to 0 when programming the MR.

Note2: The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
During write leveling, Dynamic ODT is not available.

CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings.
DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available.

Self-Refresh Temperature (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode’s refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a TC of 85°C while in self refresh mode.

When SRT is enabled, the DRAM self refresh is changed internally from 1x to 2x, regardless of the case temperature. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode. The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if SRT is enabled, the standard self refresh current specifications do not apply (see Extended Temperature Usage).

Extended Temperature Usage

DDR3 SDRAM supports the optional extended case temperature (TC) range of 0°C to 95°C. The extended temperature range DRAM must be refreshed externally at 2x (double refresh) anytime the case temperature is above 85°C (and does not exceed 95°C). The external refresh requirement is accomplished by reducing the refresh period from 64ms to 32ms. Thus, SRT must be enabled when TC is above 85°C or self refresh cannot be used until TC is at or below 85°C.

Self-Refresh mode summary

MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh mode
0	Self-Refresh rate appropriate for the Normal Temperature Range	Normal (0 ~ 85C)
1	Self-Refresh appropriate for either the Normal or Extended Temperature Ranges.The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 ~ 95C)

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*1	1	1	0*1												MPR	MPR Loc		Mode Register (3)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	MPR
0	Normal operation *3
1	Dataflow from MPR

A1	A0	MPR location
0	0	Predefined pattern *2
0	1	RFU
1	0	RFU
1	1	RFU

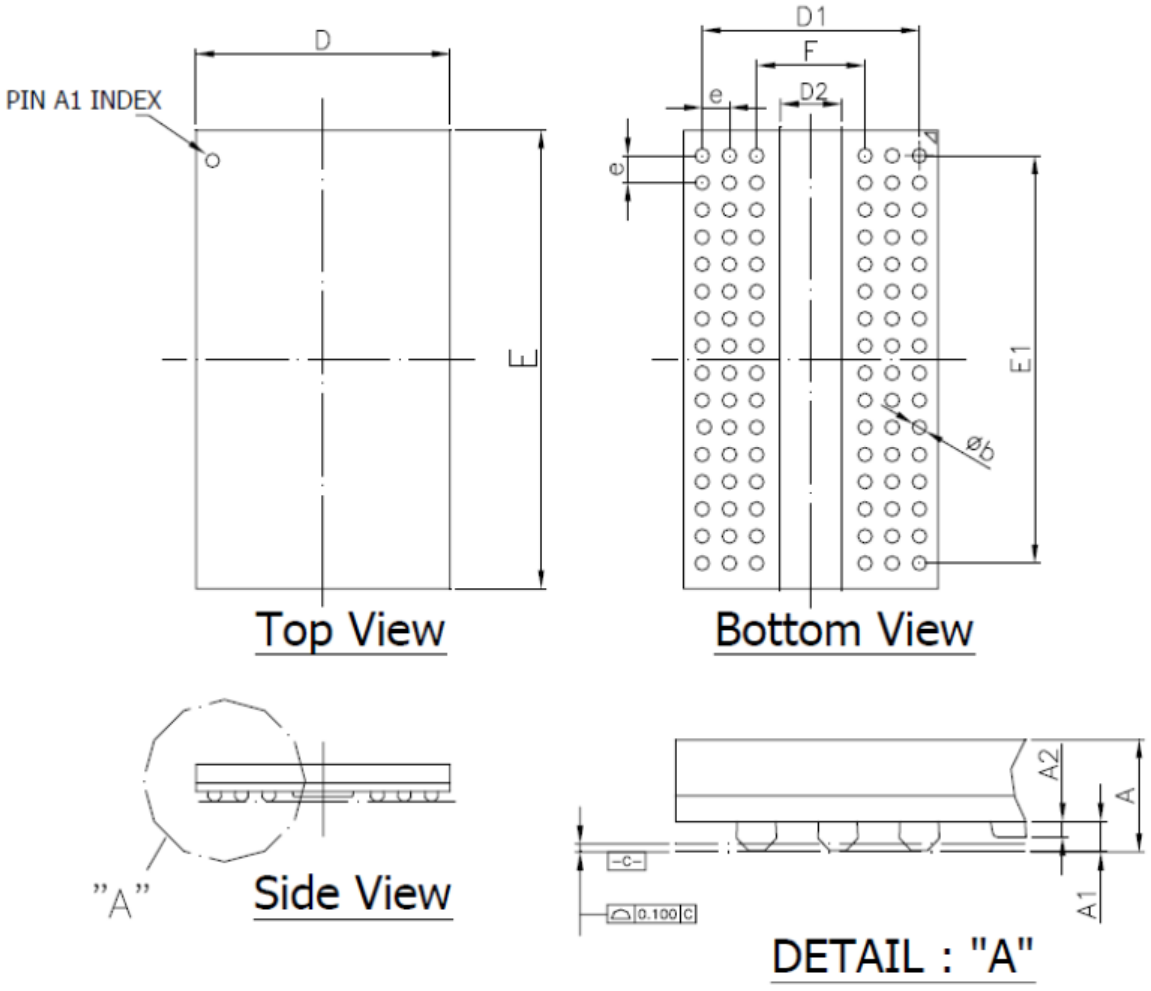
Note1: BA2, A3 - A14 are RFU and must be programmed to 0 during MRS.

Note2: The predefined pattern will be used for read synchronization.

Note3: When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Package Description: 96Ball-FBGA 7.5x13.5x1.2mm

Solder ball: Lead free (Sn-Ag-Cu)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.010	--	0.016	0.25	--	0.40
A2	--	--	0.008	--	--	0.20
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.528	0.531	0.535	13.40	13.50	13.60
D1	--	0.252	--	--	6.40	--
E1	--	0.472	--	--	12.00	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
D2	--	--	0.081	--	--	2.05

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Jul. 2020	Ternence Chen	N/A
1.0	First SPEC. release.	Aug. 2020	Rico Yang	N/A