8Gb (64Mx8Banksx16) DDR3 SDRAM

Descriptions

The H2A408G1666C is a high speed Double Date Rate 3 (DDR3) low voltage Synchronous DRAM fabricated with ultra high performance CMOS process which organized as 64Mbits x 8 banks by 16 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin (DDR3-1866) for general applications. The chip is designed to comply with the following key DDR3 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) On Die Termination, (4) programmable driver strength data,(5) seamless BL4 access with bank-grouping. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional differential data strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style.

Features

- Power Supply: VDD = VDDQ = 1.5V ±0.075V
- All inputs and outputs are compatible with SSTL_15 interface.
- Fully differential clock inputs (CK, /CK) operation.
- Eight Banks
- Posted CAS by programmable additive latency
- Bust length: 4 with Burst Chop (BC) and 8.
- CAS Write Latency (CWL): 5,6,7,8
- CAS Latency (CL): 6, 7, 8, 9, 10, 11
- Write Latency (WL) =Read Latency (RL) -1.
- Bi-directional Differential Data Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available both for 8 & 4 with BC.
- Multi Purpose Register (MPR) for pre-defined pattern read out
- On Die Termination (ODT) options: Synchronous ODT, Dynamic ODT, and Asynchronous ODT
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- Refresh Interval: 85°C ~ 95°C
- RoHS Compliance
- Driver Strength: RZQ/7, RZQ/6(RZQ=240Ω)
- High Temperature Self-Refresh rate enable
- ZQ calibration for DQ drive and ODT
- RESET pin for initialization and reset function

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A408G1666CDDC	512M X 16	DDR3-1333MHz 9-9-9	96Ball BGA, 9x14mm	Commercial
H2A408G1666CFDC	512M X 16	DDR3-1600MHz 11-11-11	96Ball BGA, 9x14mm	Commercial
H2A408G1666CGDC	512M X 16	DDR3-1866MHz 13-13-13	96Ball BGA, 9x14mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDDQ	DQU13	DQU15	A	DQU12	VDDQ	VSS
VSSQ	VDD	VSS	B	/DQSU	DQU14	VSSQ
VDDQ	DQU11	DQU9	C	DQSU	DQU10	VDDQ
VSSQ	VDDQ	/DMU	D	DQU8	VSSQ	VDD
VSS	VSSQ	DQL0	E	DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL	F	DQL1	DQL3	VSSQ
VSSQ	DQL6	/DQSL	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4	H	DQL7	DQL5	VDDQ
NC	VSS	/RAS	J	CK	VSS	NC
ODT	VDD	/CAS	K	/CK	VDD	CKE
NC	/CS	/WE	L	A10 / AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12 /BC	BA1	VDD
VSS	A5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	/RESET	A13	T	A14	A8	VSS

96-Ball FBGA – x16 Ball Descriptions

Pin	Symbol	Description
J7,K7	CK, /CK	**(System Clock)** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK . Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
L2	/CS	**(Chip Select)** All commands are masked when /CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
K9	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self- refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including self-refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self -refresh.
N3,P7,P3,N2, P8,P2,R8,R2, T8,R3,L7,R7, N7,T3,T7	A0~A9,A10(AP), A11,A12(/BC), A13,A14	**(Address)** Provided the row address (RA0 – RA13) for active commands and the column address (CA0-CA9) and auto precharge bit for read/write commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). The address inputs also provide the op-code during Mode Register Set commands. A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
M2,N8,M3	BA0, BA1,BA2	**(Bank Address)** BA0 – BA2 define to which bank an active, read, write or precharge command is being applied. Bank address also determines if the mode register is to be accessed during a MRS cycle.
K1	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS , DM/TDQS, and TDQS signal. The ODT pin will be ignored if the Mode Register ***MR1*** is programmed to disable ODT.

E3, F7, F2, F8, H3, H8, G2, H7, D7, C3, C8, C2 F3, G3, C7, B7	DQL, DQU, DQS, /DQS DQSL /DQSL DQSU,/DQSU	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, DQSU are paired with differential signals /DQS, /DQSL, /DQSU to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
D3,E7	/DMU, DML	**(Termination Data Strobe)** When enabled via Mode Register A11=1 in ***MR1***, DRAM will enable the same termination resistance function on TDQS /TDQS that is applied DQS/DQS. When disabled via mode register A11=0 in ***MR1***, DM/TDQS will provide the data mask function and /TDQS is not used.
J3, K3, L3	/RAS ,/CAS , /WE	**(Command Inputs)** /RAS , /CAS and /WE (along with /CS) define the command being entered.
E3, F7, F2, F8, H3, H8, G2, H7	DQL0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
E1, N1, R1, T1, B2, J2, K2,B3, G7, J8, K8, A9, D9,M9, N9, P9, R9, T9	VDD,VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
A1, C1, F1, D2, H2, A8, C9,E9, H9, B1, D1, G1, E2, C8,E8, B9, F9, G9	VDDQ VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
L8	ZQ	**(ZQ Calibration)** Reference pin for ZQ calibration

N2	/RESET	**(Active Low Asynchronous Reset)** Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD,i.e. 1.20V for DC high and 0.30V for DC low.
H1	VREFDQ	**(Reference Voltage)** Reference voltage for DQ
M8	VREFCA	**(Reference Voltage)** Reference voltage for CA
J1, L1, J9, L9	NC	**(No Connection)** No internal electrical connection is present.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.4 ~ +1.975		V
VDD	Power Supply Voltage	-0.4 ~ +1.975		V
VDDQ	Power Supply Voltage	-0.4 ~ +1.975		V
TOP	Operating Temperature Range	Commercial	0 ~ +95	°C
TSTG	Storage Temperature Range	-55 ~ +100		°C

Note: 1. VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 × VDDQ. When VDD and VDDQ are <500mV, VREF can be <=300mV.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Power Supply for I/O Voltage	1.425	1.5	1.575	V
I_I	Input leakage current	-2	-	2	uA
I_{VREF}	V_{REF} supply leakage current	-1	-	1	uA

Input/ Output Capacitance

Symbol	Parameters	Pins	Min.	Max.	Unit	Notes
CCK	Input pin capacitance, CK, /CK	CK, /CK	0.8	1.4	pF	
CDCK	Delta input pin capacitance, CK, /CK		0	0.15	pF	
CIN_CTRL	Input pin capacitance, control pins	/CS,CKE,ODT	0.75	1.3	pF	
CDIN_CTRL	Delta input pin capacitance, control pins		-0.4	0.2	pF	
CIN_ADD_CMD	Input pin capacitance, address and command pins	/RAS,/CAS,/WE, Address	0.75	1.3	pF	
CDIN_ADD_CMD	Delta input pin capacitance, address and command pins		-0.4	0.4	pF	
CIO	Input/output pins capacitance	DQ,DQS,/DQS TDQS,/TDQS, DM	1.4	2.3	pF	
CDIO	Delta input/output pins capacitance		-0.5	0.3	pF	
CDDQS	Delta input/output pins capacitance	DQS, /DQS	0	0.15	pF	
CZQ	Input/output pin capacitance, ZQ	ZQ	-	3	pF	

Notes1: VDD = 1.35V (1.283–1.45V), VDDQ = VDD, VREF = VSS, f = 100 MHz, TC = 25°C. VOUT(DC) = 0.5 × VDDQ, VOUT = 0.1V (peak-to-peak).

Notes2: DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

Notes3: Includes TDQS, TDQS#. CDDQS is for DQS vs. DQS# and TDQS vs. TDQS# separately.

Notes4: CDIO = CIO(DQ) - 0.5 × (CIO(DQS) + CIO(DQS#)).

Notes5: Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR =A[n:0], BA[2:0].

Notes6: CDI_CTRL = CI(CTRL) - 0.5 × (CCK(CK) + CCK(CK#)).

Notes7: CDI_CMD_ADDR = CI(CMD_ADDR) - 0.5 × (CCK(CK) + CCK(CK#))

Recommended DC Operating Conditions

VDD/VDDQ = 1.5V±0.075V

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I_{DD0}	**Operating One Bank Active-Precharge Current:** CKE: High; External clock: On; BL: 8(1); AL: 0;/CS : High between ACT and PRE; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0, 0, 1,1,2,2... Output Buffer and RTT: Enabled in Mode Registers (2); ODT Signal: stable at 0.	69	67	65	mA
I_{DD1}	**Operating One Bank Active-Read-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	91	88	85	mA
I_{DD2P1}	**Precharge Power-Down Current Fast Exit:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	16	14	12	mA
I_{DD2N}	**Precharge Standby Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	38	36	34	mA
I_{DD3P}	**Active Power-Down Current:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	38	36	34	mA
I_{DD4W}	**Operating Burst Write Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	195	185	175	mA
I_{DD4R}	**Operating Burst Read Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between RD; Command, Address: par-tially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	195	185	175	mA

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I_{DD5B}	**Burst Refresh Current:** CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; /CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	250	245	240	mA
I_{DD6}	**Self Refresh Current: Normal Temperature Range;** TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	24	24	24	mA
I_{DD7}	**Operating Bank Interleave Read Current;** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	230	220	210	mA

Note 1: TC = 85°C; SRT and ASR are disabled

Note 2: Enabling ASR could increase IDDx by up to an additional 2mA.

Note 3: Restricted to TC (MAX) = 85°C.

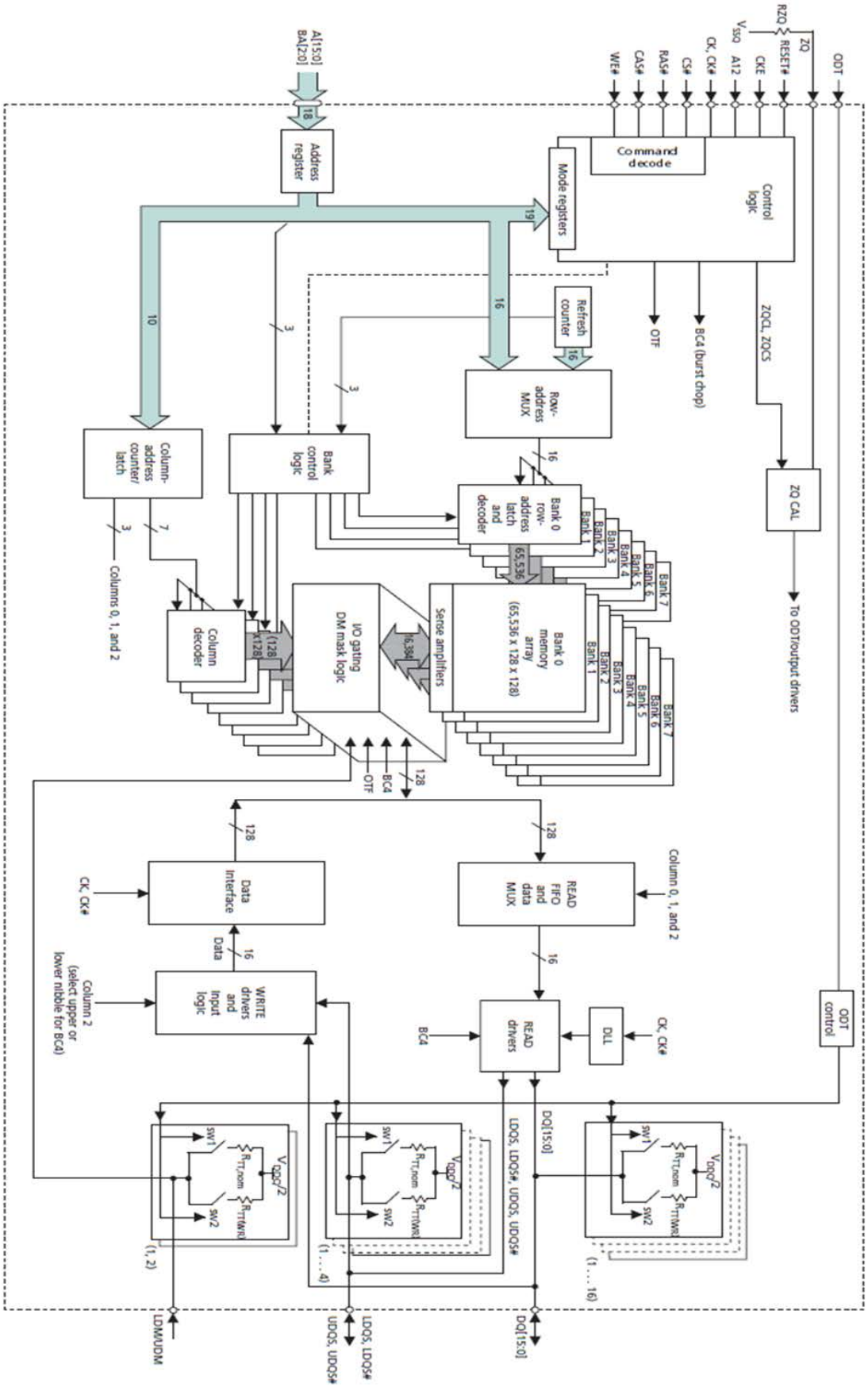
Note 4: TC = 85°C; ASR and ODT are disabled; SRT is enabled.

Note 5: The IDD values must be derated (increased) on IT-option devices when operated outside of the range 0°C <=TC <= +85°C:

5a. When TC < 0°C: IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6 and IDD7 must be derated by 7%.

5b. When TC > 85°C: IDD0, IDD1, IDD2N, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; IDD2Px must be derated by 30%.

Functional Block Diagram



AC Operating Test Characteristics

DDR3-1333 & DDR3-1600 & DDR3-1866 Speed Bins

VDD/VDDQ = 1.5V±0.075V

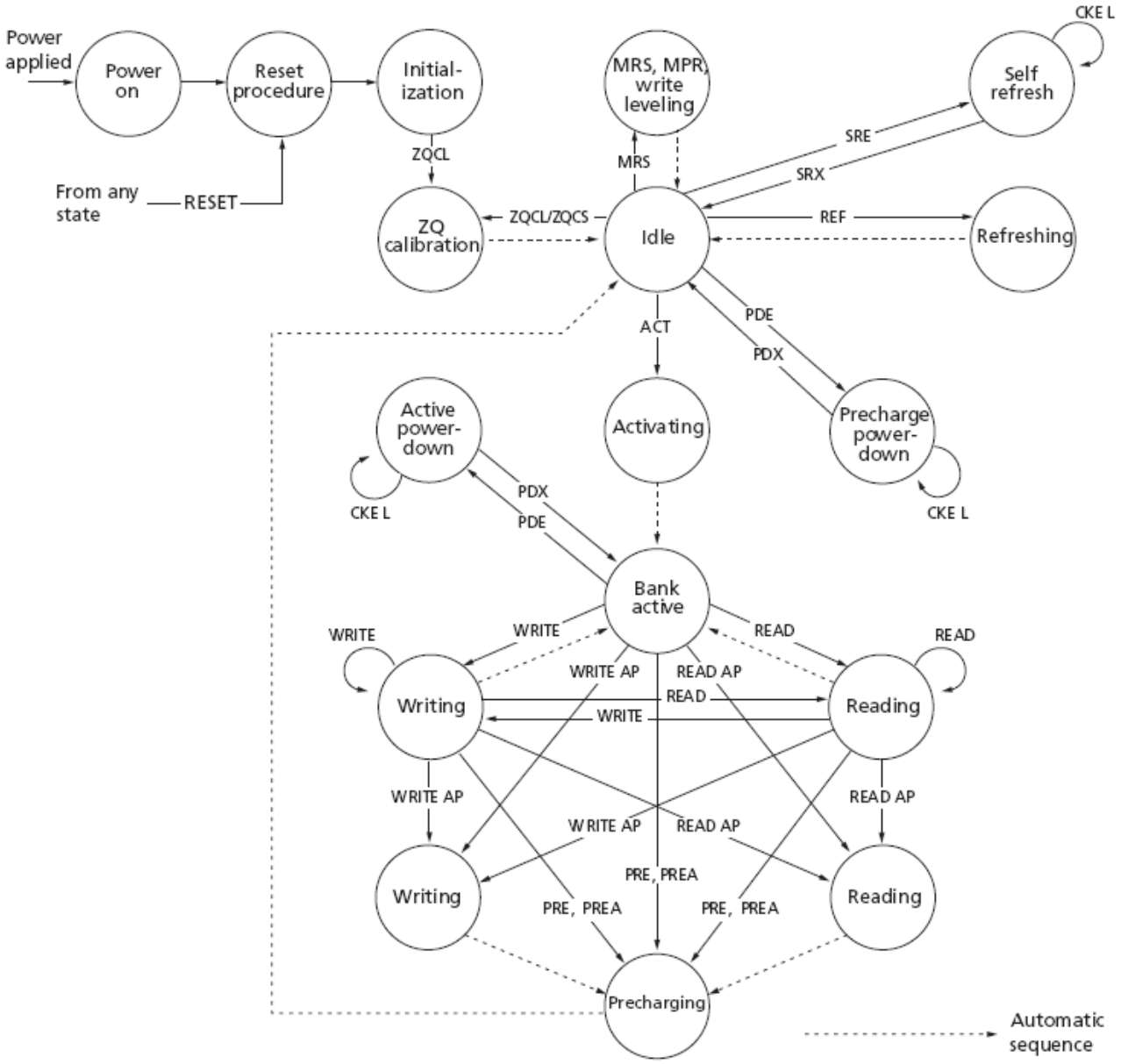
Symbol	Speed Bin	DDR3-1866		DDR3-1600		DDR3-1333		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
tAA	Internal read command to first data	13.91	20	13.75	-	13.5	-	ns	
tRCD	Active to read or write delay	13.91	-	13.75	-	13.5	-	ns	
tRP	Precharge command period	13.91	-	13.75	-	13.5	-	ns	
tRC	Active to active/auto refresh command	47.91	-	48.75	-	49.5	-	ns	
tRAS	Active to precharge command period	34	9*t_{REFI}	35	9*t_{REFI}	36	9*t_{REFI}	ns	1
tCK (AVG)	Average Clock Cycle, CL=6, CWL=5	2.5	3.3	2.5	3.3	2.5	3.3	ns	2
tCK (AVG)	Average Clock Cycle, CL=7, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	2
tCK (AVG)	Average Clock Cycle, CL=8, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	2
tCK (AVG)	Average Clock Cycle, CL=9, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	2
tCK (AVG)	Average Clock Cycle, CL=10, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	2
tCK (AVG)	Average Clock Cycle, CL=11, CWL=8	1.25	<1.5	1.25	<1.5	-	-	ns	2
tCK (AVG)	Average Clock Cycle, CL=12, CWL=9	Reserved							
tCK (AVG)	Average Clock Cycle, CL=13, CWL=9	1.07	<1.25						
-	Support CL Settings	6,7,8,9,10,11,13		6,7,8,9,10,11		6,7,8,9,10		nCK	
-	Support CWL Settings	5,6,7,8,9		5,6,7,8		5,6,7		nCK	

Notes1: tREFI depends on TOPER.

Notes2: The CL and CWL settings result in tCK requirements. When making a selection of tCK,both CL and CWL requirement settings need to be fulfilled.

Notes3: Reserved settings are not allowed

Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA(2:0)	An	A12	A10	A(11,9:0)
		n-1	N									
MODE REGISTER SET	MRS	H	H	L	L	L	L	BA	OP Code			
REFRESH	REF	H	H	L	L	L	H	V	V	V	V	V
Self refresh entry	SRE	H	L	L	L	L	H	V	V	V	V	V
Self refresh exit	SRX	L	H	H	V	V	V	V	V	V	V	V
				L	H	H	H					
Single-bank PRECHARGE	PRE	H	H	L	L	H	L	BA	V	V	L	V
PRECHARGE all banks	PREA	H	H	L	L	H	L	V		V	H	V
Bank ACTIVATE	ACT	H	H	L	L	H	H	BA	Row address(RA)			
WRITE (BL8MRS,BC4MRS)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA
WRITE (BC4OTF)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA
WRITE (BL8OTF)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA
WRITE with auto pre-charge (BL8MRS,BC4MRS)	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA
WRITE with auto pre-charge (BC4OTF)	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA
WRITE with auto pre-charge (BL8OTF)	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA
READ (BL8MRS,BC4MRS)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA
READ (BC4OTF)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA
READ (BL8OTF)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA
READ with auto pre-charge (BL8MRS,BC4MRS)	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA
READ with auto pre-charge (BC4OTF)	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA
READ with auto pre-charge (BL8OTF)	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA
NO OPERATION	NOP	H	H	L	H	H	H	V	V	V	V	V
Device DESELECTED	DES	H	H	H	X	X	X	X	X	X	X	X
Power-down entry	PDE	H	L	L	H	H	H	V	V	V	V	V
				H	V	V	V					
Power-down exit	PDX	L	H	L	H	H	H	V	V	V	V	V
				H	V	V	V					
ZQ CAL. LONG	ZQCL	H	H	L	H	H	L	X	X	X	H	X
ZQ CAL. SHORT	ZQCS	H	H	L	H	H	L	X	X	X	L	X

Note1: Commands are defined by the states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-, density-, and configurationdependent.

Note2: RESET# is enabled LOW and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.

Note3: The state of ODT does not affect the states described in this table.

Note4: Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.

Note5: "V" means "H" or "L" (a defined logic level), and "X" means "Don't Care."

Note6: Self refresh exit is asynchronous

Note7: Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.

Note8: The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.

Note9: The DES and NOP commands perform similarly.

Note10: The power-down mode does not perform any REFRESH operations.

Note11: ZQ CALIBRATION LONG is used for either ZQinit (first ZQCL command during initialization) or ZQoper (ZQCL command after initialization).

CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	
	L	H	DESELECT or NOP	Power down exit	
Self Refresh	L	L	X	Maintain self refresh	
	L	H	DESELECT or NOP	Self refresh exit	
Bank Active	H	L	DESELECT or NOP	Active power down entry	
Reading	H	L	DESELECT or NOP	Power down entry	
Writing	H	L	DESELECT or NOP	Power down entry	
Precharging	H	L	DESELECT or NOP	Power down entry	
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	
	H	L	REFRESH	Self refresh	
For more details with all signals, see “Command Truth Table”					6

Note1: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note2: tCKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKE (MIN) + tIH.

Note3: Current state = The state of the DRAM immediately prior to clock edge n.

Note4: CKE (n) is the logic state of CKE at clock edge n; CKE (n - 1) was the state of CKE at the previous clock edge.

Note5: COMMAND is the command registered at the clock edge. Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.

Note6: Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All self refresh exit and power-down exit parameters are also satisfied.

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power. RESET# is recommended to be below 0.2 × VDDQ during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (RTT is also High-Z).All other inputs, including ODT, may be undefined.

   During power-up, either of the following conditions may exist and must be met:
   - Condition A:
     • VDD and VDDQ are driven from a single-power converter output and are ramped with a maximum delta voltage between them of □V □ 300mV. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side, and must be greater than or equal to VSSQ and VSS on the other side.
     • Both VDD and VDDQ power supplies ramp to VDD,min and VDDQ,min within tVDDPR = 200ms.
     • VREFDQ tracks VDD × 0.5, VREFCA tracks VDD × 0.5.
     • VTT is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, tVTD should be greater than or equal to 0 to avoid device latchup.
   - Condition B:
     • VDD may be applied before or at the same time as VDDQ.
     • VDDQ may be applied before or at the same time as VTT, VREFDQ, and VREFCA.
     • No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200µs to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.

3. CKE must be LOW 10ns prior to RESET# transitioning HIGH.

4. After RESET# transitions HIGH, wait 500µs (minus one clock) with CKE LOW.

5. After the CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least tIS prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.

6. After CKE is registered HIGH and after tXPR has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).

7. Issue an MRS command to MR3 with the applicable settings.

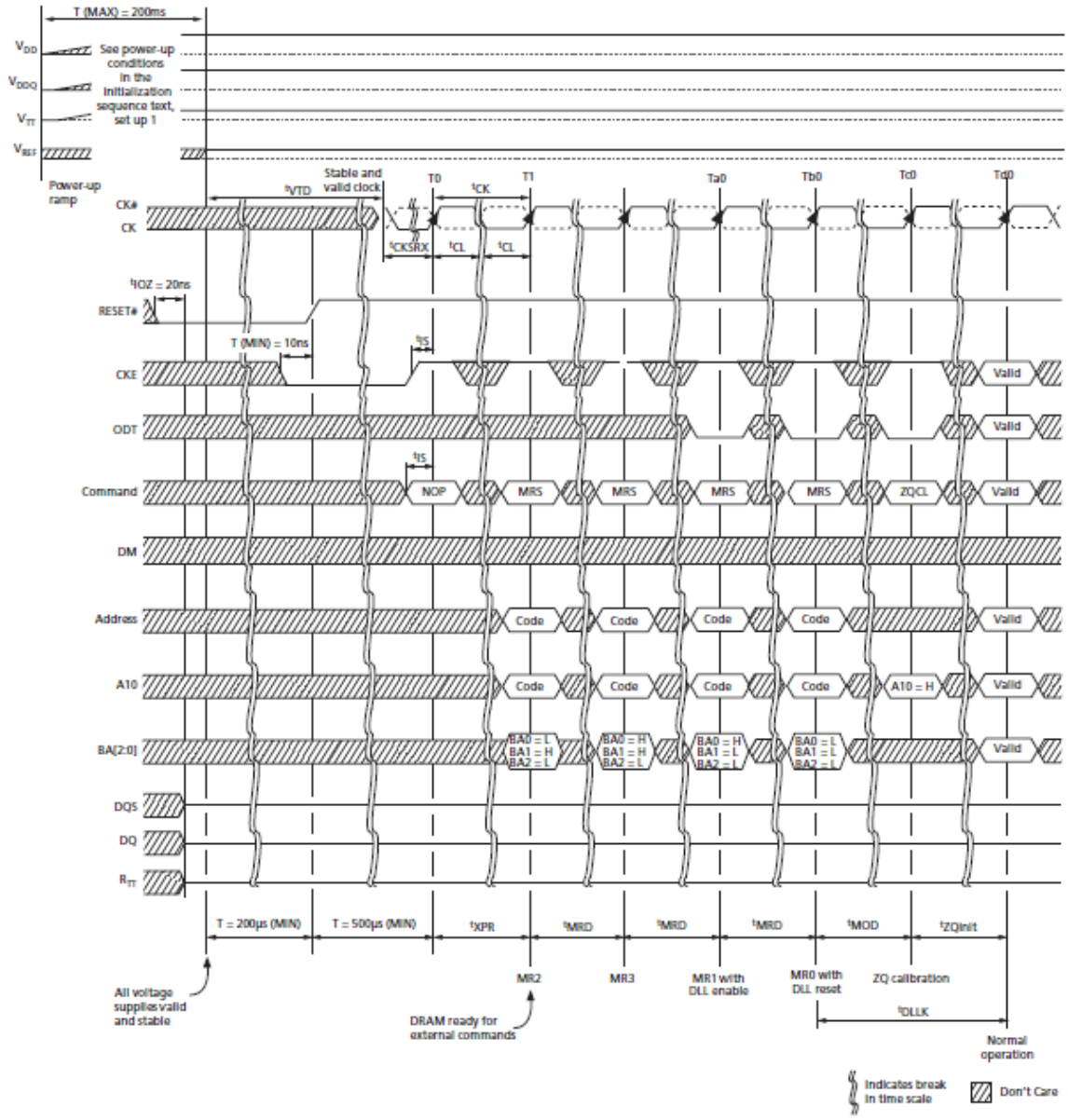
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.

9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. tDLLK (512) cycles of clock input are required to lock the DLL.

10. Issue a ZQCL command to calibrate RTT and RON values for the process voltage temperature (PVT). Prior to normal operation, tZQinit must be satisfied.

11. When tDLLK and tZQinit have been satisfied, the DDR3 SDRAM will be ready for normal operation.

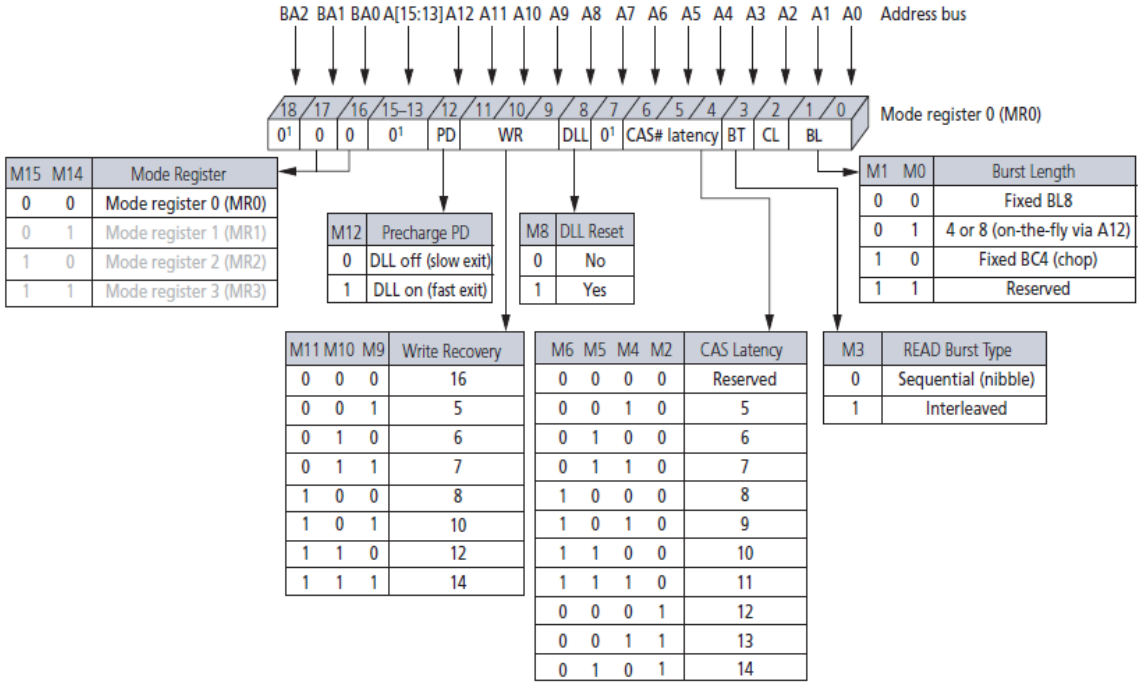
Reset and Power up initialization sequence



Mode Register Definition

Mode Register MR0

The base register, mode register 0 (MR0), is used to define various DDR3 SDRAM modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and precharge power-down mode



M15	M14	Mode Register
0	0	Mode register 0 (MR0)
0	1	Mode register 1 (MR1)
1	0	Mode register 2 (MR2)
1	1	Mode register 3 (MR3)

M12	Precharge PD
0	DLL off (slow exit)
1	DLL on (fast exit)

M8	DLL Reset
0	No
1	Yes

M1	M0	Burst Length
0	0	Fixed BL8
0	1	4 or 8 (on-the-fly via A12)
1	0	Fixed BC4 (chop)
1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

M6	M5	M4	M2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

M3	READ Burst Type
0	Sequential (nibble)
1	Interleaved

Note1: MR0[18, 15:13, 7] are reserved for future use and must be programmed to 0.

Burst Type

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0123ZZZZ	0123ZZZZ
	R	0	0	1	1230ZZZZ	1032ZZZZ
	R	0	1	0	2301ZZZZ	2301ZZZZ
	R	0	1	1	3012ZZZZ	3210ZZZZ
	R	1	0	0	4567ZZZZ	4567ZZZZ
	R	1	0	1	5674ZZZZ	5476ZZZZ
	R	1	1	0	6745ZZZZ	6745ZZZZ
	R	1	1	1	7456ZZZZ	7654ZZZZ
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

Note1: Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.

Note2: Z = Data and strobe output drivers are in tri-state.

Note3: V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.

Note4: X = “Don’t Care.”

CAS Latency

CAS latency (CL) is defined by MR0[6:4], CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. CL can be set to 5 through 14. DDR3 SDRAM do not support half-clock latencies.

DLL Reset

DLL RESET is defined by MR0[8]. Programming MR0[8] to 1 activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of 0 after the DLL RESET function has been initiated.

Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 512 (tDLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization can result in invalid output timing specifications, such as tDQSCK timings.

Write Recovery

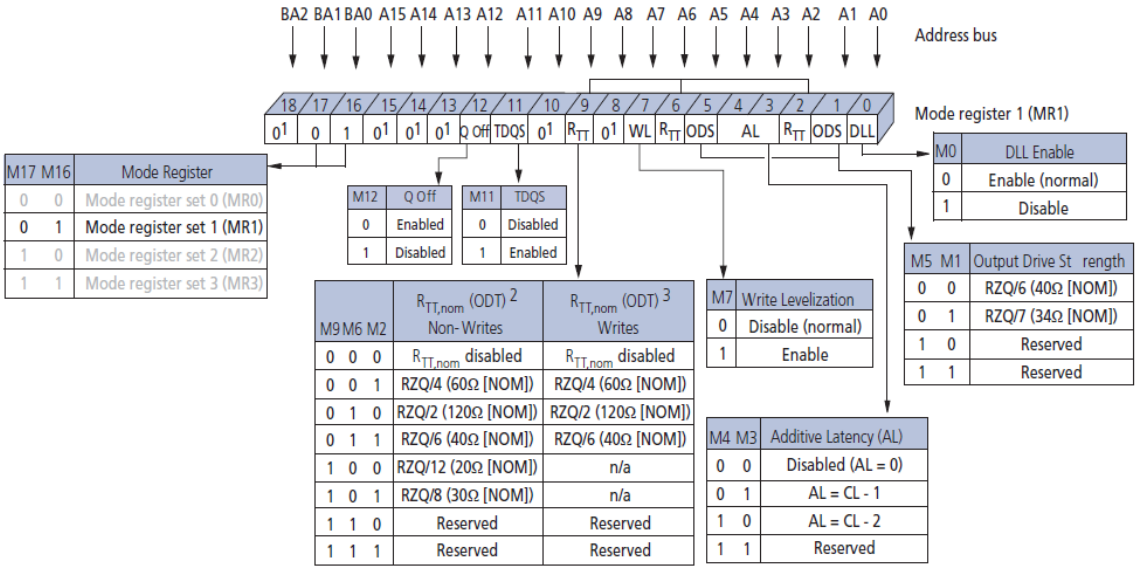
WRITE recovery time is defined by MR0[11:9]. Write recovery values of 5, 6, 7, 8, 10, or 12 can be used by programming MR0[11:9]. The user is re- quired to program the correct value of write recovery, which is calculated by dividing tWR (ns) by tCK (ns) and rounding up a noninteger value to the next integer: WR (cycles) = roundup (tWR (ns)/tCK (ns)).

Precharge PD DLL

The precharge power-down (precharge PD) bit applies only when precharge powerdown mode is being used. When MR0[12] is set to 0, the DLL is off during precharge power-down, providing a lower standby current mode; however, tXPDLL must be satisfied when exiting. When MR0[12] is set to 1, the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, tXP must be satisfied when exiting.

Mode Register MR1

The mode register 1 (MR1) controls additional functions and features not available in the other mode registers: Q OFF (OUTPUT DISABLE),, DLL ENABLE/DLL DISABLE, RTT,nom value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, until RESET# goes LOW, or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is performed correctly. The MR1 register must be loaded when all banks are idle and no bursts are in progress.The controller must satisfy the specified timing parameters tMRD and tMOD before initiating a subsequent operation.



Note1: MR1[18, 15:13, 10, 8] are reserved for future use and must be programmed to 0.

Note2: During write leveling, if MR1[7] and MR1[12] are 1, then all RTT,nom values are available for use.

Note3: During write leveling, if MR1[7] is a 1, but MR1[12] is a 0, then only RTT,nom write values are available for use.

DLL Enable/Disable

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command. The DLL must be enabled for normal operation.DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation.Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled even upon exit of SELF REFRESH operation until it is re-enabled and reset.

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled.Disabling the DLL also implies the need to change the clock frequency.

ODT Rtt Values

ODT resistance RTT,nom is defined by MR1[9, 6, 2]. The RTT termination value applies to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls. DDR3 supports multiple RTT termination values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240 ohm.Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. RTT,nom termination is allowed any time after the DRAM is initialized,calibrated, and not performing read access, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT (RTT(WR)) enabled temporarily replaces RTT,nom with RTT(WR).The actual effective termination, RTT(EFF), may be different from the RTT targeted due to nonlinearity of the termination. For RTT(EFF) values and calculations.The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT for any or all devices.The ODT input control pin is used to determine when RTT is turned on (ODTL on) and off (ODTL off), assuming ODT has been enabled via MR1[9, 6, 2].Timings for ODT are detailed in On-Die Termination (ODT).

Posted CAS additive Latency

POSTED CAS ADDITIVE latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1[4, 3] define the value of AL. MR1[4, 3] enable the user to program the DDR3 SDRAM with AL = 0, CL - 1, or CL - 2.

Write Leveling

The WRITE LEVELING function is enabled by MR1[7].Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks.The fly-by topology benefits from a reduced number of stubs and their lengths. However,fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining tDQSS, tDSS, and tDSH specifications without supporting write leveling in systems which use fly-by topology-based modules. Write leveling timing and detailed operation information is provided in Write Leveling.

Output Enable/Disable

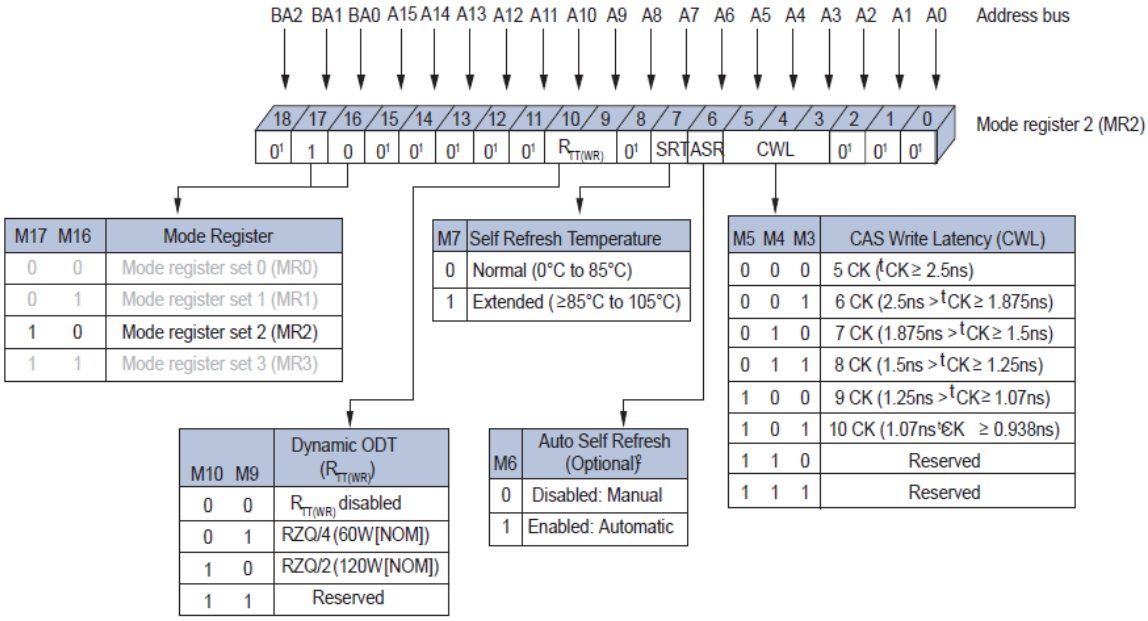
The OUTPUT ENABLE function is defined by MR1[12]. When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3 SDRAM outputs (DQ and DQS, DQS#) are tri-stated. The output disable feature is intended to be used during IDD characterization of the READ current and during tDQSS margining (write leveling) only.

TDQS Enable

Termination data strobe (TDQS) is a feature of the x8 DDR3 SDRAM configuration that provides termination resistance (RTT) and may be useful in some system configurations.TDQS is not supported in x4 or x16 configurations. When enabled via the mode register (MR1[11]), the RTT that is applied to DQS and DQS# is also applied to TDQS and TDQS#.In contrast to the RDQS function of DDR2 SDRAM, DDR3's TDQS provides the termination resistance RTT only. The OUTPUT DATA STROBE function of RDQS is not provided by TDQS; thus, RON does not apply to TDQS and TDQS#. The TDQS and DM functions share the same ball. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided, and the TDQS# ball is not used. The TDQS function is available in the x8 DDR3 SDRAM configuration only and must be disabled via the mode register for the x4 and x16 configurations.

Mode Register MR2

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT (RTT(WR)).The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress,and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.



M17	M16	Mode Register
0	0	Mode register set 0 (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M7	Self Refresh Temperature
0	Normal (0°C to 85°C)
1	Extended (≥85°C to 105°C)

M5	M4	M3	CAS Write Latency (CWL)
0	0	0	5 CK (^{t}CK≥ 2.5ns)
0	0	1	6 CK (2.5ns >^{t}CK≥ 1.875ns)
0	1	0	7 CK (1.875ns >^{t}CK≥ 1.5ns)
0	1	1	8 CK (1.5ns >^{t}CK≥ 1.25ns)
1	0	0	9 CK (1.25ns >^{t}CK≥ 1.07ns)
1	0	1	10 CK (1.07ns >^{t}CK ≥ 0.938ns)
1	1	0	Reserved
1	1	1	Reserved

M10	M9	Dynamic ODT ($R_{TT(WR)}$)
0	0	$R_{TT(WR)}$ disabled
0	1	RZQ/4 (60W[NOM])
1	0	RZQ/2 (120W[NOM])
1	1	Reserved

M6	Auto Self Refresh (Optional)[2]
0	Disabled: Manual
1	Enabled: Automatic

Note1: MR2[18, 15:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

CAS Write Latency (CWL)

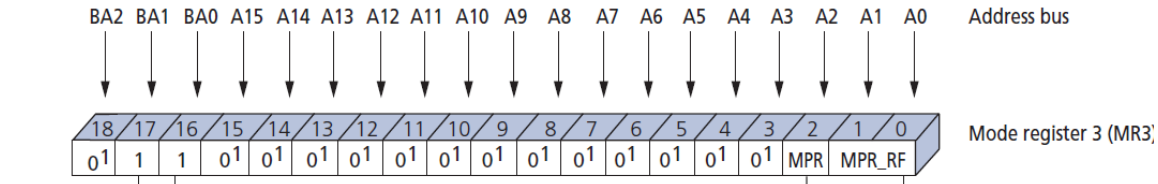
CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency. The overall WRITE latency (WL) is equal to CWL + AL.

Dynamic ODT (Rtt_WR)

The dynamic ODT (RTT(WR)) feature is defined by MR2[10, 9]. Dynamic ODT is enabled when a value is selected. This new DDR3 SDRAM feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination on-the-fly.With dynamic ODT (RTT(WR)) enabled, the DRAM switches from normal ODT (RTT_nom) to dynamic ODT (RTT(WR)) when beginning a WRITE burst and subsequently switches back to ODT (RTT_nom) at the completion of the WRITE burst. If RTT_nom is disabled, the RTT_nom value will be High-Z. Special timing parameters must be adhered to when dynamic ODT (RTT(WR)) is enabled: ODTLcnw, ODTLcnw4, ODTLcnw8, ODTH4, ODTH8,and tADC.Dynamic ODT is only applicable during WRITE cycles. If ODT (RTT_nom) is disabled, dynamic ODT (RTT(WR)) is still permitted. RTT_nom and RTT(WR) can be used independent of one other. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT (RTT_nom).

Mode Register MR3

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR).This function is controlled via the bits. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress,and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.



M17	M16	Mode Register
0	0	Mode register set (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M2	MPR Enable
0	Normal DRAM operations[2]
1	Dataflow from MPR

M1	M0	MPR READ Function
0	0	Predefined pattern[3]
0	1	Reserved
1	0	Reserved
1	1	Reserved

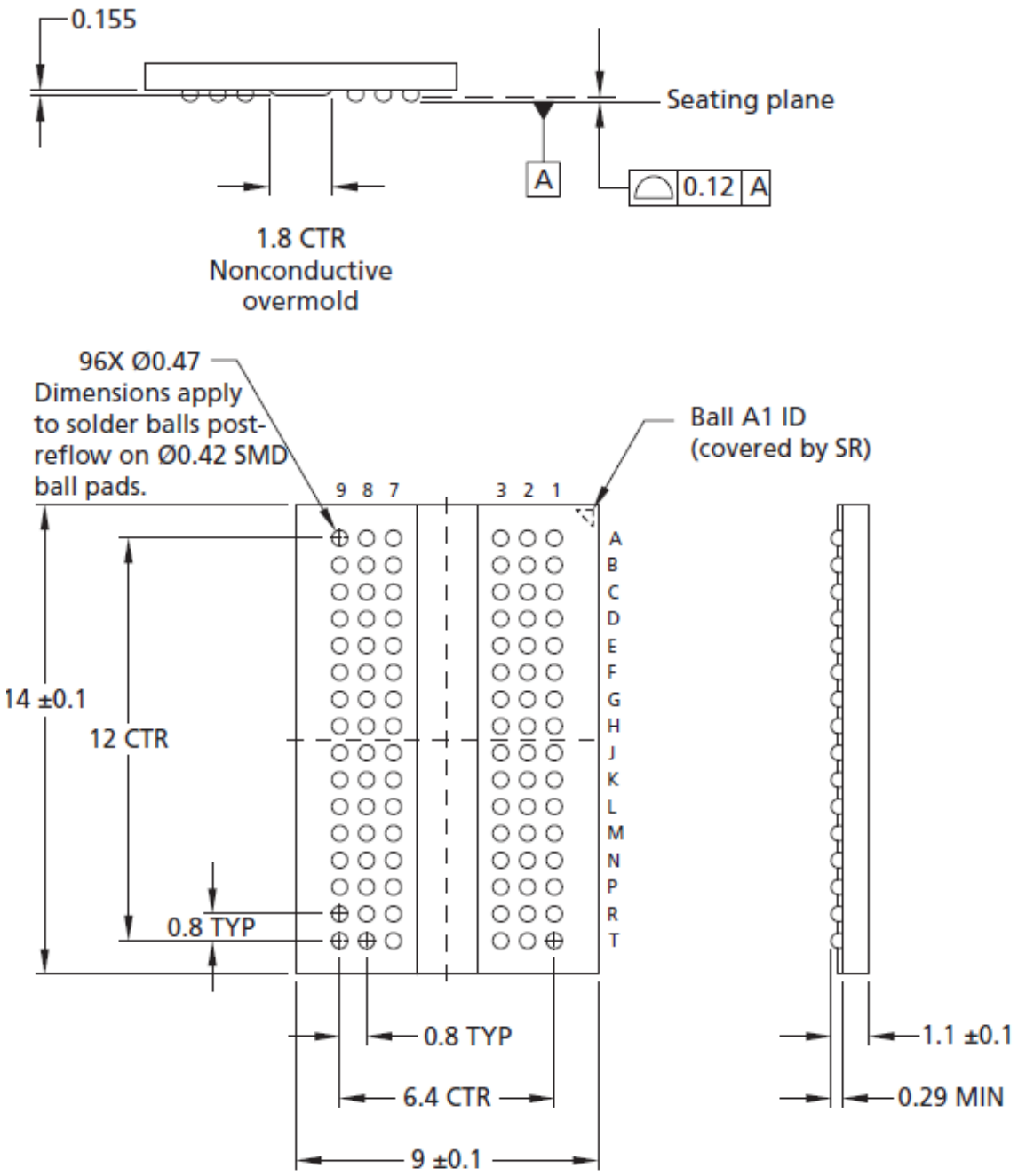
Note1: MR3[18 and 15:3] are reserved for future use and must all be programmed to 0.
Note2: When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
Note3: Intended to be used for READ synchronization.

Multi Purpose Register (MPR)

The MULTIPURPOSE REGISTER function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. If MR3[2] is a 0, then the MPR access is disabled, and the DRAM operates in normal mode. However, if MR3[2] is a 1, then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] is equal to 00, then a predefined read pattern for system calibration is selected.To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged,and tRP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or a RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled. When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0).Power-down mode, self refresh, and any other nonREAD/RDAP commands are not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Package Description: 96Ball-FBGA 9x14mm pitch: 0.8mm,

Solder ball: Lead free (Sn-Ag-Cu)



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Feb. 2018	David Chen	N/A
1.0	First SPEC. release.	Mar. 2018	Maven Hsu	N/A