Industrial Micro SSD Specification (MLC) V2.0

Micro SSD Overview

- ***Capacity***
  - *15nm: 8GB to 128GB*
- ***SATA Interface***
  - *SATA 1.5Gbps, 3Gbps, and 6Gbps interface*
- ***Flash Interface***
  - *Flash Type: MLC*
- ***Performance***
  - *Read: up to 560MB/s*
  - *Write: up to 465MB/s*
- ***Power Consumption****Note1*
  - *Active mode: ≦1,600mW*
  - *Idle mode: ≦316mW*
- ***TBW (Terabyte Written)****Note2*
  - *87 TBW for 128GB*
- ***MTBF***
  - *More than 2,000,000 hours*
- ***Minimum Average Program/Erase cycle***
  - *MLC: 3,000 cycles*
- ***Advanced Flash Management***
  - *Static and Dynamic Wear Leveling*
  - *Bad Block Management*
  - *TRIM*
  - *SMART*
  - *NCQ*
  - *Over-Provision*
  - *Firmware Update*
  - *SMARTZIP™*
- ***Low Power Management***
  - *DIPM/HIPM Mode*
- ***Storage Temperature Rang***
  - *-40°C~ 85°*
- ***Operation Temperature Range***
  - *Industrial Grade: -40°C to 85°C*
- ***RoHS compliant***

Performance and Power Consumption

Capacity	Flash Structure	Performance		Power Consumption	
		CrystalDiskMark		Read (mW)	Write (mW)
		Read (MB/s)	Write (MB/s)		
8GB	8GBx1,TSB 15nm	300	100	830	820
16GB	8GBx2,TSB 15nm	550	200	1050	1000
	16GBx1,TSB 15nm	320	80	850	800
32GB	16GBx2,TSB 15nm	550	155	990	990
64GB	16GBx4,TSB 15nm	550	345	1050	1500
128GB	16GBx8,TSB 15nm	560	465	1000	1600

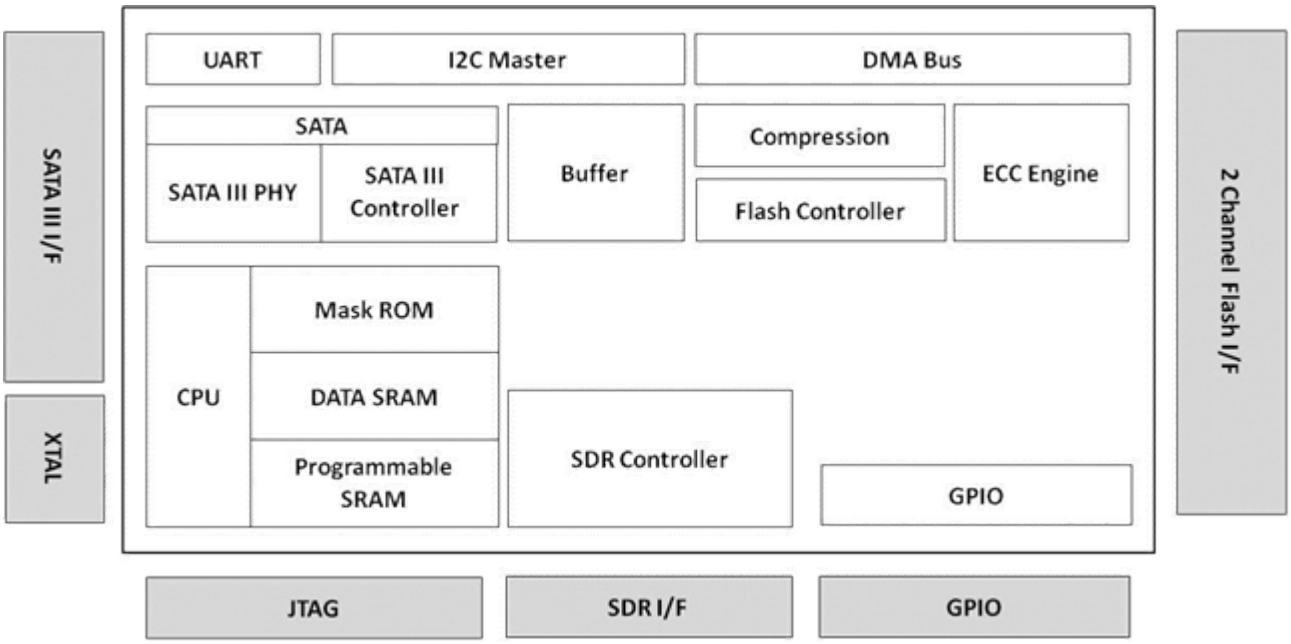
NOTE:
For more details on Power Consumption, please refer to Chapter 4.2

1. INTRODUCTION

1.1. General Description

Axeme's micro SSD delivers all the advantages of Flash Disk technology with the Serial ATA I/II/III interface in an embedded BGA form factor. Axeme micro SSD have a small physical size and can offer wide range application for industrial grade. Its capacity could provide a wide range from 8GB to 128GB with 15nm MLC. Moreover, it can reach up to 560MB/s read as well as 465MB/s write high performance, and lower power consumption makes it an ideal storage choice for high performance demanding mobile and customized devices.

1.2. Controller Block Diagram



HDA2xG22211I Controller Block Diagram

1.3. Flash Management

1.3.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, this micro SSD applies the LDPC (Low Density Parity Check) of ECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

1.3.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.
Axeme provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.3.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Axeme implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.3.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

1.3.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

1.3.6. Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input / Output Operations per Second) is improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.3.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

1.4. Low Power Management

1.4.1. DEVSLP Mode(Optional)

With the increasing need of aggressive power/battery life, SATA interfaces include a new feature, Device Sleep (DEVSLP) mode, which helps further reduce the power consumption of the device. DEVSLP enables the device to completely power down the device PHY and other sub-systems, making the device reach a new level of lower power operation. The DEVSLP does not specify the exact power level a device can achieve in the DEVSLP mode, but the power usage can be dropped down to 2mW or less.

1.4.2. DIPM/HIPMMode

SATA interfaces contain two low power management states for power saving: Partial and Slumber modes. For Partial mode, the device has to resume to full operation within 10 microseconds, whereas the device will spend 10 milliseconds to become fully operational in the Slumber mode. SATA interfaces allow low power modes to be initiated by Host (HIPM, Host Initiated Power Management) or Device (DIPM, Device Initiated Power Management). As for HIPM, Partial or Slumber mode can be invoked directly by the software. For DIPM, the device will send requests to enter Partial or Slumber mode.

1.5. Flushing Mechanism for Power Loss Protection

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. For this device, SDR performs as a cache, and its sizes include 32MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, Axeme's device applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. This Smart Cache Flush technology allows incoming data to only have a "pit stop" in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (such as random 4Kdata), the cache will be treated as an "organizer", consolidating incoming data into groups before written into the flash to improve write amplification.

1.6. Advanced Self-Defense Mechanism

1.6.1. Secure Erase

Secure Erase is a standard ATA command and will write all "0x00"to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

1.6.2. Write Protect

When a SSD contains too many bad blocks and data are continuously written in, then the SSD might not be used anymore. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

1.7. SSD Lifetime Management

1.7.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity) / WAF

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash. Typically, the P/E cycle of MLC is 3K.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WLE: Wear Leveling Efficiency (WLE) represents the ratio of the average amount of erases on all the blocks to the erases on any block at maximum.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

1.8. Adaptive Performance Tuning Technology

1.8.1. Throughput

Based on the available space of the disk, device will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, device will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

1.8.2. Predict Fetch

Normally, when the Host tries to read data from the SSD, the SSD will only perform one read action after receiving one command. However, device applies Predict Fetch to improve the read speed. When the Host issues sequential read commands to the SSD, the SSD will automatically release that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

1.8.3. 1.8.3. SmartZIP™

Write data to the NAND Flash costs time. To improve the write speed performance, this device launches with compression technique-- SmartZIP
Whether a file could be compressed or not depending on the file type, for file types have redundancy data pattern, through our embedded encode engine, we could reduce the amount of data that is actually written to the Flash. Comparing to the SSD without the compression, write efficiency is raised and the SSD endurance is also improved since Flash could be benefit from less data written for a longer SSD lifetime.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - From 8GB up to 128GB (support 48-bit addressing mode)
- **Electrical/Physical Interface**
  - SATA Interface
    - – Compatible with SATA 1.5Gbps, 3Gbps and 6Gbps interface
    - – AC coupling for transmitter and receiver
    - – Self-calibrated and embedded termination resistor at transmitter
    - – Support power management
    - – Support expanded register for SATA protocol 48-bit addressing mode
- **Flash**
  - 15nm MLC, Toggle
- **ECC Scheme**
  - Micro SSD applies the LDPC (Low Density Parity Check) of ECC algorithm.
- **Operation Voltage Supply**
  - 3.3V±5%
  - 1.8V±5%
- **Power Saving Implementation**
  - Idle mode
  - Partial mode
  - Slumber mode
- **Built-in 32-Bit Microcontroller (Core)**
- **UART function**
- **Implement Voltage Detector**
- **GPIO**
- **Support SMART and TRIM commands**

- **Performance**

Capacity	Flash Structure	Sequential	
		Read	Write
8GB	8GB x 1, TSB 15nm	300	100
16GB	8GB x 2, TSB 15nm	550	200
	16GB x 1, TSB 15nm	320	80
32GB	16GB x 2, TSB 15nm	550	155
64GB	16GB x 4, TSB 15nm	550	345
128GB	16GB x 8, TSB 15nm	560	465

NOTES:

1. The performance was measured using CrystalDiskMark v5.0x64 with SATA 3Gbps host.
2. Samples are made of 15nm MLC NAND Flash.
3. Performance may vary from flash configuration, SDR configuration, and platform.
4. The table above is for your reference only.

- **TBW (Terabytes Written)**

Capacity	Flash Structure	TBW
8GB	8GB x 1, TSB 15nm	3
16GB	8GB x 2, TSB 15nm	6
	16GB x 1, TSB 15nm	
32GB	16GB x 2, TSB 15nm	13
64GB	16GB x 4, TSB 15nm	30
128GB	16GB x 8, TSB 15nm	87

NOTES:

1. Samples are made of 15nm NAND Flash.
2. TBW may vary from flash configuration, SDR configuration, and platform. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

Temperature and Humidity

- **Temperature:**
  - Storage: -40°C to 85°C
  - Operation (Industrial Diamond grade): -40°C to 85°C

- **Humidity:**
  - RH 95% under 55°C (in operation)

Table 3-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	85°C	0% RH	72 hours
Storage	85°C	0% RH	168 hours

Test Reference: IEC 60068-2-2 **Result**: No any abnormality is detected.

Table 3-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	-40°C	0% RH	72 hours
Storage	-40°C	0% RH	168 hours

Test Reference: IEC 60068-2-1 **Result**: No any abnormality is detected.

Table 3-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	55°C	95% RH	72 hours
Storage	55°C	95% RH	96 hours

Test Reference: IEC 60068-2-3 **Result**: No any abnormality is detected.

Table 3-4 Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation	-40°C	30 min.	20 Cycle
	85°C	30 min.	20 Cycle
Storage	-40°C	30 min.	50 Cycle
	85°C	30 min.	50 Cycle

Test Reference: IEC 60068-2-14 **Result**: No any abnormality is detected.

Electrostatic Discharge (ESD)

Table 3-5 micro SSD Contact ESD Specification

Device	Capacity	Temperature	Relative Humidity	+/- 4KV	Result
Micro SSD	8GB	23.0°C	49% (RH)	Device functions are affected, but EUT will be back to its normal or operational state automatically.	**PASS**
	16GB				
	32GB				
	64GB				
	128GB				

Test Reference: IEC 61000-4-2

EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

3.2. Package Qualification

High Temperature Storage Life Test (HTSL)

Parameter	Test Condition	
Storage	Temperature	Test Duration
	150°C	168/1000 hours

Test Reference: JESD22 A103 **Result**: No any abnormality is detected.

Solderability Test

Parameter	Test Condition
Storage	85°C/85% RH 16 hours, bake 1 hour at 125°C. Molten solder temperature: 245+5°C Dwell time: 5 seconds

Note: Spec: > 95% of coating area, pinhole, voids, do not exceed 5% of total area.
Result: Pass.

Pre-condition Test

Parameter	Test Method	Test Condition
Storage	JEDS 22-A113	1. Temperature Cycle (-65°C/150°C, 5 cycles) 2. Baking (125°C, 24 hours) 3. Temp & Humidity Soaking (30°C/60% RH, 192 hours) 4. IR Reflow 3 cycles

Note: The parts passing this test will be used to do HAST and TCT.
Results: Pass

High Acceleration Stress Test (HAST/unbias)

Parameter	Test Method	Test Condition		
Storage	JEDS 22-A110	Ambient Temperature	Ambient Humidity	Test Duration
		130°C	85% (RH)	96 hours

Result: Pass

Temperature Cycling Test (TCT)

Parameter	Test Method	Test Condition		
Storage	JEDS 22-A104	High Temperature	Low Temperature	Test Duration
		150°C	-65°C	200/500 cycles

Result: Pass

X-rayTest

Parameter	Test Method	Test Condition		
Storage	ISO7816-1	Sample	Test Times	Result
		8GB 10pcs	20	Function Pass

Result: No any abnormality is detected.

3.3. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Axeme's micro SSD is more than 2,000,000 hours.

3.4. Certification & Compliance

- RoHs
- SATA Ⅲ (SATA Rev. 3.2)
- Up to ATA/ATAPI-8 (Including S.M.A.R.T)

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Parameter	Rating
VCC	3.3V
VCCQ	1.8V

4.2. Power Consumption

Current	Flash Structure	Read	Write	Partial	Slumber	Idle
8GB	8GB x 1	830	820	18	12	315
16GB	8GB x 2	1050	1000	19	13	316
	16GB x 1	850	800	15	10	265
32GB	16GB x 2	990	990	20	15	270
64GB	16GB x 4	1050	1500	18	12	280
128GB	16GB x 8	1000	1600	18	12	280

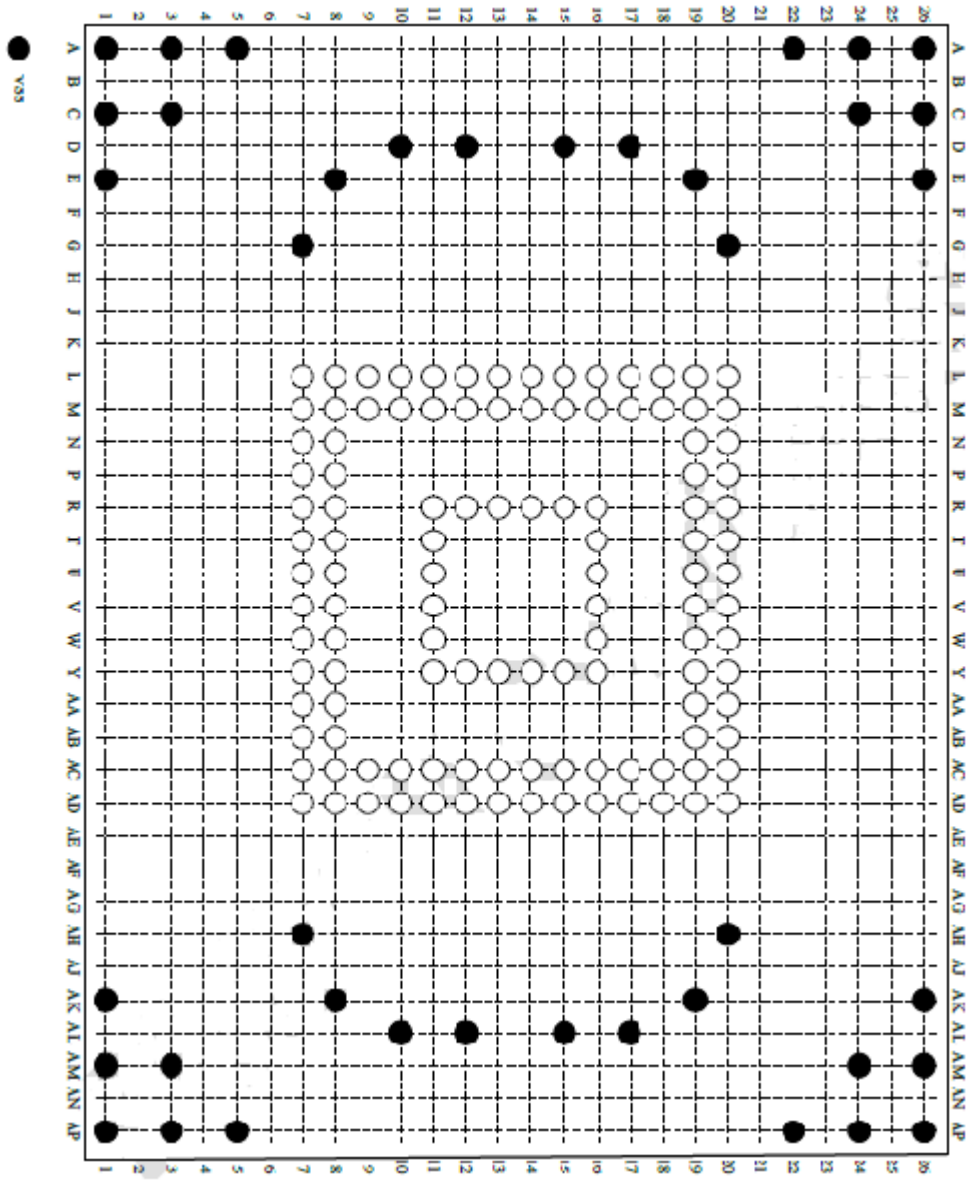
Unit: mW

NOTES:

1. The average value of power consumption is achieved based on 100% conversion efficiency.
2. The measured power voltage includes 1.8V and 3.3V.
3. Samples were built using 15nm MLC NAND Flash and measured under normal temperature.
4. Sequential R/W is measured while testing 4000MB sequential R/W 5 times by Cyrstal Disk Mark. DEVSLP is measured while entering device sleep mode for 5 minutes.
5. Power Consumption may differ according to flash configuration and platform.

5. INTERFACE

5.1. Pin Assignment and Descriptions



HDA2xG22211I micro SSDPin Assignment (Top View)

HDA2xG22211I micro SSD Pin Assignment

Table 5-1 HDA2xG22211I micro SSD Pin Descriptions

Pin Name	BGA 156	Pin Type	PU/PD	Description
UART/GPIO				
XTXD XRXD	M12 AA20	O I	PU 75K	UART transmit/receive port
GPIO0 GPIO1 GPIO2 GPIO3 GPIO6	AC14 AD13 AC13 AD11 AD9	IO	PD 75K	General purpose input/output pins
SATA interface signals				
SATA_RX_N SATA_RX_P	R7 P7	I		Differential Signal Pair A. SATA Device Receive Signal Differential Pair.
SATA_TX_N SATA_TX_P	U7 V7	O		Differential Signal Pair B. SATA Device Transmit Signal Differential Pair.
DAS	M13	O		Device Activity Signal
SATA_VCC	U8,V8			+3.3V
SATA_VSS	N7,T7,W7			Ground
Control Signals				
XTAL_IN XTAL_OUT	M10 L9	I O		Crystal input/outputpin. (30MHz)
PWR_RESETN	M9	I		Hardware Reset, low active.
Power supply Signals				
VCC	L12 M11 R13 R14 R15 R16 R19 R20 T16 U16 V11 Y19 Y20 AA19 AC8			+3.3V
VDDC	W11 Y11 Y12 Y13			+1.1V(DNU)
VCCQ	V16,W16,Y16			+1.8V

GND Signals				
VSS	R12,U11,L7,L8 M7,L11,L19, L20,M19,M20 N19,P19,AC20 AD20,AD19 AD8,AD7,T8 Y14,Y15,U19 P20,U20,V19 AC7,AB7,N8 A1,C1,E1,AK1 AM1			Ground
VSS	AP1,A3,C3 AM3,AP3,A5 AP5,G7,AH7 E8,AK8,D10 AL10,D12,AL12 D15,AL15,D17 AL17,E19,AK19 G20,AH20,A22 AP22,AC24,C24 AM24,AP24,A26 C26,E26,AK26 AM26,AP26			Ground
Other Signals				
DEVSLP	AC9	I	PU 69.8K & PD 75K	DEVICE SLEEP, High active.(Normal is Low)
NC	P8,R8,L15,L16,L17 L18,AA8,AA7 AB19,AB20 AB8,AC10 AC11,AC15 AC16,AC17 AC18,AC19 AD10,AD12 AD14,AD15 AD16,AD17 AD18,L10 M16,M17 M8,T19,T20 W19,W8,Y7 Y8,L13,L14 M14,M15, M18,N20,T11 V20,W20,AC12,R11	--	--	DNU

1. There is an internal Power On Reset at ball #M9 and power on sequence of internal POR is 22ms.

It's an optional function to choose whether POR (M9) is connected to an external capacitance or not.

6. SUPPORTED COMMANDS

6.1. ATA Command List

Op Code	Description	Op Code			Description
00h	NOP	C9h			Read DMA without Retry
06h	Data Set Management	CAh			Write DMA
10h-1Fh	Recalibrate	CBh			Write DMA without Retry
20h	Read Sectors	CEh			Write Multiple FUA EXT
21h	Read Sectors without Retry	E0h			Standby Immediate
24h	Read Sectors EXT	E1h			Idle Immediate
25h	Read DMA EXT	E2h			Standby
27h	Read Native Max Address EXT	E3h			Idle
29h	Read Multiple EXT	E4h			Read Buffer
2Fh	Read Log EXT	E5h			Check Power Mode
30h	Write Sectors	E6h			Sleep
31h	Write Sectors without Retry	E7h			Flush Cache
34h	Write Sectors EXT	E8h			Write Buffer
35h	Write DMA EXT	E9h			READ BUFFER DMA
37h	Set Native Max Address EXT	EAh			Flush Cache EXT
38h	CFA WRITE SECTORS WITHOUT ERASE	EBh			Write Buffer DMA
39h	Write Multiple EXT	ECh			Identify Device
3Dh	Write DMA FUA EXT	EFh			Set Features
3Fh	Write Long EXT	EFh	02h		Enable volatile write cache
40h	Read Verify Sectors	EFh	03h		Set transfer mode
41h	Read Verify Sectors without Retry	EFh	05h		Enable the APM feature set
42h	Read Verify Sectors EXT	EFh	10h		Enable use of SATA features et
44h	Zero EXT	EFh	10h	02h	Enable DMA Setup FIS Auto-Activate optimization
45h	WRITE UNCORRECTABLE EXT	EFh	10h	03h	Enable Device-initiated interface power state (DIPM) transitions
47h	READ LOG DMA EXT	EFh	10h	06h	Enable Software Settings Preservation (SSP)
57h	WRITE LOG DMA EXT	EFh	10h	07h	Enable Device Automatic Partial to Slumber transitions
60h	Read FPDMA Queued	EFh	10h	09h	Enable Device Sleep
61h	Write FPDMA Queued	EFh	55h		Disable read look-ahead
70h-7Fh	Seek	EFh	66h		Disable reverting to power-on defaults

90h		Execute Device Diagnostic	EFh	82h		Disable volatile write cache
91h		Initialize Device Parameters	EFh	85h		Disable the APM feature set
92h		Download Microcode	EFh	90h		Disable use of SATA feature set
93h		DOWNLOAD MICROCODE DMA	EFh	90h	02h	Disable DMA Setup FIS Auto-Activate optimization
B0h		SMART	EFh	90h	03h	Disable Device-initiated interface power state (DIPM) transitions
B0h	D0h	SMART READ DATA	EFh	90h	06h	Disable Software Settings Preservation (SSP)
B0h	D1h	SMART READ ATTRIBUTE THRESHOLDS	EFh	90h	07h	Disable Device Automatic Partial to Slumber transitions
B0h	D2h	SMART ENABLE/DISABILE ATTRIBUTE AUTOSAVE	EFh	90h	09h	Disable Device Sleep
B0h	D3h	SMART SAVE ATTRIBUTE VALUES	EFh	AAh		Enable read look-ahead
B0h	D4h	SMART EXECUTE OFF-LINE IMMEDIATE	EFh	CCh		Enable reverting to power-on defaults
B0h	D5h	SMART READ LOG	F1h			Security Set Password
B0h	D6h	SMART WRITE LOG	F2h			Security Unlock
B0h	D8h	SMART ENABLE OPERATIONS	F3h			Security Erase Prepare
B0h	D9h	SMART DISABLE OPERATIONS	F4h			Security Erase Unit
B0h	DAh	SMART RETURN STATUS	F5h			Security Freeze Lock
B0h	DBh	SMART ENABLE/DISABILE AUTOMATIC OFF-LINE	F6h			Security Disable Password
B1h		DEVICE CONFIGURATION	F8h			Read Native Max Address
B4h		Sanitize	F9h			Set Max Address
C4h		Read Multiple	F9h	01h		SET MAX SET PASSWORD
C5h		Write Multiple	F9h	02h		SET MAXLOCK
C6h		Set Multiple Mode	F9h	03h		SET MAX UNLOCK
C8h		Read DMA	F9h	04h		SET MAX FREEZE LOCIK

6.2. Identify Device Data

The following table detailsthe sector data returned by the IDENTIFY DEVICE command.

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
0	F	0040h	General configuration bit-significant information
1	X	***1**	Obsolete
2	F	C837h	Specific configuration
3	X	0010h	Obsolete
4-5	X	00000000h	Retired
6	X	003Fh	Obsolete
7-8	X	00000000h	Reserved for assignment by the Compact Flash Association
9	X	0000h	Retired
10-19	V	Varies	Serial number (20 ASCII characters)
20-21	X	00000000h	Retired
22	X	0000h	Obsolete
23-26	V	Varies	Firmware revision (8 ASCII characters)
27-46	V	Varies	Model number (xxxxxxxx)
47	F	8010h	7:0- Maximum number of sectors transferred per interrupt on MULTIPLE commands
48	F	4000h	Trusted Computing feature set options(not support)
49	F	2F00h	Capabilities
50	F	4000h	Capabilities
51-52	X	000000000h	Obsolete
53	F	0007h	Words 88 and 70:64 valid
54	X	***1**	Obsolete
55	X	0010h	Obsolete
56	X	003Fh	Obsolete
57-58	X	***2**	Obsolete
59	F	5D10h	Sanitize and Number of sectors transferred per interrupt on MULTIPLE commands
60-61	V	***3**	Maximum number of sector (28bit LBA mode)
62	X	0000h	Obsolete

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
63	F	0407h	Multi-word DMA modes supported/selected
64	F	0003h	PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Manufacturer's recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	1D00h	Additional Supported (support download microcode DMA)
70	X	0000h	Reserved
71-74	X	0000000000000000h	Reserved for the IDENTIFY PACKET DEVICE command
75	F	001Fh	Queue depth
76	F	E70Eh	Serial SATA capabilities
77	F	0006h	Serial ATA Additional Capabilities
78	F	0044h	Serial ATA features supported
79	F	0040h	Serial ATA features enabled
80	F	0FF8h	Major Version Number
81	F	0000h	Minor Version Number
82	F	746Bh	Command set supported
83	F	7D09h	Command set supported
84	F	4163h	Command set/feature supported extension
85	F	746Bh	Command set/feature enabled
86	F	BC01h	Command set/feature enabled
87	F	6163h	Command set/feature default
88	F	007Fh	Ultra DMA Modes
89	F	0003h	Time required for security erase unit completion
90	F	001Eh	Time required for Enhanced security erase completion
91	F	0000h	Current advanced power management value
92	F	FFFEh	Master Password Revision Code
93	F	0000h	Hardware reset result. For SATA devices, word 93 shall be set to the value 0000h.

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
94	X	0000h	Obsolete
95	F	0000h	Stream Minimum Request Size
96	F	0000h	Streaming Transfer Time – DMA
97	F	0000h	Streaming Access Latency – DMA and PIO
98-99	F	0000h	Streaming Performance Granularity
100-103	V	***4**	Maximum user LBA for 48 bit Address feature set
104	F	0000h	Streaming Transfer Time – PIO
105	F	0008h	Maximum number of 512-byte blocks per DATA SET MANAGEMENT command
106	F	4000h	Physical sector size/Logical sector size
107	F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	V	Varies	World Wide Name
112-115	X	000000000000 0000h	Reserved
116	X	0000h	Reserved
117-118	F	00000000h	Words per logical Sector
119	F	401Ch	Supported settings
120	F	401Ch	Command set/Feature Enabled/Supported
121-126	X	0h	Reserved
127	X	0000h	Obsolete
128	F	0021h	Security status
129-140	V	Varies	Vendor specific
141	V	Varies	Vendor specific
142-159	V	Varies	Vendor specific
160	X	000h	Reserved for CFA
161-167	X	0h	Reserved for CFA
168	V	Varies	Device Nominal Form Factor
169	F	0001h	DATA SET MANAGEMENT command is supported
170-173	F	000000000000 0000h	Additional Product Identifier
174-175	X	00000000h	Reserved
176-205	F	0h	Current media serial number

Word	F: Fixed V: Variable X: retired/obsolete /reserved	Default Value	Description
206	F	000h	SCT Command Transport
207-208	X	00000000h	Reserved
209	F	4000h	Alignment of logical blocks within a physical block
210-211	F	00000000h	Write-Read-Verify Sector Count Mode 3 (not support)
212-213	F	00000000h	Write-Read-Verify Sector Count Mode 2 (not support)
214-216	X	0h	Obsolete
217	F	0001h	Non-rotating media device
218	X	000h	Reserved
219	X	0000h	NV Cache relate (not support)
220	V	0000h	Write read verify feature set current mode
221	X	0000h	Reserved
222	F	10FFh	Transport major version number
223	F	0000h	Transport minor version number
224-229	X	0h	Reserved
230-233	F	000000000000 0000h	Extend number of user addressable sectors
234	F	0001h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	F	FFFEh	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	X	0h	Reserved
255	F	XXA5h XX is variable	Integrity word (Checksum and Signature)

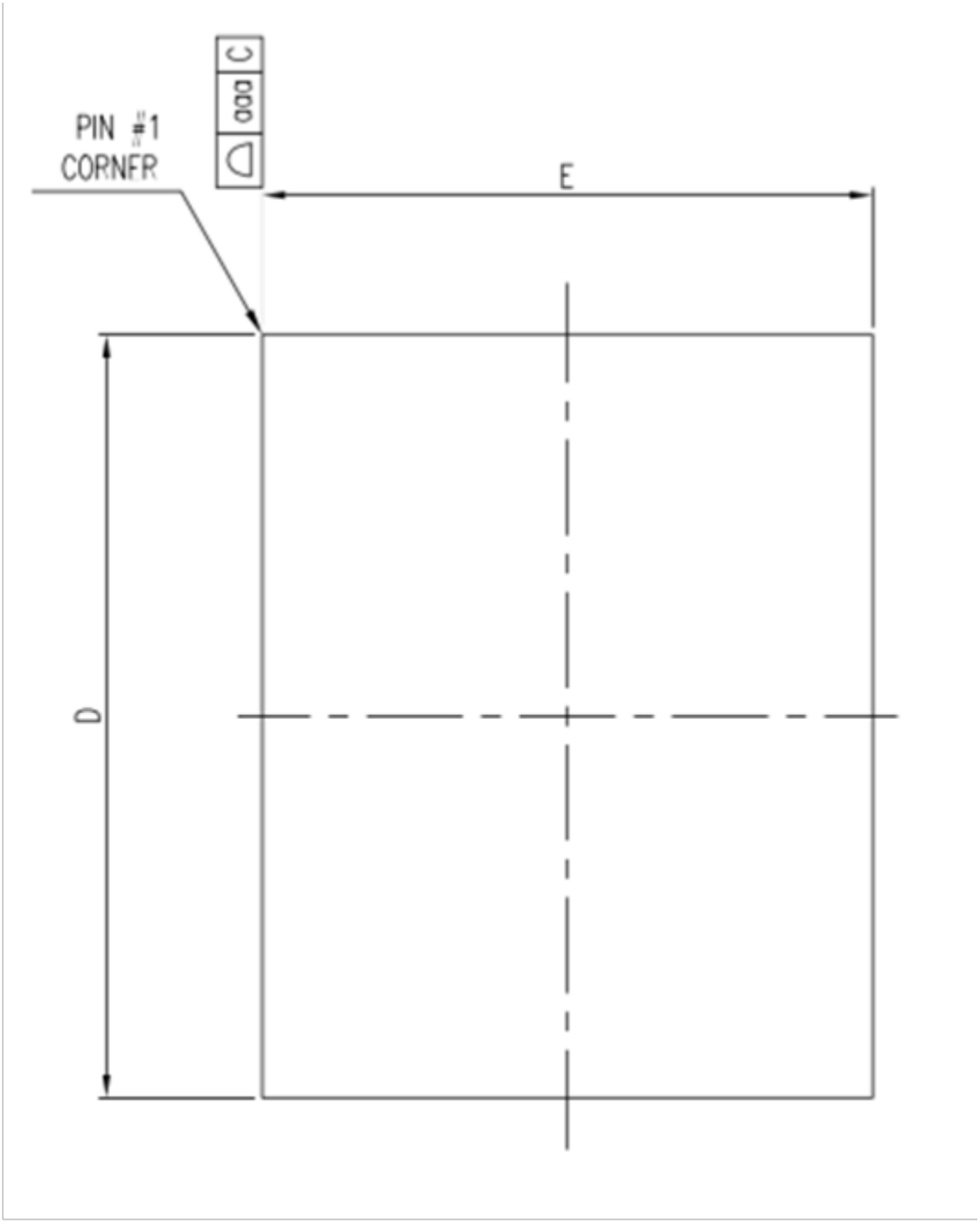
List of Device Identification for Each Capacity

Capacity (GB)	*1 (Word 1/Word 54)	*2 (Word 57 – 58)	*3 (Word 60 – 61)	*4 (Word 100 – 103)
8	3CA5h	EEC9B0h	EEC9B0h	EEC9B0h
16	3FFFh	FBFC10h	1DD40B0h	1DD40B0h
32	3FFFh	FBFC10h	3BA2EB0h	3BA2EB0h
64	3FFFh	FBFC10h	7740AB0h	7740AB0h
128	3FFFh	FBFC10h	EE7C2B0h	EE7C2B0h

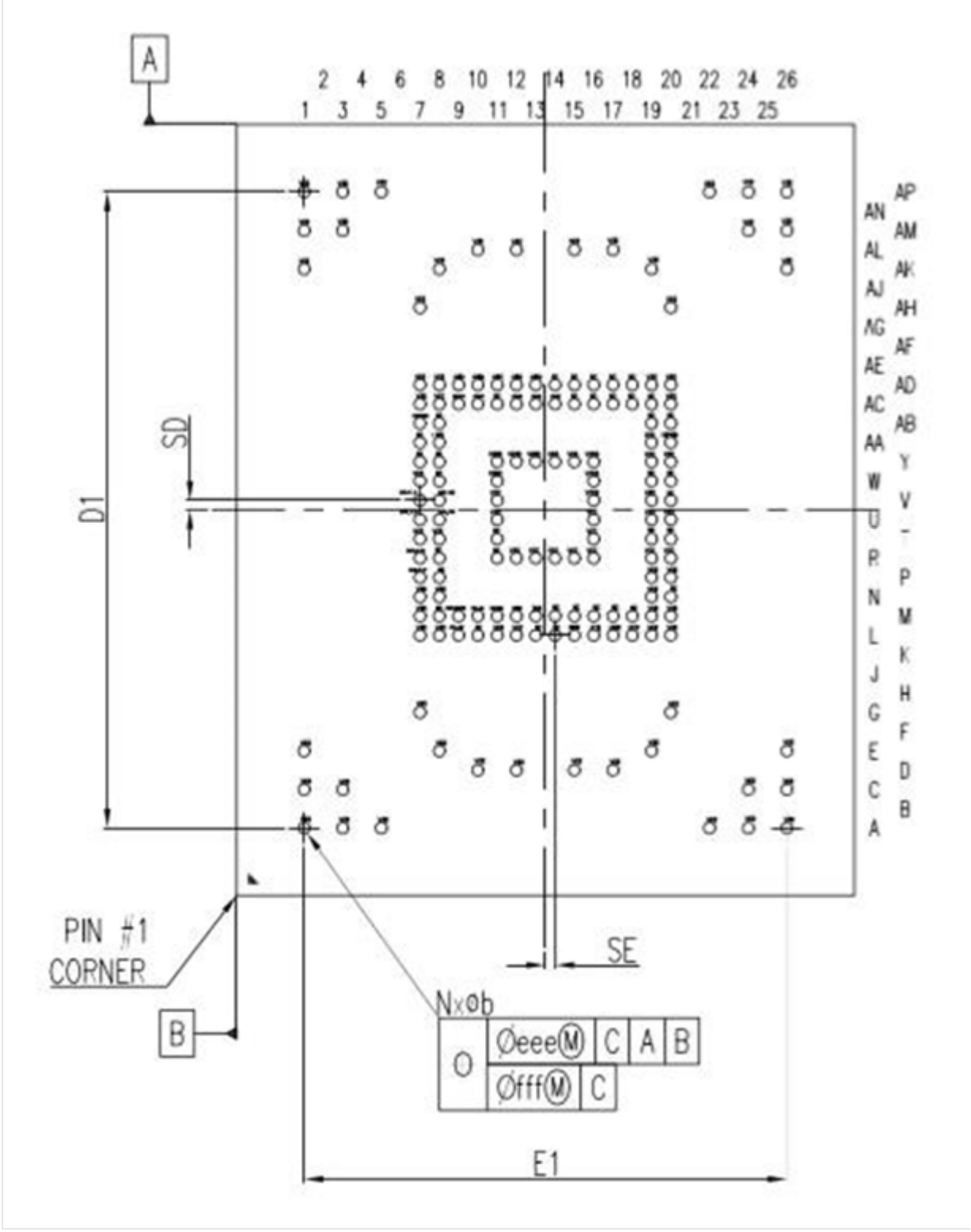
7. PHYSICAL DIMENSION

Dimension: 16mm(L) x 20mm(W)

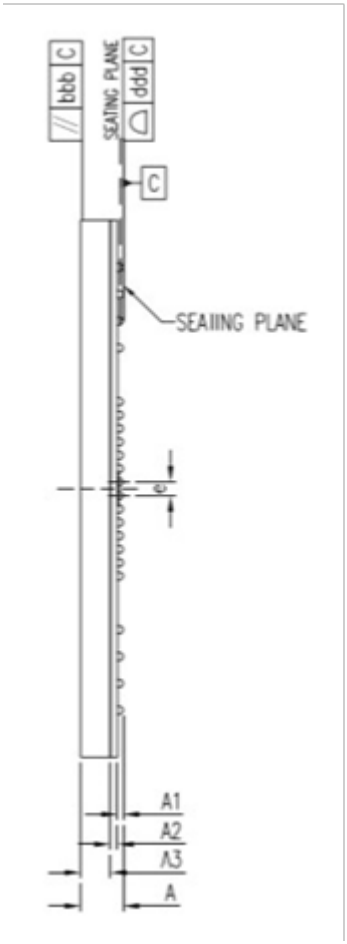
Bottom View



Bottom View


A
2 4 6 8 10 12 14 16 18 20 22 24 26
1 3 5 7 9 11 13 15 17 19 21 23 25
AP AN AM AL AK AJ AH AG AF AE AD AC AB AA Y W V U T R P N M L K J H G F E D C B A
SD
D1
PIN #1
CORNER
B
SE
Nxøb
Øeee M C A B
Øfff M C
E1

Side View



	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	1.45	1.57	1.70
STAND OFF	A1	0.16	0.21	0.26
SUBSTRATE THICKNESS	A2		0.26	
MOLD THICKNESS	A3		1.10	
BODY SIZE	D		20	
	F		16	
BALL DIAMETER			0.30	
BALL OPENING			0.275	
BALL WIDTH	b	0.25	0.30	0.35
BALL PITCH	e		0.50	
BALL COUNT	n		156	
EDGE BALL CENTER TO CENTER	D1		16.50 BSC.	
	E1		12.50 BSC.	
BODY CENTER TO CONTACT BALL	SD		0.25 BSC.	
	SE		0.25 BSC.	
JEDEC(REF)			MO-276(REF.)	
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.20	
COPLANARITY	ddd		0.08	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.05	

8. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Term	Definitions
ATTO	Commercial performance benchmark application
DEVSLP	Device sleep mode
DIPM	Device initiated power management
HIPM	Host initiated power management
LBA	Logical block addressing
MB	Mega-byte
MTBF	Mean time between failures
NCQ	Native command queue
SATA	Serial advanced technology attachment
SDR	Synchronous dynamic access memory
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk

9. ORDERING INFORMATION

Part Number	Capacity	Dimension	BGA	Flash Mode	Grade
HDA28G22211I	8GB	16x20x1.7mm	156 Ball	1-CH	Industrial (-40°C~ 85°)
HDA2AG22211I	16GB			1-CH/2-CH	Industrial (-40°C~ 85°)
HDA2BG22211I	32GB			2-CH	Industrial (-40°C~ 85°)
HDA2CG22211I	64GB			2-CH	Industrial (-40°C~ 85°)
HDA2DG22211I	128GB			2-CH	Industrial (-40°C~ 85°)