4G-Bit 3.3V NAND FLASH MEMORY

Descriptions

Offered in 512Mx8bit, the H7A14G21A1CX is a 4G-bit NAND Flash Memory with spare 128M-bit. The device is offered in 3.3V VCC. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 400us on the (2K+64)Byte page and an erase operation can be performed in typical 4.5ms on a (128K+4K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The H7A14G21A1CX is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable app. lications requiring non-volatility..

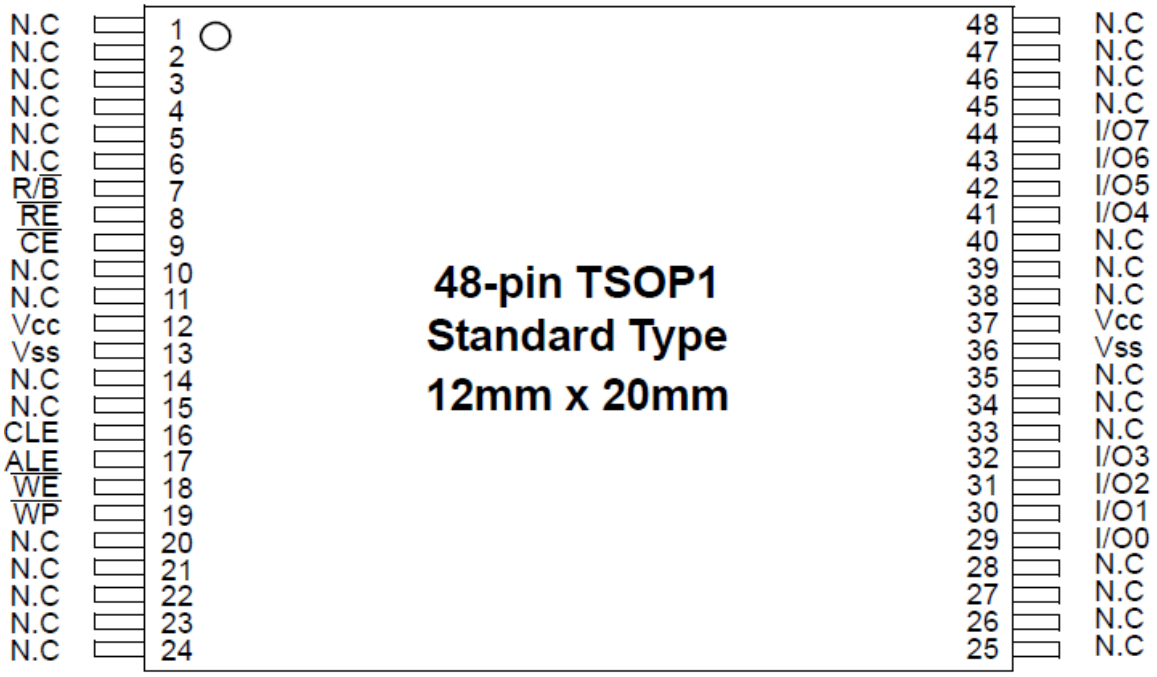
Features

- **Basic Features**
  - Density : 4Gbit
  - Vcc : 3.3V(2.7V to 3.6V)
  - Bus width : x8
  - Operating temperature
    Commercial: 0˚C to 70˚C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - Memory Cell Array : (512M + 16M) x 8bit
  - Page size : 2,112 Bytes (2048 + 64 Bytes)
  - Data Register : (2K + 64) x 8bit
  - Block Size :(128K + 4K Byte)
- **Automatic Program and Erase**
  - Page Program :(2K + 64) Byte
  - Block Erase :(128K + 4K Byte)
- **Page Read Operation**
  - Random Read : 25us(Max.)
  - Serial Access : 25ns(Min.)
  - Data Transfer Rate : SDR 20Mhz(40Mbps)
- **Fast Write Cycle Time**
  - Page Program time : 400us(Typ.)
  - Block Erase Time : 4.5ms(Typ.)
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
  - Program/Erase Lockout During Power Transitions
- **Command Driven Operation**
- **Unique ID for Copyright Protection**
- **Package:**
  - 48 - Pin TSOP1 (12 x 20/0.5 mm pitch)
  - Pb-Free, Halogen-Free Package

Ordering Information

Part No	Density	Organization	Package	Grade
H7A14G21A1CX	4G-bit/512M-byte	X8	48-Pin TSOP1 12x20mm	Commercial

Pin Assignment



48-pin TSOP1

Pin Description (Simplified)

48-pin TSOP1,12x20mm		
Pin Name	**I/O**	**Function**
#WP	Input	Write Protect
ALE	Input	Address Latch Enable
#CE	Input	Chip Enable
#WE	Input	Write Enable
RY#BY	Output	Ready/Busy Output
#RE	Input	Read Enable
CLE	Input	Command Latch Enable
I/O[0-7]	Input / Output	Data Input / Output (x8)
V_{cc}	Supply	Device Power Supply
V_{SS}	Supply	Ground
N.C	-	Not Connect

Note: Connect all VCC and VSS pins of each device to common power supply outputs.

Absolute Maximum Rating

Item	Symbol	Rating	Unit
Voltage on any pin relative to VSS	V_{cc}	-0.6 ~ 4.6	V
	V_{in}	-0.6 ~ 4.6	V
	$V_{I/O}$	-0.6 to Vcc +0.3 (< 4.6V)	V
Storage Temperature	T_{STG}	-65 ~ 150	˚C
Temperature Under Bias	T_{BIAS}	-10 ~125	˚C
Short circuit output current	I_{os}	5	mA

Note 1: Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.

Note 2: Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

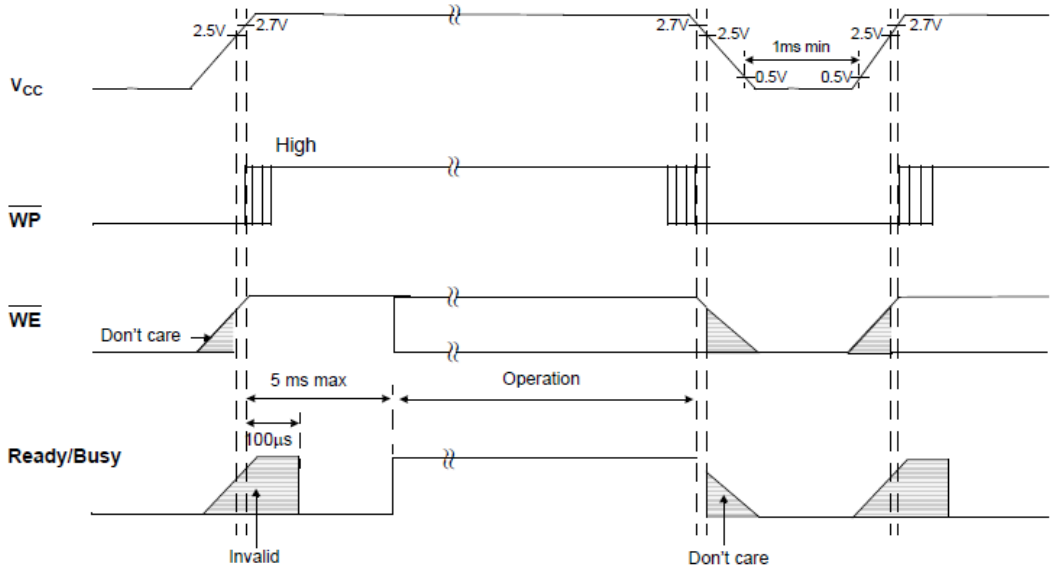
Note 3: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Ranges

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	Vcc	2.7	3.3	3.6	V
Ground Supply Voltage	Vss	0	0	0	V
Ambient Temperature, Operating	Ta	0	-	70	˚C

Device Power-up Timing

The device is designed to offer protection from any involuntary program/erase during power-transitions.
An internal voltage detector disables all functions whenever VCC is below about 2V(3.3V device).
#WP pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down.
A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences as shown below. The two step command sequence for program/erase provides additional software protection.



AC Waveforms for Power Transition

DC Characteristics

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	

Page Read Access Operation Current	Icc1	tRC= 50ns
		#CE=VIL
		IOUT=0mA
			-	15	30	mA

Program current	Icc2	-	-	15	30	mA
Erase current	Icc3	-	-	15	30	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	70	uA
Input leakage current	ILI	VIN= 0V to Vcc(max)	-	-	+/-10	uA
Output leakage current	ILO	VOUT=0V to Vcc(max)	-	-	+/-10	uA
Input high voltage(1)	VIH	-	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage(1)	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage	VOH	IOH=-400µA	2.4	-	-	V
Output low voltage	VOL	IOL=2.1mA	-	-	0.4	V
Output low current	IOL(RY/#BY)	VOL=0.4V	8	10	-	mA

Note 1: VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20ns or less.

Note 2: Typical value is measured at VCC=3.3V, TA=25°C. Not 100% tested..

AC Measurement Conditions

Parameter	Symbol	Spec.		Unit
		MIN	Max	
Input Capacitance(1), (2)	CIN	-	8	pF
Input/Output Capacitance(1), (2)	CIO	-	8	pF
Input Rise and Fall Times	-	-	5	ns
Input Pulse Level	-	0 to VCC		V
Input/Output timing Level	-	Vcc/2		V
Output load	-	1TTL GATE and CL=50pF		-

Note 1: Capacitance is periodically sampled and not 100% tested.

Note 2: Test conditions TA=25'C, f=1MHz, VIL/VIN=0V

Read / Program / Erase Characteristics

Parameter	Symbol	Spec.			Unit
		MIN	Typ.	MAX	
Data Transfer from Cell to Register	tR	-		25	us
Program Time	tPROG	-	400	900	us
Dummy Busy Time for Two-Plane Page Program	tDBSY	-	0.5	1	us
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	tBEARS	-	4.5	16	ms

Note: 1. Typical value is measured at VCC=3.3V, TA=25'C. Not 100% tested.

Note: 2. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V VCC and 25'C temperature.

AC Timing Parameters Table

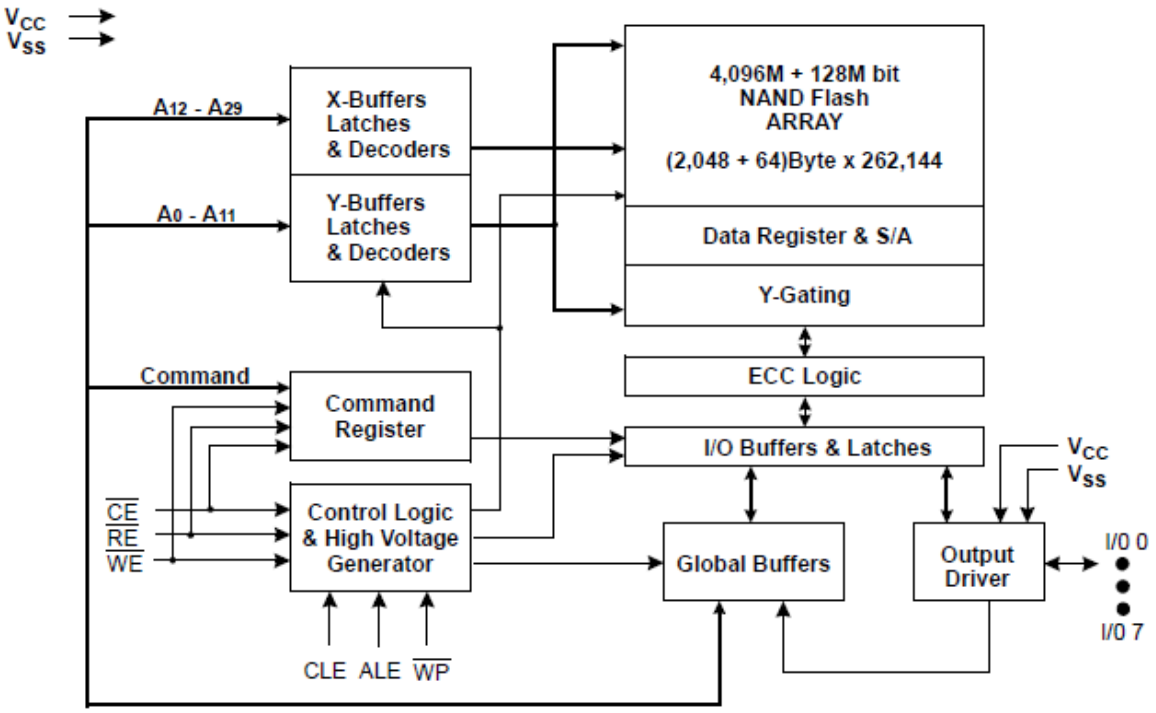
Parameter	Symbol	Spec.		Unit
		MIN	MAX	
CLE Setup Time(1)	tCLS	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE Setup Time(1)	tCS	20	-	ns
CE Hold Time	tCH	5	-	ns
WE Pulse Width	tWP	12	-	ns
ALE Setup Time(1)	tALS	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time(1)	tDS	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE High Hold Time	tWH	10	-	ns
Address to Data Loading Time(2)	tADL	70	-	ns
ALE to RE Delay	tAR	10	-	ns
CLE to RE Delay	tCLR	10	-	ns
Ready to RE Low	tRR	20	-	ns
RE Pulse Width	tRP	12	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	25	-	ns
RE Access Time	tREA	-	20	ns
CE Access Time	tCEA	-	25	ns
RE High to Output Hi-Z	tRHZ	-	100	ns
CE High to Output Hi-Z	tCHZ	-	30	ns
CE High to ALE or CLE Don't Care	tCSD	0	-	ns
RE High to Output Hold	tRHOH	15	-	ns
RE Low to Output Hold	tRLOH	5	-	ns
Data Hold Time after CE Disable	tCOH	15	-	ns
RE High Hold Time	tREH	10	-	ns
Output Hi-Z to RE Low	tIR	0	-	ns
RE High to WE Low	tRHW	100	-	ns
WE High to RE Low	tWHR	60	-	ns
Device Resetting Time (Read/Program/Erase)(3)	tRST	-	5/10/500	us

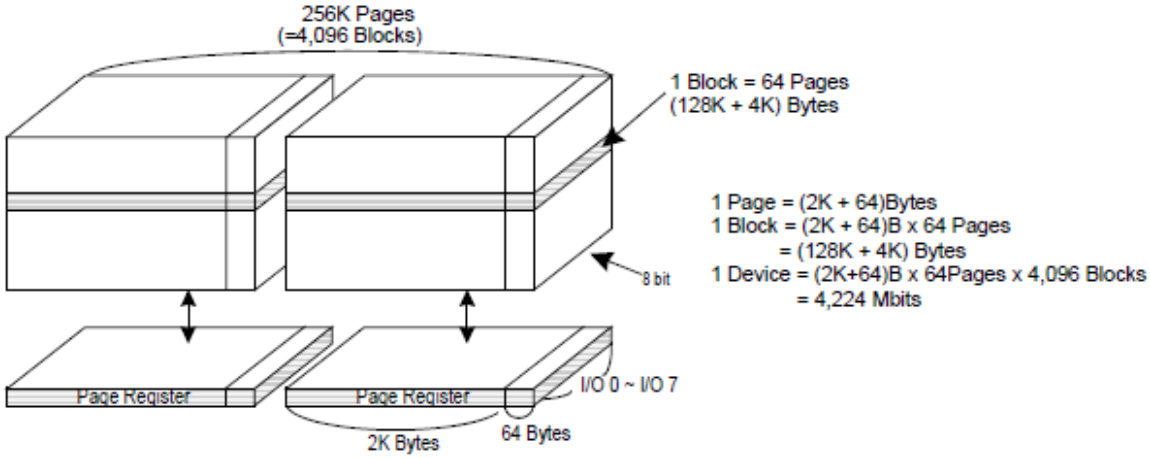
Note 1: The transition of the corresponding control pins must occur only once while #WE is held low.

Note 2: tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.

Note 3: If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

Block Diagram and Array Organization





	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle	A28	A29	**A30	*L	*L	*L	*L	*L

Note : * L must be set to "Low".

* The device ignores any additional input of address cycles than required.

**A30 is used for DDP with a single #CE.

**A30 must be set to "Low" for SDP.

Mode Selection Table

Mode		CLE	ALE	#CE	#WE	#RE	#WP
Read Mode	Command input	H	L	L	⎍	H	X
	Address input(5 cycles)	L	H	L	⎍	H	X
Write Mode	Command input	H	L	L	⎍	H	H
	Address input(5 cycles)	L	H	L	⎍	H	H
Data input		L	L	L	⎍	H	H
Data output		L	L	L	H	⎍	X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X*	X	X	X	L
Standby		X	X	H	X	X	0V/ Vcc

Note 1: X* can be VIL or VIH.

Note 2: #WP should be biased to CMOS HIGH or LOW for standby.

Command Table

Command	1st Cycle	2nd Cycle	Acceptable during busy
PAGE READ	00h	30h	
READ for COPY BACK	00h	35h	
READ ID	90h	-	
RESET	FFh	-	Yes
PAGE PROGRAM	80h	10h	
Two-Plane Page Program(2)	80h---11h	81h---10h	
PROGRAM for COPY BACK	85h	10h	
Two-Plane Copy-Back Program(2)	80h---11h	81h---10h	
BLOCK ERASE	60h	D0h	
Two-Plane Block Erase	60h---60h	D0h	
RANDOM DATA INPUT(1)	85h	-	
RANDOM DATA OUTPUT(1)	05h	E0h	
READ STATUS	70h	-	Yes
ECC READ STATUS	7Ah		

Note 1: RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.

Note 2: Any command between 11h and 81h is prohibited except 70h and FFh.

Invalid Block Management

The H7A14G21A1CX may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.

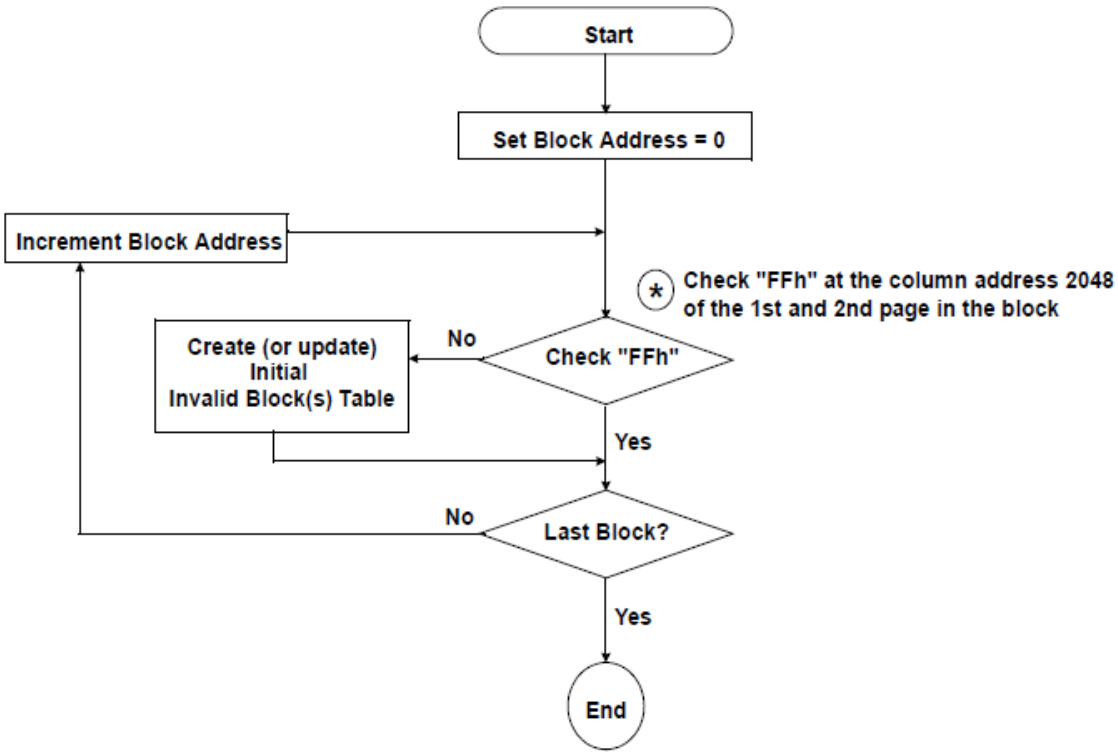
Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	4016	4096	blocks

Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Axeme. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.

Identifying Initial Invalid Blocks

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Axeme makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Below). Any intentional erasure of the original initial invalid block information is prohibited.

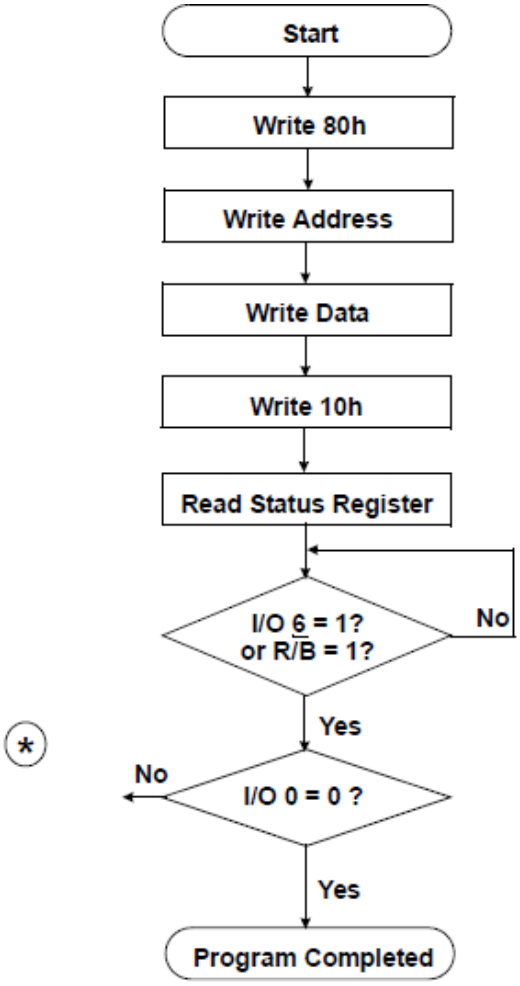


flow chart to create initial invalid block table

Error in operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

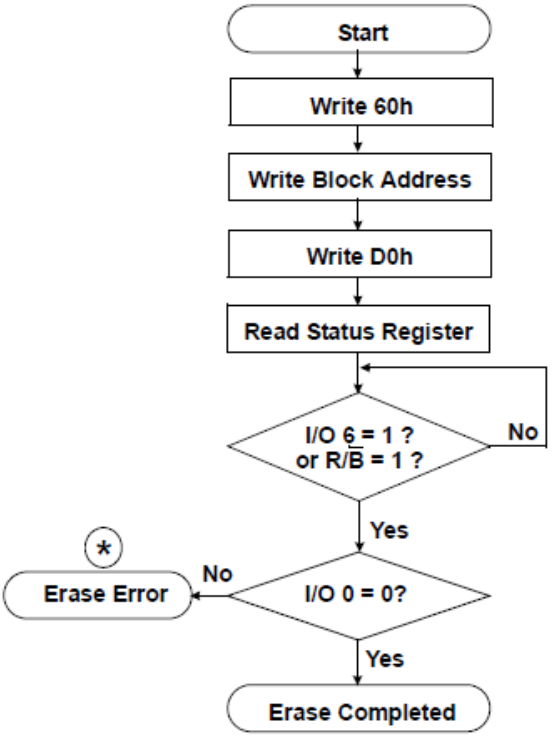
Failure Mode		Detection and countermeasure procedure
Write	Erase Failure	Status read after erase → Block Replacement
	Program Failure	Status read after program → Block Replacement
Read	Single bit Failure	Verify ECC → ECC correction



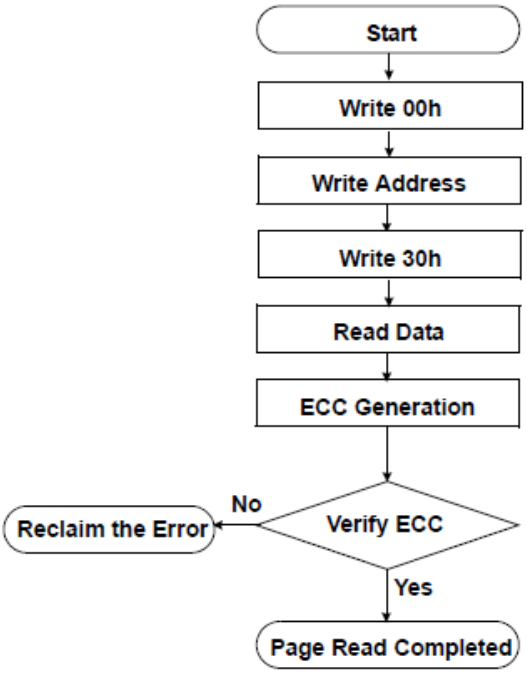
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Program Flow Chart

Erase Flow Chart

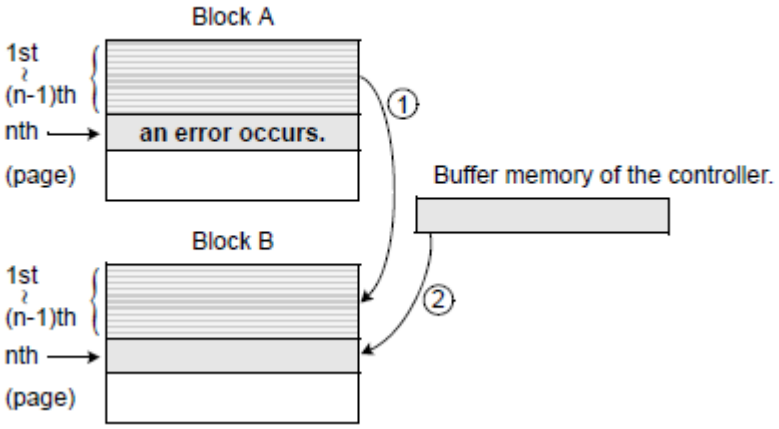


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



Step 1: When an error happens in the nth page of the Block 'A' during erase or program operation.

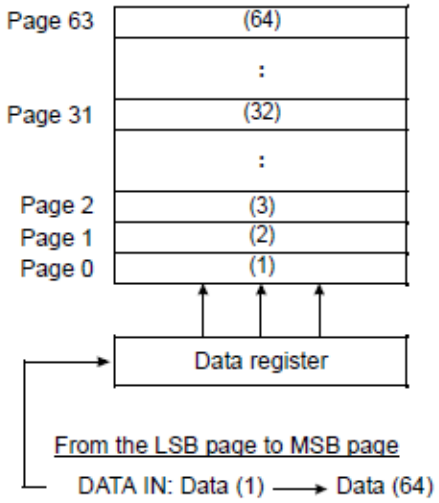
Step 2: Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')

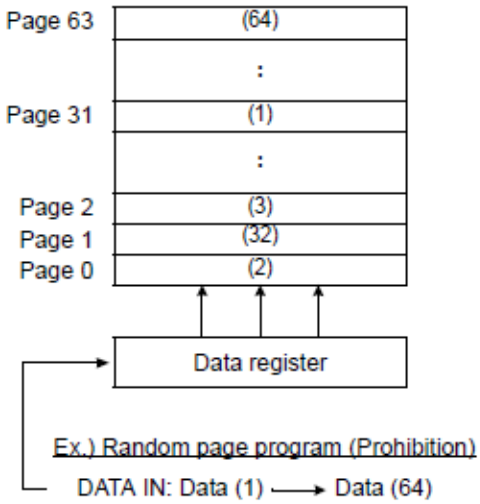
Step 3: Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.

Step 4: Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing in program operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.

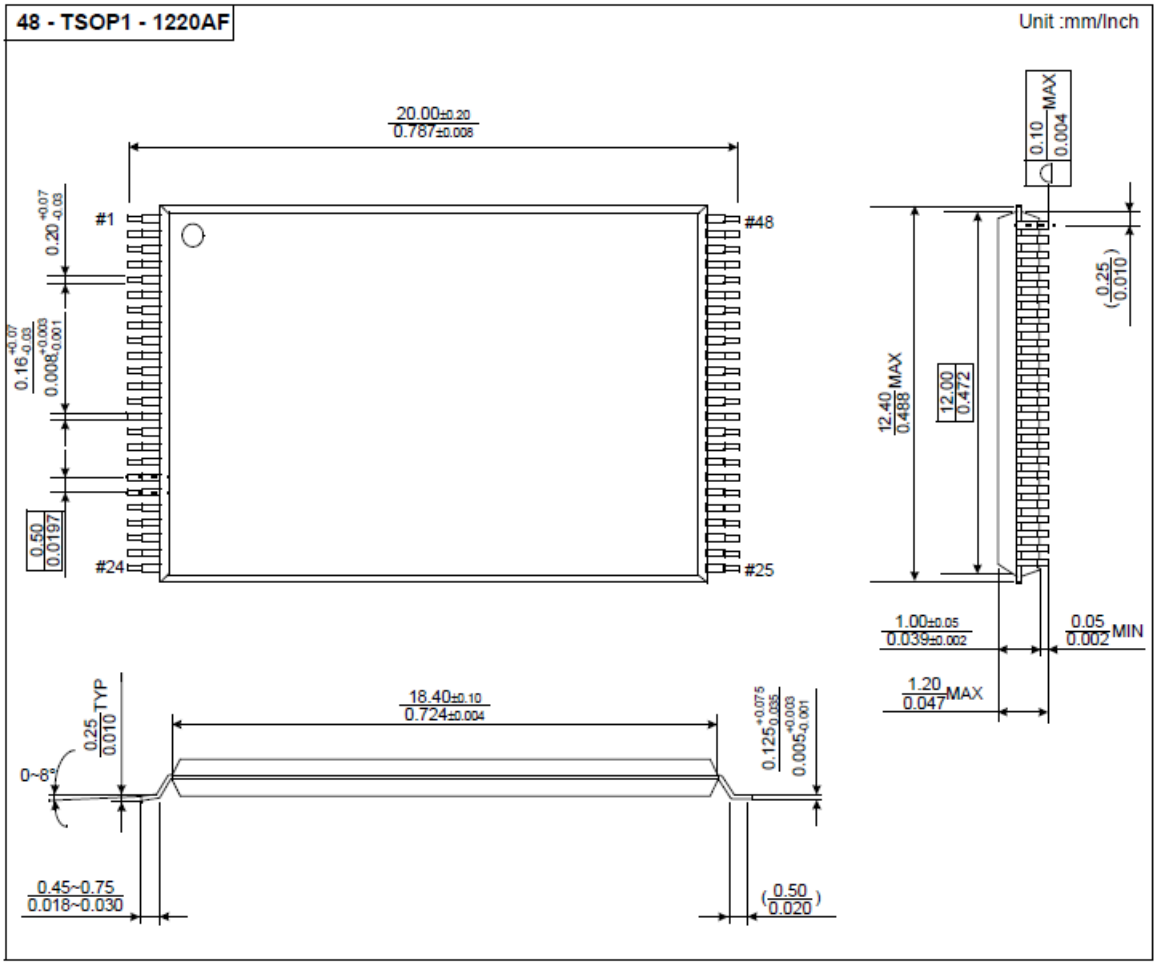




DQ	DATA	ADDRESS				
DQx	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
DQ 0 ~ DQ 7	2112 Byte	A0 ~ A7	A8 ~ A11	A12 ~ A19	A20 ~ A27	A28 ~ A29

Package Description

TSOP 48-pin 12x20



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2017	Maven Hsu	N/A
1.0	First SPEC. Release.	Aug. 2017	Maven Hsu	N/A