4G-Bit 3.3V NAND FLASH MEMORY

Descriptions

The H7A14G21B1CN (4G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as,voice, video, text and photos. The device operates on a single 2.7V to 3.6V power supply with active current consumption as low as 25mA at 3V and 10uA for CMOS standby current.

The memory array totals 553,648,128 bytes, and organized into 4,096 erasable blocks of 135,168 bytes. Each block consists of 64 programmable pages of 2,112-bytes each. Each page consists of 2,048-bytes for the main data storage area and 64-bytes for the spare data area (The spare area is typically used for error management functions). The H7A14G21B1CN supports the standard NAND flash memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions.

The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

Features

- **Basic Features**
  - Density : 4Gbit (Single chip solution)
  - Vcc : 2.7V to 3.6V
  - Bus width : x8
  - Operating temperature
    Commercial: 0˚C to 70˚C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - Density: 4G-bit/512M-byte
  - Page size
    2,112 bytes (2048 + 64 bytes)
  - Block size
    64 pages (128K + 4K bytes)
- **Highest Performance**

– Read performance (Max.)
  - Random read: 25us
  - Sequential read cycle: 25ns

– Write Erase performance
  - Page program time: 250us(typ.)
  - Block erase time: 2ms(typ.)

– Endurance 100,000 Erase/Program Cycles
– 10-years data retention

- **Command set**

– Standard NAND command set
– Additional command support
  - Sequential / Random Cache Read
  - Cache Program
  - Copy Back
  - Two-plane operation

– OTP feature
– Block Lock feature

- **Lowest power consumption**

– Read: 25mA(typ.3V)
– Program/Erase: 25mA(typ.3V)
– CMOS standby: 10uA(typ.)

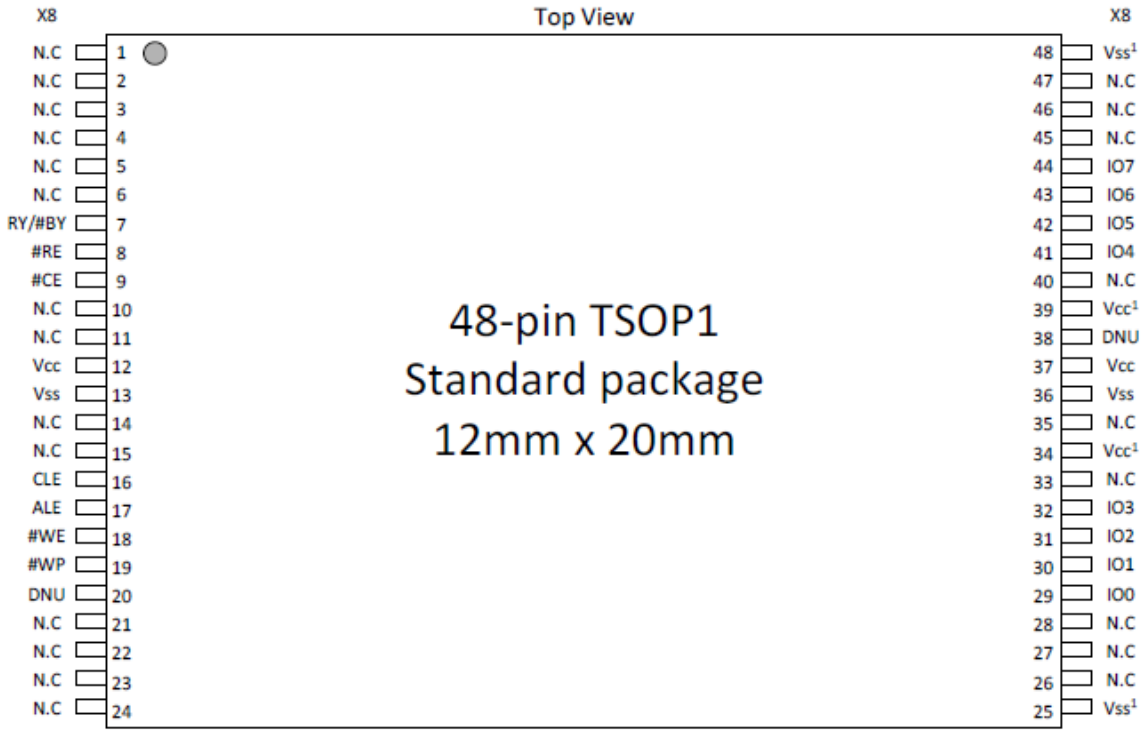
- **Space Efficient Packaging**

– 48-pin standard TSOP1

Ordering Information

Part No	Density	Organization	Package	Grade
H7A14G21B1CN	4G-bit/512M-byte	X8	48-Pin TSOP1 12x20mm	Commercial

Pin Assignment



48-pin TSOP1

Pin Description (Simplified)

48-pin TSOP1,12x20mm		
Pin Name	**I/O**	**Function**
#WP	Input	Write Protect
ALE	Input	Address Latch Enable
#CE	Input	Chip Enable
#WE	Input	Write Enable
RY#BY	Output	Ready/Busy
#RE	Input	Read Enable
CLE	Input	Command Latch Enable
I/O[0-7]	Input / Output	Data Input / Output (x8)
V_{cc}	Supply	Power Supply
V_{SS}	Supply	Ground
DNU	-	Do Not Use:
N.C	-	Not Connect

Note1: Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.

Absolute Maximum Rating(3.3V)

Item	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{cc}		-0.6 ~ 4.6	V
Voltage Applied to Any Pin	V_{in}	Relative to Ground	-0.6 ~ 4.6	V
Storage Temperature	T_{STG}		-65 ~ 150	˚C
Short circuit output current	I_{os}		5	mA

Note 1: Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.

Note 2: Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

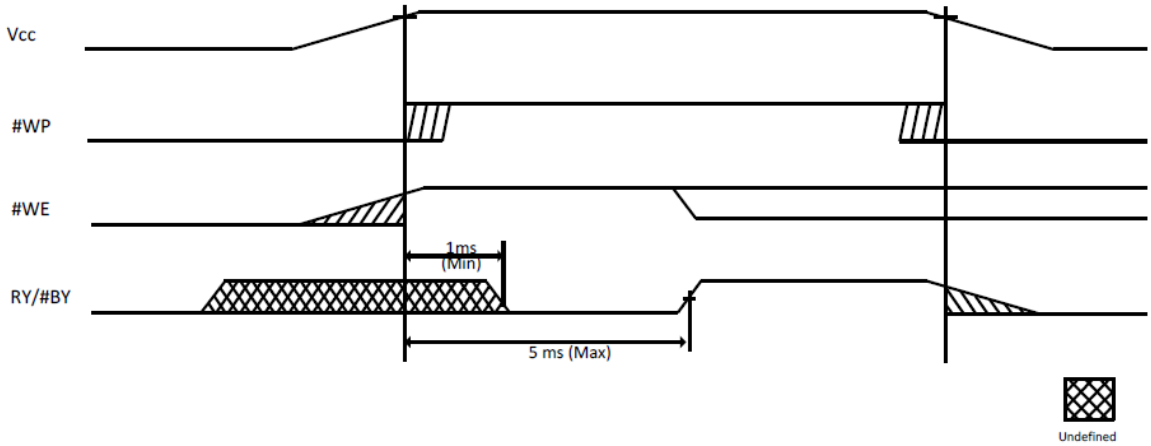
Note 3: This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

Operating Ranges(3.3V)

Parameter	Symbol	Conditions	Spec.		Unit
			Min.	Max.	
Supply Voltage	Vcc		2.7	3.6	V
Ambient Temperature, Operating	Ta	Commercial	0	70	˚C

Device Power-up Timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, an internal voltage detector disables all functions whenever Vcc is below about 2V at 3V device. Write Protect (#WP) pin provides hardware protection and is recommended to be kept at VIL during power up and power down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences (See Below Figure).



Power ON/OFF sequence

DC Characteristics(3.3V)

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	

Sequential Read current	Icc1	tRC= tRC MIN
		#CE=VIL
		IOUT=0mA
			-	25	35	mA

Program current	Icc2	-	-	25	35	mA
Erase current	Icc3	-	-	25	35	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	50	uA
Input leakage current	ILI	VIN= 0 V to Vcc	-	-	+/-10	uA
Output leakage current	ILO	VOUT=0V to Vcc	-	-	+/-10	uA
Input high voltage	VIH	I/O7~0, #CE,#WE,#RE, #WP,CLE,ALE	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	VOH	IOH=-400μA	2.4	-	-	V
Output low voltage(1)	VOL	IOL=2.1mA	-	-	0.4	V
Output low current	IOL(RY/#BY)	VOL=0.4V	8	10	-	mA

Note 1: VOH and VOL may need to be relaxed if I/O drive strength is not set to full.

Note 2: IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full.

AC Measurement Conditions(3.3V)

Parameter	Symbol	Spec.		Unit
		MIN	Max	
Input Capacitance(1), (2)	CIN	-	10	pF
Input/Output Capacitance(1), (2)	CIO	-	10	pF
Input Rise and Fall Times	TR/TF	-	5	ns
Input Pulse Voltages	-	0 to VCC		V
Input/Output timing Voltage	-	Vcc/2		V
Output load (1)	CL	1TTL GATE and CL=30pF		-

Note 1: Verified on device characterization , not 100% tested

Note 2: Test conditions TA=25'C, f=1MHz, VIN=0V

AC timing characteristics for Command, Address and Data Input(3.3V)

Parameter	Symbol	Spec.		Unit
		MIN	MAX	
ALE to Data Loading Time	tADL	70	-	ns
ALE Hold Time	tALH	5	-	ns
ALE setup Time	tALS	10	-	ns
#CE Hold Time	tCH	5	-	ns
CLE Hold Time	tCLH	5	-	ns
CLE setup Time	tCLS	10	-	ns
#CE setup Time	tCS	15	-	ns
Data Hold Time	tDH	5	-	ns
Data setup Time	tDS	10	-	ns
Write Cycle Time	tWC	25	-	ns
#WE High Hold Time	tWH	10	-	ns
#WE Pulse Width	tWP	12	-	ns
#WP setup Time	tWW	100	-	ns

Note: 1. tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.

AC timing characteristics for Operation(3.3V)

Parameter	Symbol	Spec.		Unit
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	25	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	30	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Cache Busy in Cache Read mode	tRCBSY	-	25	us
Output High-Z to #RE LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	us
READ Cycle Time	tRC	25	-	ns
#RE Access Time	tREA	-	20	ns
#RE HIGH Hold Time	tREH	10	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	100	ns
#RE LOW to output hold	tRLOH	5	-	ns
#RE Pulse Width	tRP	12	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	us
#WE HIGH to Busy(3)	tWB	-	100	ns
#WE HIGH to #RE LOW	WHR	60	-	ns

Note 1: Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested

Note 2: Do not issue new command during tWB, even if RY/#BY is ready.

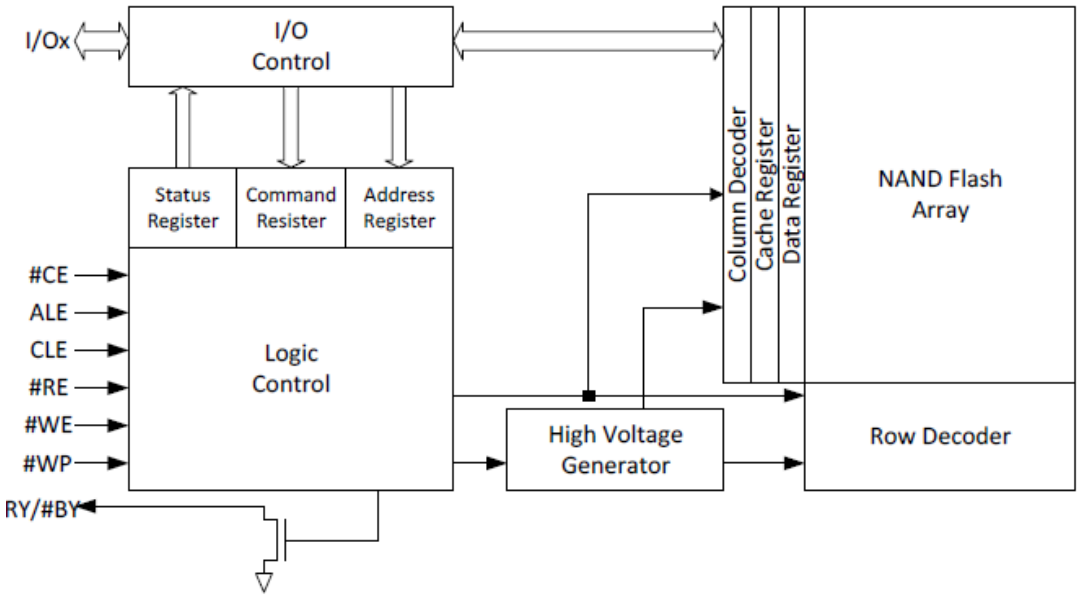
Program and Erase Characteristics

Parameter	Symbol	Spec.		Unit
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	250	700	us
Busy Time for Cache program (1)	tCBSY	3	700	us
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	us
Busy Time for program/erase at locked block	tLBSY	-	3	us
Busy Time for OTP program when OTP is protected	tOBSY	-	30	us
Block Erase Time	tBERS	2	10	ms
Last Page Program time (2)	tLPROG	-	-	-
Busy Time for Two Plane page program and Two Plane Block Erase	tDBSY	0.5	1	us

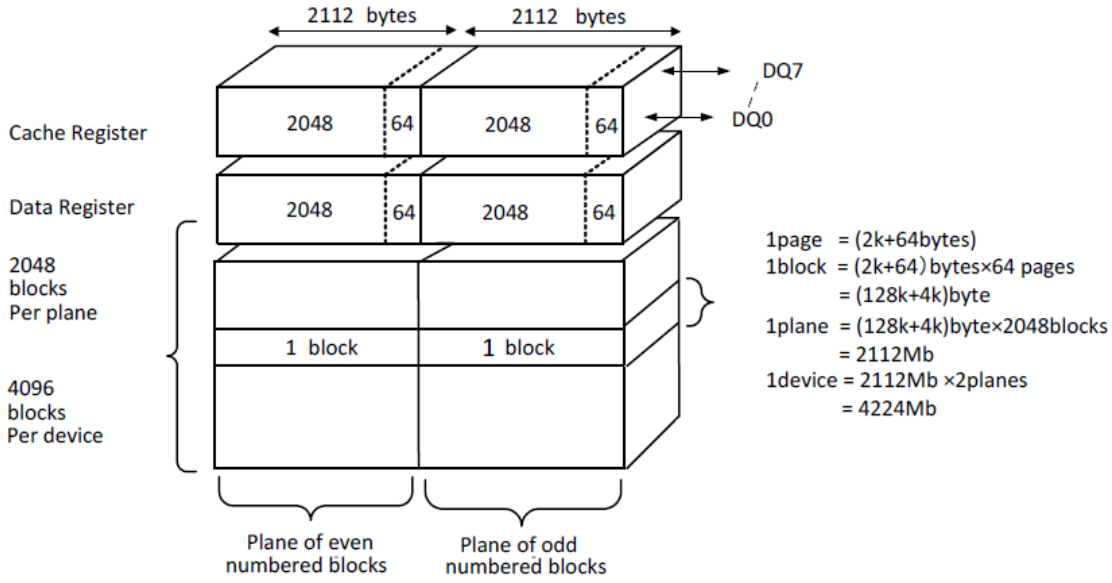
Note: 1. tCBSY maximum time depends on timing between internal program complete and data-in.

Note: 2. tLPROG = Last tPROG + Last -1 tPROG – Last page Address, Command and Data load time.

Block Diagram



Memory Array Organization



	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	A11	A10	A9	A8
3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
5th cycle	L	L	L	L	L	L	A29	A28

Note: 1. "L" indicates a low condition, which must be held during the address cycle to insure correct processing.

Note: 2. A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A29 during the 3rd to 5th cycles are row addresses.

Note: 3. A18 is plane address and the device ignores any additional address inputs that exceed the device's requirement.

Mode Selection Table

Mode		CLE	ALE	#CE	#WE	#RE	#WP
Read Mode	Command input	H	L	L	⌐‾⌐	H	X
	Address input	L	H	L	⌐‾⌐	H	X
Program Erase Mode	Command input	H	L	L	⌐‾⌐	H	H
	Address input	L	H	L	⌐‾⌐	H	H
Data input		L	L	L	⌐‾⌐	H	H
Sequential Read and Data output		L	L	L	H	⌐‾⌐	X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/ Vcc

Note 1: "H" indicates a HIGH input level, "L" indicates a LOW input level, and "X" indicates a Don't Care Level.

Note 2: #WP should be biased to CMOS HIGH or LOW for standby.

Command Table

Command	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable during busy
PAGE READ	00h	30h			
READ for COPY BACK	00h	35h			
SEQUENTIAL CACHE READ	31h				
RANDOM CACHE READ	00h	31h			
LAST ADDRESS CACHE READ	3Fh				
READ ID	90h				
READ STATUS	70h				Yes
RESET	FFh				Yes
PAGE PROGRAM	80h	10h			
PROGRAM for COPY BACK	85h	10h			
CACHE PROGRAM	80h	15h			
BLOCK ERASE	60h	D0h			
RANDOM DATA INPUT(1)	85h				
RANDOM DATA OUTPUT(1)	05h	E0h			
READ PARAMETER PAGE	ECh				
READ UNIQUE ID	EDh				
GET FEATURES	EEh				
SET FEATURES	EFh				
READ STATUS ENHANCED	78h				Yes
TWO PLANE READ PAGE	00h	00h	30h		
TWO PLANE READ FOR COPY BACK	00h	00h	35h		
TWO PLANE RANDOM DATA READ	06H	E0h			
TWO PLANE PROGRAM(TRADITIONAL)	80h	11h	81h	10h	
TWO PLANE PROGRAM(ONFI)	80h	11h	80h	10h	

TWO PLANE CACHE PROGRAM(START/CONTINUE)(TRADITIONAL)	80h	11h	81h	15h	
TWO PLANE CACHE PROGRAM(START/CONTINUE) (ONFI)	80h	11h	80h	15h	
TWO PLANE CACHE PROGRAM(END)(TRADITIONAL)	80h	11h	81h	10h	
TWO PLANE CACHE PROGRAM(END)(ONFI)	80h	11h	80h	10h	
TWO PLANE PROGRAM FOR COPY BACK(TRADITIONAL)	85h	11h	81h	10h	
TWO PLANE PROGRAM FOR COPY BACK(ONFI)	85h	11h	85h	10h	
TWO PLANE BLOCK ERASE(TRADITIONAL)	60h	60h	D0h		
TWO PLANE BLOCK ERASE(ONFI)	60h	D1h	60h	D0h	

Note 1: RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.
Note 2: Any commands that are not in the above table are considered as undefined and are prohibited as inputs.
Note 3: Do not cross plane address boundaries when using Copy Back Read and Program for copy back.

Invalid Block Management

The H7A14G21B1CN may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks(see below table). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

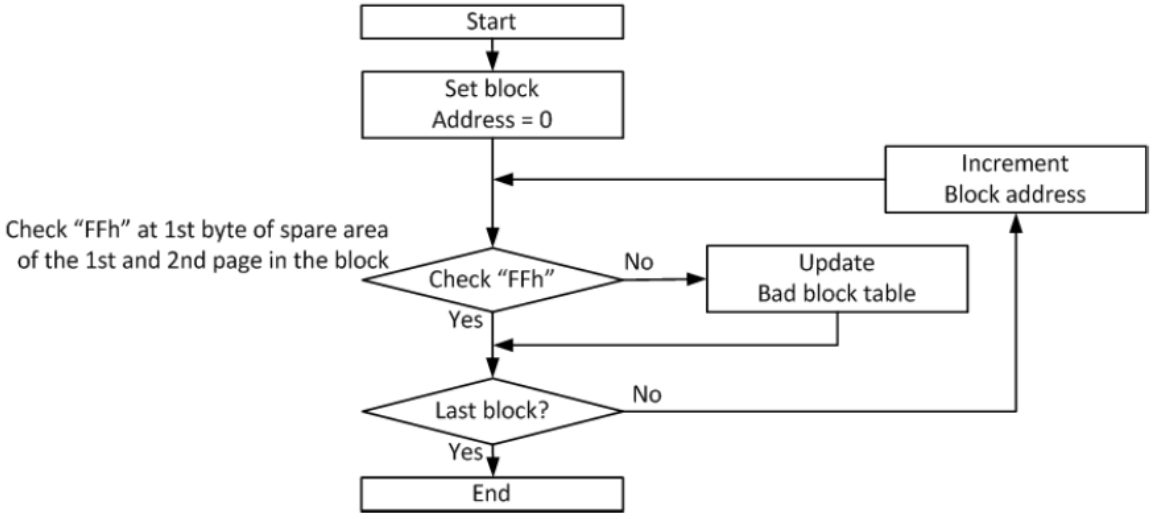
Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	4016	4096	blocks

Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The H7A14G21B1CN has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart.



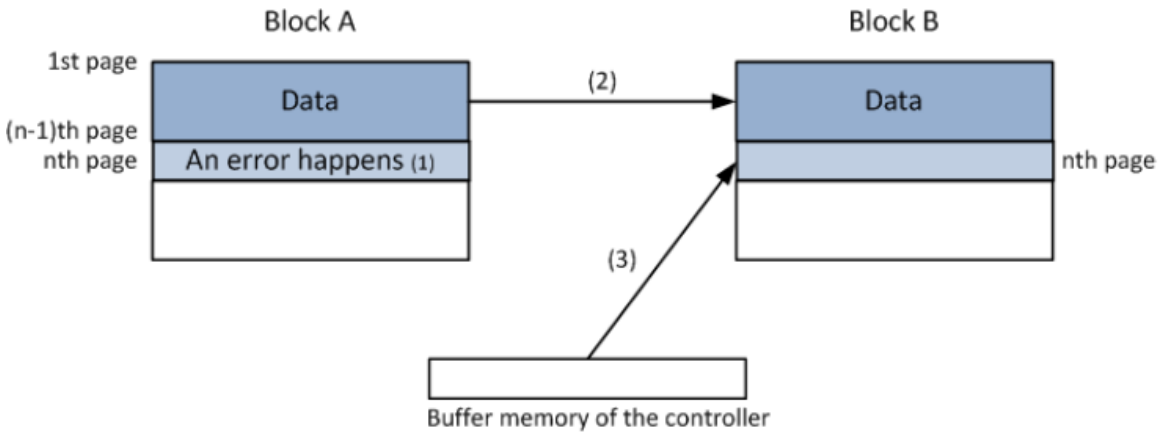
flow chart of create initial invalid block table

Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction



Bad block Replacement

Note 1: An error happens in the nth page of block A during program or erase operation.

Note 2: Copy the data in block A to the same location of block B which is valid block.

Note 3: Copy the nth page data of block A in the buffer memory to the nth page of block B

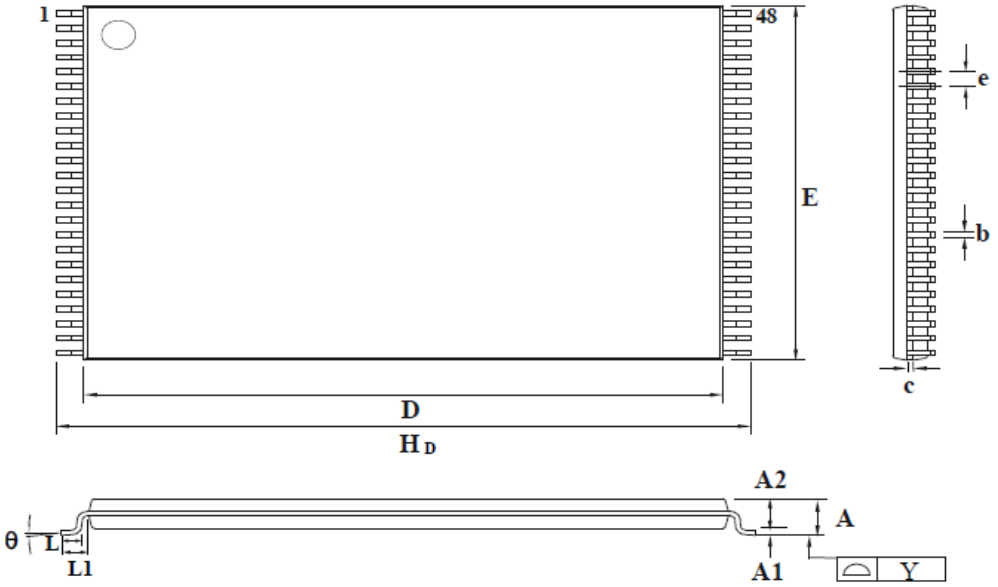
Note 4: Creating or updating bad block table for preventing further program or erase to block A

Addressing in program operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

Package Description

TSOP 48-pin 12x20



Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
HD	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Oct. 2017	Maven Hsu	N/A
1.0	First SPEC. Release.	Oct. 2017	Maven Hsu	N/A