128G-Bit 3.3V NAND FLASH MEMORY

Descriptions

The H7A2DG21C1CX (128G-bit) NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

The H7A2DG21C1CX (128G-bit) NAND Flash device additionally includes a synchronous data interface for high-performance I/O operations. When the synchronous interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN).

Features

- Open NAND Flash Interface (ONFI) 2.3-compliant1
- Multiple-level cell (MLC) technology
- Organization

– Page size: 8936 bytes (8192 + 744 bytes)
– Block size: 256 pages (2048K + 186K bytes)
– Plane size: 2 planes x 1064 blocks per plane
– Device size: 128Gib =8512 blocks

- Synchronous I/O performance4:

1. Up to synchronous timing mode 4[3]

– Clock rate: 10ns (DDR)
– Read/write throughput per pin: 166MT/s

- Asynchronous I/O performance:

– Up to asynchronous timing mode 5
– tRC/tWC: 20ns (MIN)
– Read/write throughout per pin: 50MT/s

- Array performance

– Read Page: 130µs (MAX)
– Program Page: 3200µs (MAX)
– Erase Block: 15ms (MAX)

- Operating voltage range

– VCC: 2.7–3.6V
– VCCQ: 2.7V-3.6V

- Command set: ONFI NAND Flash Protocol
- Advanced Command Set

– Program cache
– Read cache sequential
– Read cache random
– One-time programmable (OTP) mode
– Multi-plane commands
– Multi-LUN operations
– Copyback

- Operating temperature:

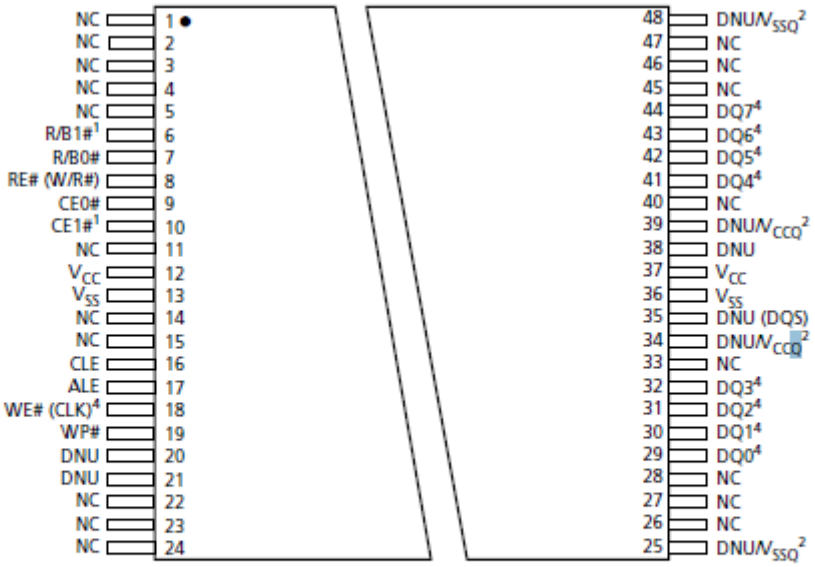
– Commercial: +10°C to +70°C

- Package: 48-pin TSOP
- RESET (FFh) required as first command after Power-on

Ordering Information

Part No	Density	Organization	Package	Grade
H7A2DG21C1CX	128G-bit/8512M-byte	X8	48-Pin TSOP1 12x20mm	Commercial

Pin Assignment



Notes: 1. CE2# and R/B2# are available on dual die and quad die packages. These pins are NC for other configurations.
2. These V_{CCQ} and V_{SSQ} pins are for compatibility with ONFI 2.3. If not supplying V_{CCQ} or V_{SSQ} to these pins, do not use them.

Pin Description (Simplified)

48-pin TSOP1,12x20mm		
Pin Name	**I/O**	**Function**
ALE	Input	Address latch enable
CE#	Input	Chip enable
CLE	Input	Command latch enable
DQx	I/O	Data inputs/outputs
DQS	I/O	Data strobe
W/R#	Input	Read Enable and write/read
CLK	Input	Command Latch Enable
WP#	Input	Data Input / Output (x8)
R/B#	Output	Power Supply
Vcc	Supply	Ground
VccQ	Supply	
Vss	Supply	
VssQ	Supply -	
NC	-	Do Not Use:

DNU		Do Not Use:
RFU		Reserved for future use

Note1: Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.

Absolute Maximum Rating(3.3V)

Item	Symbol	Min1	Max1	Unit
Voltage input	V_{IN}	-0.6	4.6	V
V_{CC} supply voltage	V_{CC}	-0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.6	4.6	V
Storage temperature	T_{STG}	-65	150	°C

Note 1: Voltage on any pin relative to V_{SS}.

Operating Ranges(3.3V)

Parameter	Symbol	Conditions	Spec.		Unit
			Min.	Max.	
Supply Voltage	Vcc		2.7	3.6	V
Ambient Temperature, Operating	Ta	Commercial	10	70	˚C

DC Characteristics(Asynchronous)

Parameters	Symbol	Conditions	Spec.		Unit
			MIN	Max	
Array read current (active)	Icc1_A	-	-	50	mA
Array program current (active)	Icc2_A	-	-	50	mA
Erase current (active)	Icc3_A	-	-	50	mA
I/O burst read current	Icc4R_A	tRC = tRC (MIN); IOUT= 0mA	-	35	mA
I/O burst write current	Icc4W_A	tWC = tWC (MIN)	-	10	mA
Bus idle current	Icc5_A	-	-	5	mA
Current during first RESET command after power-on	Icc6	-	-	10	mA
Standby current - VCC	ISB	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	360	uA
Standby current - VCCQ	ISBQ	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	20	uA
Staggered power-up current	IST	tRISE = 1ms; CLINE = 0.1uF	-	10	mA

DC Characteristics(Synchronous)

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	Max	Unit	
Array read current (active)	Icc1_S	CE# = VIL; tCK = tCK (MIN)	-	50	mA	
Array program current (ac-active)	Icc2_S	tCK = tCK (MIN)	-	50	mA	
Erase current (active)	Icc3_S	tCK = tCK (MIN)	-	50	mA	
I/O burst read current	Icc4R_S	tCK = tCK (MIN)	-	35	mA	
I/O burst write current	Icc4W_S	tCK = tCK (MIN)	-	20	mA	
Bus idle current	Icc5_S	tCK = tCK (MIN)	-	10	mA	
Standby current - VCC	ISB	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	360	uA	
Standby current - VCCQ	ISBQ	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	20	uA	

Notes: 1. All values are per LUN unless otherwise specified.

DC Characteristics(3.3V VCCQ)

Parameters	Symbol	Conditions	Spec.			Unit	Notes
			Symbol	MIN	Max		
AC input high voltage	VIH(AC)	CE#, DQx, DQS, DQS#, ALE, CLE, CLK (WE#), CLK#, W/R# (RE#), WP#	V_{IH} (AC)	0.8 × V_{CCQ}	V_{CCQ} + 0.3	V	
AC input low voltage	VIL(AC)		V_{IL} (AC)	–0.3	0.2 × V_{CCQ}	V	
DC input high voltage	VIH(DC)	DQx, DQS, DQS#, ALE, CLE, CLK (WE#), CLK#, W/R# (RE#)	V_{IH} (DC)	0.7 × V_{CCQ}	V_{CCQ} + 0.3	V	
DC input low voltage	VIL(DC)		V_{IL} (DC)	–0.3	0.3 × V_{CCQ}	V	
Input leakage current	ILI	Any input VIN = 0V to VCCQ (all other pins under test=0V)	I_{LI}		±10	µA	
Output leakage current	ILO	I/Os are disabled; VOUT = 0V to VCCQ	I_{LO}		±10	µA	1
Output low current (R/B#)	IOL (R/B#)	VOL = 0.4V	I_{OL}	8	-	µA	2

Notes: 1. All leakage currents are per LUN. Two LUNs have a maximum leakage current of ±20µA and four LUNs have a maximum leakage current of ±40µA in the asynchronous interface.

2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to Full. See Table 14 on page 59 for additional details.

AC timing characteristics for Command, Address and Data Input(3.3V)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 57		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		50		30		20		15		12		10		ns	
Frequency		≈20		≈33		≈50		≈70		≈83		≈100		MHz	
Access window of DQx from CLK	tAC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data start	tADL	100	–	100	–	70	–	70	–	70	–	70	–	ns	1
Command, address data delay	tCAD	25	–	25	–	25	–	25	–	25	–	25	–	ns	
ALE, CLE, W/R#	tCALH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# setup	tCALS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ hold – command, address	tCAH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ setup – command, address	tCAS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# hold	tCH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
Average CLK cycle time	tCK (avg)	50	100	30	50	20	30	15	20	12	15	10	12	ns	3
Absolute CLK cycle time, from rising edge to rising edge	tCK (abs)	tCK (abs) MIN = tCK (avg) + tJIT (per) MIN tCK (abs) MAX = tCK (avg) + tJIT (per) MAX												ns	
CLK cycle HIGH	tCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK	4
CLK cycle LOW	tCKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK	4
Data output end to W/R# HIGH	tCKWR	tCKWR (MIN) = RoundUp[(tDQSCK(MAX) + tCK)/ tCK]												tCK	
CE# setup time	tCS	35	–	25	–	15	–	15	–	15	–	15	–	ns	
Data hold time	tDH	5	–	2.5	–	1.7	–	1.3	–	1.1	–	0.8	–	ns	
Access window of DQS from CLK	tDQSCK	–	20	–	20	–	20	–	20	–	20	–	20	ns	
DQS, DQx Driven by NAND	tDQSD	–	18	–	18	–	18	–	18	–	18	–	18	ns	
DQS, DQx to tri-state	tDQSHZ	–	20	–	20	–	20	–	20	–	20	–	20	ns	5

DQS input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-DQ skew	tDQSQ	–	5	–	2.5	–	1.7	–	1.3	–	1.0	–	0.85	ns	
Data input	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
Data setup time	tDS	40	–	20	–	15	–	10	–	10	–	7	–	ns	
DQS falling edge from CLK rising – hold	tDSH	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	tCK	
DQS falling to CLK rising – set-up	tDSS	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	tCK	
Data valid window	tDVW	tDVW = tQH - tDQSQ												ns	

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 57		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Half clock period	tHP	tHP = MIN(tCKH, tCKL)												ns	
The deviation of a given tCK (abs) from a tCK (avg)	tJIT (per)	–0.7	0.7	–0.7	0.7	–0.7	0.7	–0.6	0.6	–0.6	0.6	–0.5	0.5	ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	tQH = tHP - tQHS												ns	
Data hold skew factor	tQHS	–	6	–	3	–	2	–	1.5	–	1.2	–	1	ns	
RE# high to WE# low	tRHW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Ready to RE# low	tRR	20	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# high to R/B# low	tWB	–	100	–	100	–	100	–	100	–	100	–	100	ns	
Command cycle to data output	tWHR	80	–	60	–	60	–	60	–	60	–	60	–	ns	

DQS write preamble	tWPRE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	tCK	
DQS write post-amble	tWPST	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	tCK	
W/R# LOW to data output cycle	tWRCK	20	–	20	–	20	–	20	–	20	–	20	–	ns	
WP# transition to WE# low	tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	

Notes: 1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.

2. This value is specified in the parameter page.

3. tCK(avg) is the average clock period over any consecutive 200-cycle window.

4. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.

5. tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.

6. Synchronous interface is only valid for Async/sync and Speed Graded marked parts (see Figure 1 on page 2).

7. BGA devices support up to Synchronous timing mode 5. TSOP devices support up to timing mode 4.

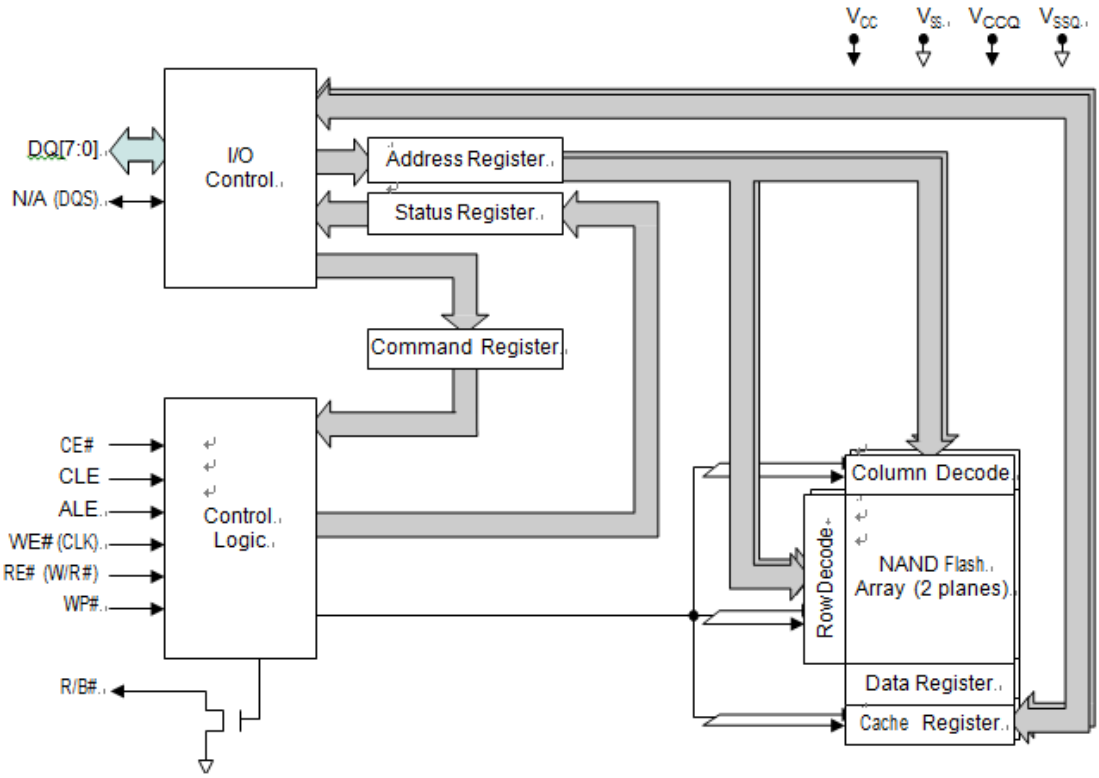
Array Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	
ERASE BLOCK operation time	tBERS	–	15	ms	
Cache busy	tCBSY	–	3200	µs	
Change column setup time to data in/out or next command	tCCS	–	250	ns	
Dummy busy time	tDBSY	–	1	µs	
Cache read busy time	tRCBSY	–	130	µs	4
Busy time for SET FEATURES and GET FEATURES operations	tFEAT	–	1	µs	
Busy time for interface change	tITC	–	1	µs	1
LAST PAGE PROGRAM operation time	tLPROG	–	–	µs	2

Power-on reset time	tPOR	–	1	ms	
PROGRAM PAGE operation time	tPROG	–	3200	µs	
READ PAGE operation time	tR	–	130	µs	4
Device reset time (Read/Program/Erase)	tRST	–	6/12/600	µs	3

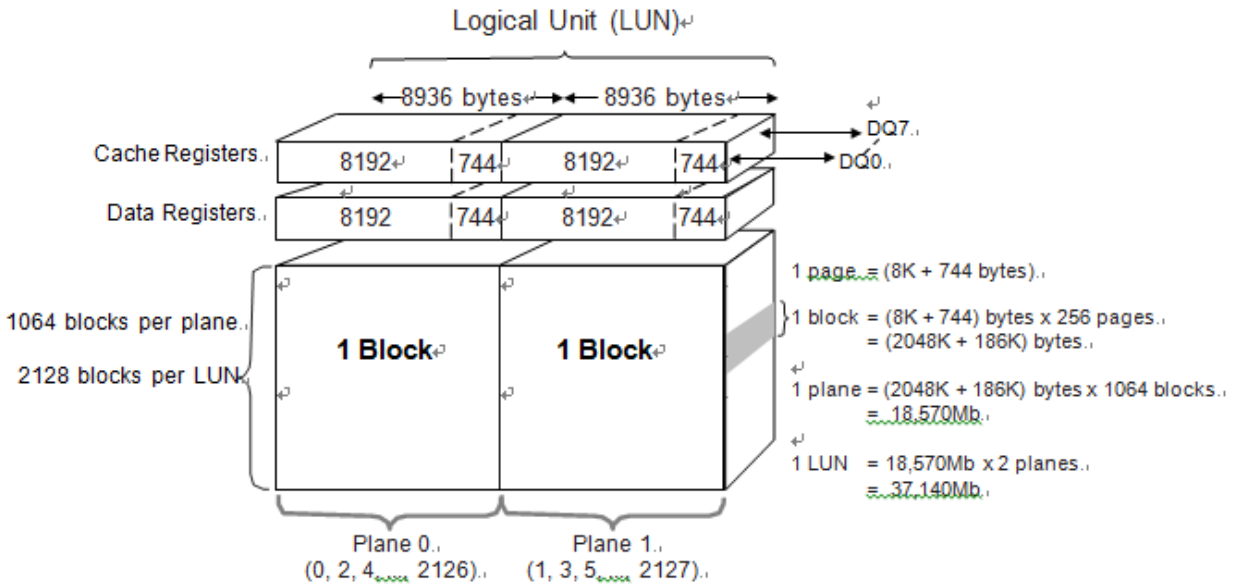
Notes: 1. tITC (MAX) is the busy time when the interface changes from asynchronous to synchronous using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the tITC time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.
2. tLPROG = tPROG (last page) + tPROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
3. If RESET command is issued when the target is READY, the target goes busy for a maximum of 5µs.
4. For Read Retry, options 4 to 7, tRCBY and tR MAX may be up to 340µs.

NAND Flash LUN Functional Block Diagram



Notes: 1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Signal names in parentheses are the signal names when the synchronous interface is active.

Memory Array Organization



Array Addressing for 32Gib Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA02
Second	LOW	LOW	CA133	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA84
Fifth	LOW	LOW	LOW	LA05	BA19	BA18	BA17	BA16

Notes: 1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.

2. When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

3. Column addresses 8936 (22E8h) through 16,383 (3FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.

4. BA[8] is the plane-select bit: Plane 0: BA[8] = 0

Plane 1: BA[8] = 1

5. LA0 and LA1 are the LUN-select bit. They are present only when two or more LUNs are shared on the target, otherwise they should be held LOW.

LUN 0: LA0 = 0, LA1 = 0

LUN 1: LA0 = 1, LA1 = 0

6. For single LUN Targets block address 2128 through 4095 are invalid, out of bounds, do not exist in the device, and cannot be addressed.

For two LUN Targets block addresses 2128 through 4095 and 6224 through 8191 are invalid, out of bounds, do not exist in the device, and cannot be addressed.

Mode Selection Table

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}
Bus idle	L	X	X	H	H	X	X	X
Command input	L	H	L		H	X	input	H
Address input	L	L	H		H	X	input	H
Data input	L	L	L		H	X	input	H
Data output	L	L	L	H		X	output	X
Write protect	X	X	X	X	X	X	X	L

Notes: 1. DQS is tri-stated when the asynchronous interface is active.

2. WP# should be biased to CMOS LOW or HIGH for standby.

3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL

Command Table

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	# Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy1	Valid While Other LUNs are Busy2	Notes
RESET Operations									
RESET by DIE	FAh	3	—	—	—	—	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	—	—	—	—	Yes	Yes	
RESET	FFh	0	—	—	—	—	Yes	Yes	
Identification Operations									
READ ID	90h	1	—	—	—	—			3
READ PARAMETER PAGE	ECh	1	—	—	—	—			
Configuration Operations									
GET FEATURES	EEh	1	—	—	—	—			3
SET FEATURES	EFh	1	4	—	—	—			4
STATUS Operations									
READ STATUS	70h	0	—	—	—	—	Yes		
READ STATUS ENHANCED	78h	3	—	—	—	—	Yes	Yes	
Column Address Operations									
CHANGE READ COLUMN	05h	2	—	E0h	—	—		Yes	

CHANGE READ COLUMN ENHANCED (ONFI)	06h	5	—	E0h	—	—		Yes	
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	5	—	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	—	—	—		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	11h (Optional)	—	—		Yes	5
READ Operations									
READ MODE	00h	0	—	—	—	—		Yes	
READ PAGE	00h	5	—	30h	—	—		Yes	6
READ PAGE MULTI-PLANE	00h	5	—	32h	—	—		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	—	—	—	—		Yes	7
READ PAGE CACHE RANDOM	00h	5	—	31h	—	—		Yes	6, 7
READ PAGE CACHE LAST	3Fh	0	—	—	—	—		Yes	7

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	# Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy1	Valid While Other LUNs are Busy2	Notes
PROGRAM Operations									
PROGRAM PAGE	80h	5	Yes	10h	—	—		Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5	Yes	11h	—	—		Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h	—	—		Yes	8
ERASE Operations									
ERASE BLOCK	60h	3	—	D0h	—	—		Yes	
ERASE BLOCK MULTI-PLANE (ONFI)	60h	3	—	D1h	—	—		Yes	
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	3	—	60h	3	D0h		Yes	
COPYBACK Operations									
COPYBACK READ	00h	5	—	35h				Yes	6

COPYBACK PROGRAM	85h	5	Optional	10h				Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h				Yes	

Valid Blocks per LUN

Parameter	Part Number Guide	Symbol	Min	Max	Unit	Notes
Valid block number	FxxL83A	NVB	2048	2128	Blocks	1

Notes: 1. Invalid blocks are block that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; how- ever, the total number of available blocks will not drop below NVB during the endurance
life of the device. Do not erase or program blocks marked invalid from the factory.

Error Management

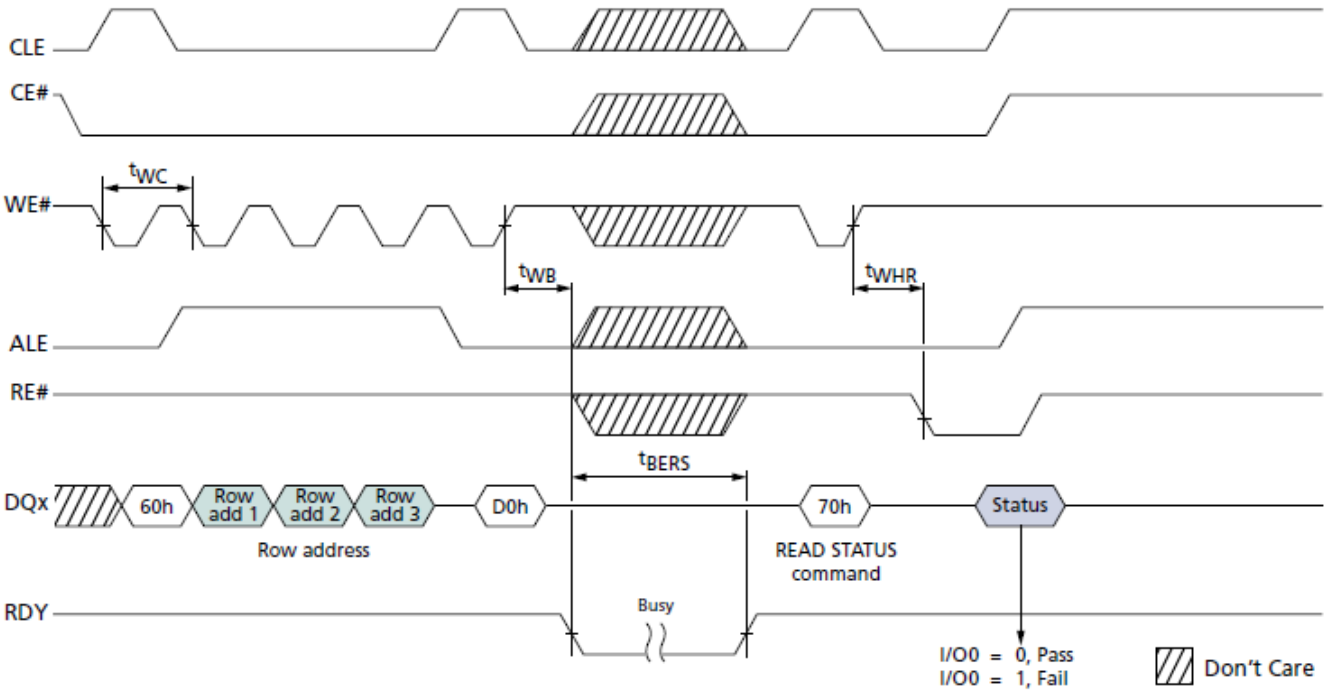
Each NAND Flash LUN is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the LUNs could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per LUN will not fall below NVB during the endurance life of the product.
Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algo- rithms. This type of software environment ensures data integrity.
Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.
NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compatible with ONFI Fac- tory Defect Mapping requirements. See Table 18 for the first spare area location and the bad-block mark.
System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.
Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation.
- Under typical conditions, use the minimum required ECC shown in Table 18.
- Use bad-block management and wear-leveling algorithms.

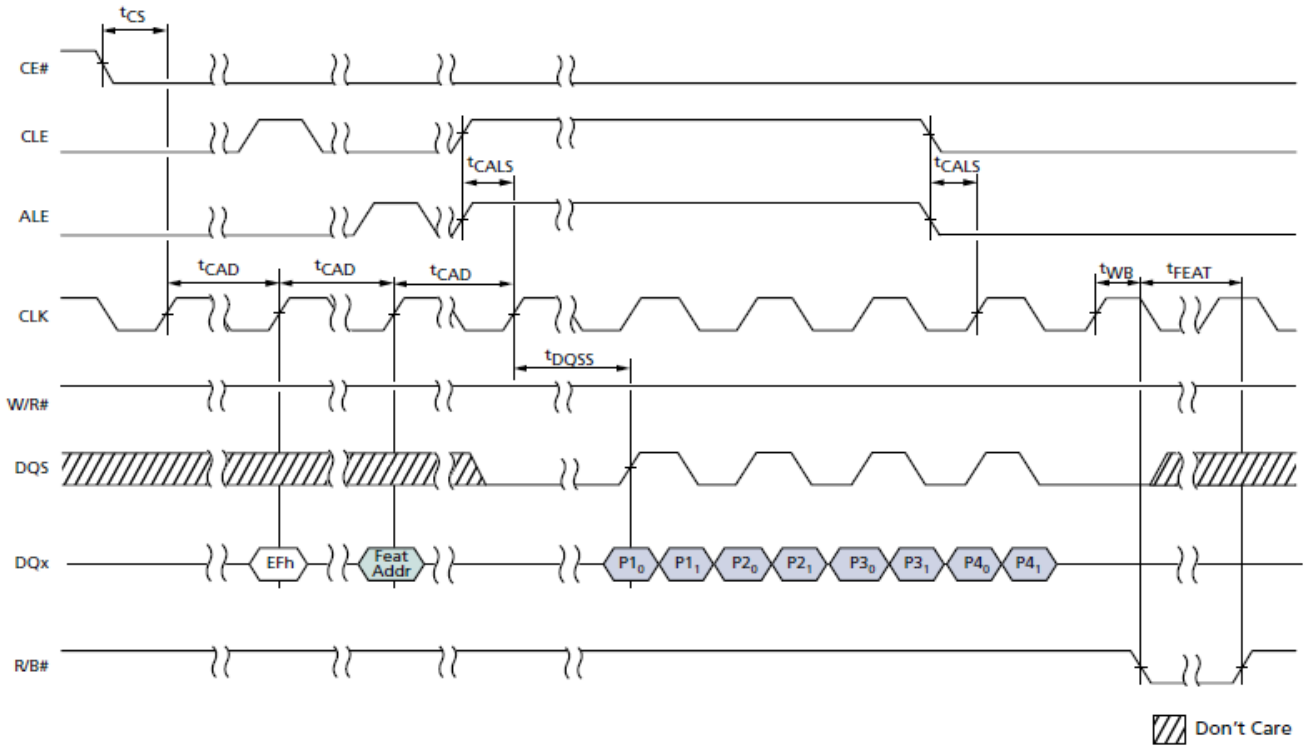
Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB)	2054
Total available blocks per LUN	2128
First spare area location	Byte 8192
Bad-block mark	00h
Minimum required ECC	40-bit ECC per 1117 bytes of data

ERASE BLOCK Operation



SET FEATURES Operation



Notes: 1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).

2. tDSH (MIN) generally occurs during tDQSS (MIN).

3. tDSS (MIN) generally occurs during tDQSS (MAX).

4. The cycle the tCAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Asynchronous Addresses

An asynchronous address is written from DQx to the address register on the rising edge of WE# when:

- CE# is LOW,
- ALE is HIGH,
- CLE is LOW, and
- RE# is HIGH.

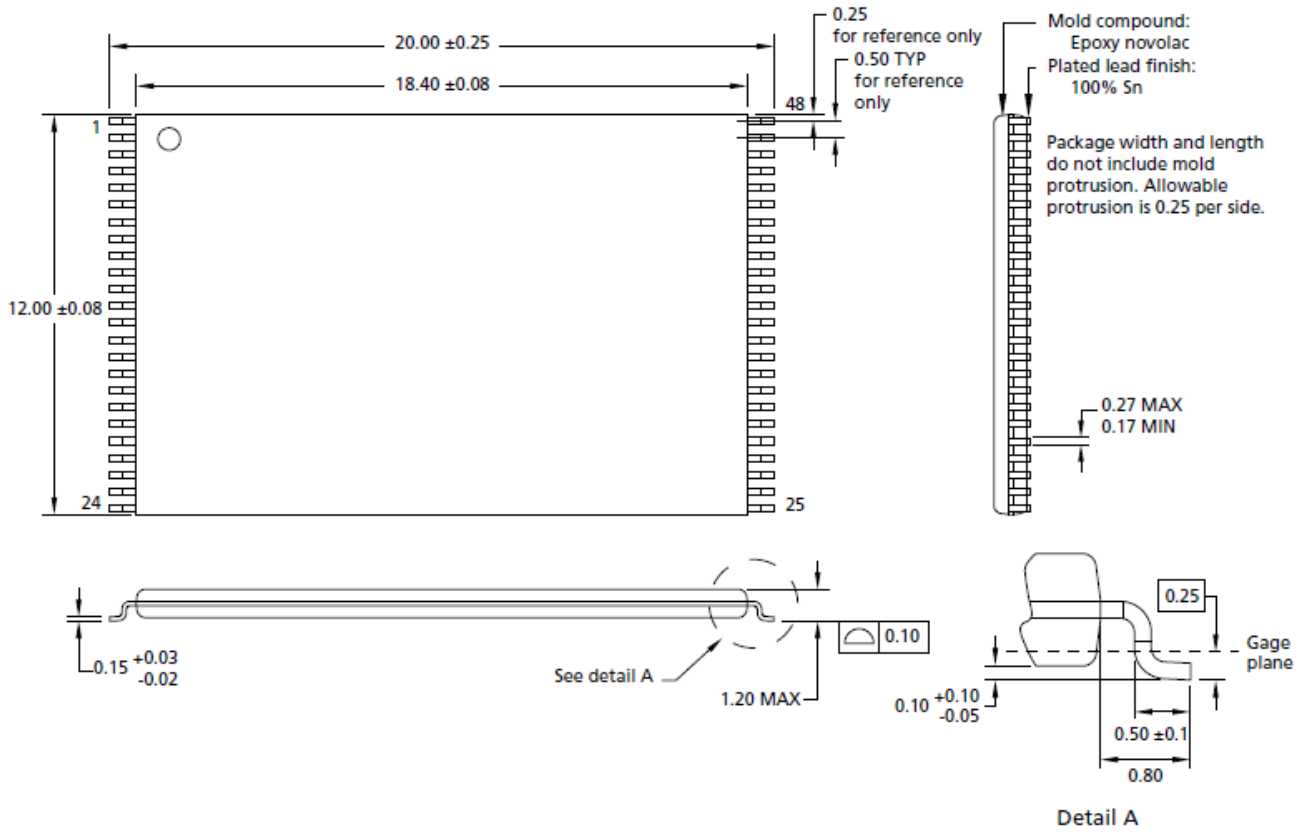
Bits that are not part of the address space must be LOW (see “Device and Array Organization”). The number of cycles required for each command varies. Refer to the command

descriptions to determine addressing requirements (see “Command Definitions”).
Addresses are typically ignored by LUNs that are busy; however, some addresses are accepted by LUNs even when they are busy; for example, like address cycles that follow the READ STATUS ENHANCED (78h) command.

Package Description

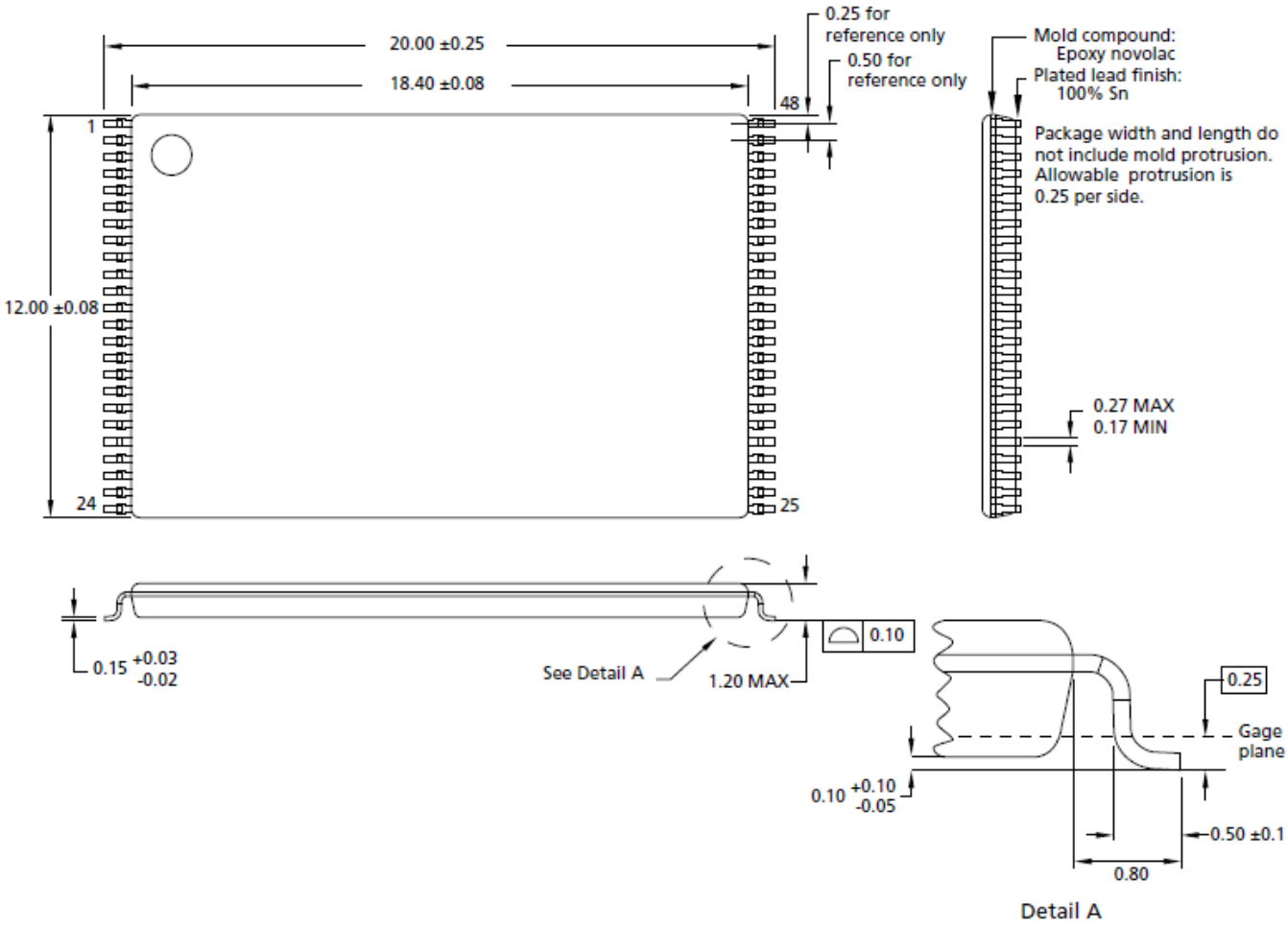
TSOP 48-pin 12x20

48-Pin TSOP Type 1 CPL (WP Package Code)



Notes: 1. All dimensions are in millimeters.

48-Pin TSOP Type 1 OCPL (WC Package Code)



Notes: 1. All dimensions are in millimeters.

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Dec. 2018	Y.T Chen	N/A
1.0	First SPEC. Release.	Dec. 2018	Y.T Chen	N/A