16G-Bit 3.3V NAND FLASH MEMORY

Descriptions

The H7A2AG21C1CX (16G-bit) NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

The H7A2AG21C1CX (16G-bit) NAND Flash device additionally includes a synchronous data interface for high-performance I/O operations. When the synchronous interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN).

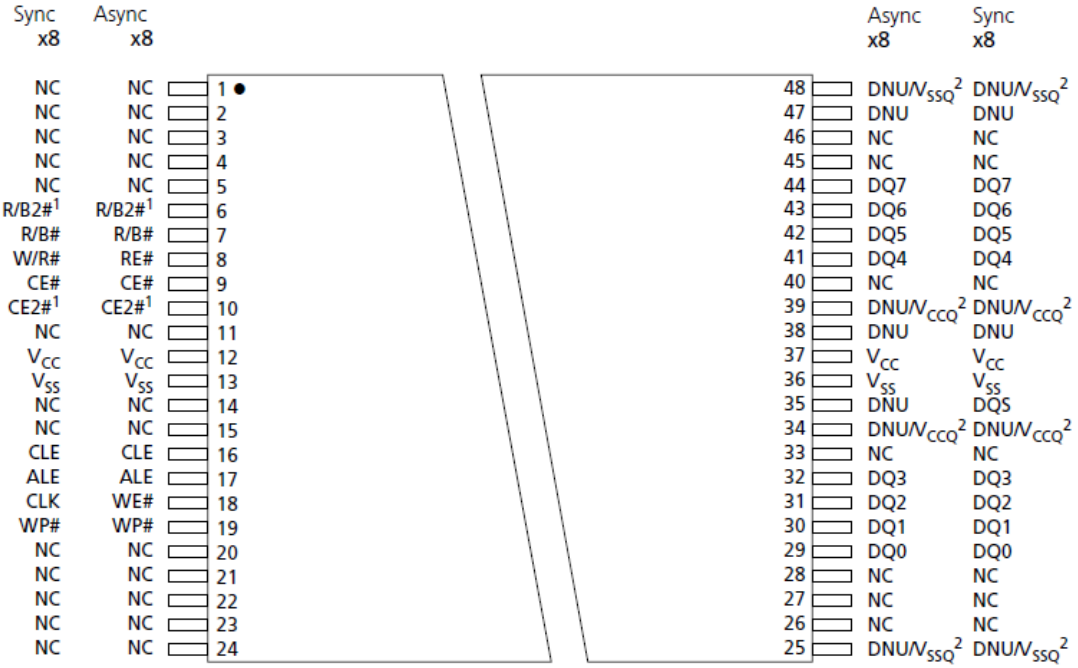
Features

- Open NAND Flash Interface (ONFI) 2.2-compliant1
- Multiple-level cell (MLC) technology
- Organization
  - Page size x8: 4320 bytes (4096 + 224 bytes)
  - Block size: 256 pages (1024K + 56K bytes)
  - Plane size: 2 planes x 1024 blocks per plane
  - Device size: 16Gb: 2048 blocks;32Gb: 4096 blocks
- Synchronous I/O performance
  - Up to synchronous timing mode 4
  - Clock rate: 12ns (DDR)
  - Read/write throughput per pin: 166 MT/s
- Asynchronous I/O performance
  - Up to asynchronous timing mode 5
  - Read/write throughput per pin: 50 MT/s
  - tRC/tWC: 20ns (MIN)
- Array performance
  - Read page: 75 μs (MAX)
  - Program page: 1300 μs (TYP)
  - Erase block: 3.8ms (TYP)
- Operating Voltage Range
  - VCC: 2.7 – 3.6V
  - VCCQ: 2.7 – 3.6V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set
  - Program cache
  - Read cache sequential
  - Read cache random
  - One-time programmable (OTP) mode
  - Multi-plane commands
  - Multi-LUN operations
  - Read unique ID
  - Copyback
- Operating temperature:
  - Commercial: 0°C to +70°C
- Package: 48-pin TSOP

Ordering Information

Part No	Density	Organization	Package	Grade
H7A2AG21C1CX	16G-bit/2048M-byte	X8	48-Pin TSOP1 12x20mm	Commercial

Pin Assignment



Notes:
1. CE2# and R/B2# are available on dual die packages. They are NC for other configurations.
2. These V_{CCQ} and V_{SSQ} pins are for compatibility with ONFI 2.2. If not supplying V_{CCQ} or V_{SSQ} to these pins, do not use them.

Pin Description (Simplified)

48-pin TSOP1,12x20mm		
Pin Name	**I/O**	**Function**
#WP	Input	Write Protect
ALE	Input	Address Latch Enable
#CE	Input	Chip Enable
#WE	Input	Write Enable and clock
R/B#	Output	Ready/Busy
#RE	Input	Read Enable and write/read
CLE	Input	Command Latch Enable
DQX	Input / Output	Data Input / Output (x8)
V_{cc}	Supply	Power Supply
V_{SS}	Supply	Ground
DNU	-	Do Not Use:
N.C	-	Not Connect

Note1: Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.

Absolute Maximum Rating(3.3V)

Item	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{cc}		-0.6 ~ 4.6	V
Voltage Applied to Any Pin	V_{in}	Relative to Ground	-0.6 ~ 4.6	V
Storage Temperature	T_{STG}		-65 ~ 150	˚C
Short circuit output current	I_{os}		5	mA

Note 1: Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.

Note 2: Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

Note 3: This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

Operating Ranges(3.3V)

Parameter	Symbol	Conditions	Spec.		Unit
			Min.	Max.	
Supply Voltage	Vcc		2.7	3.6	V
Ambient Temperature, Operating	Ta	Commercial	0	70	˚C

DC Characteristics(Asynchronous)

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	
Array read current (active)	Icc1	-	-	20	50	mA
Array program current (active)	Icc2	-	-	20	50	mA
Erase current (active)	Icc3	-	-	20	50	mA
I/O burst read current	Icc4R	tRC = tRC (MIN); IOUT= 0mA	-	8	10	mA
I/O burst write current	Icc4W	tWC = tWC (MIN)	-	8	10	mA
Bus idle current	Icc5	-	-	3	5	mA
Current during first RESET command after power-on	Icc6	-	-	-	10	mA
Standby current - VCC	ISB	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	10	50	uA
Standby current - VCCQ	ISBQ	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	3	10	uA
Staggered power-up current	IST	tRISE = 1ms; CLINE = 0.1uF	-	-	10	mA

DC Characteristics(Synchronous)

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	
Array read current (active)	Icc1	CE# = VIL; tCK = tCK (MIN)	-	25	50	mA
Array program current (ac-active)	Icc2	tCK = tCK (MIN)	-	25	50	mA
Erase current (active)	Icc3	tCK = tCK (MIN)	-	25	50	mA
I/O burst read current	Icc4R	tCK = tCK (MIN)	-	20	27	mA
I/O burst write current	Icc4W	tCK = tCK (MIN)	-	20	27	mA
Bus idle current	Icc5	tCK = tCK (MIN)	-	5	10	mA
Standby current - VCC	ISB	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	10	50	uA
Standby current - VCCQ	ISBQ	CE# = VCCQ - 0.2V; WP# = 0V/VCCQ	-	3	10	uA

DC Characteristics(VCCQ)

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	
AC input high voltage	VIH(AC)	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	-	25	35	mA
AC input low voltage	VIL(AC)		-	25	35	mA
DC input high voltage	VIH(DC)	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#)	-	25	35	mA
DC input low voltage	VIL(DC)		-	-	1	mA
Input leakage current	ILI	Any input VIN = 0V to VCCQ (all other pins under test = 0V)	-	20	100	uA
Output leakage current	ILO	DQ are disabled; VOUT = 0V to VCCQ	-	-	+/-10	uA
Output low current (R/B#)	IOL (R/B#)	VOL = 0.4V	-	-	+/-10	uA

Notes 1: All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA in the asynchronous interface.

Notes 2: DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength.

AC Measurement Conditions(3.3V)

Parameter	Symbol	Spec.		Unit
		Device	Max	
Input capacitance – ALE, CE#, CLE, RE#, WE#, WP#	CIN	Single die package	6	pF
		Dual die package	10	
Input/output capacitance – DQ[7:0], DQS	CIO	Single die package	5	
		Dual die package	8	

Note : These parameters are verified in device characterization and are not 100% tested. Test conditions: TC = 25°C; f = 1 MHz; Vin = 0V.

AC timing characteristics for Command, Address and Data Input(3.3V)

Parameter	Symbol	Spec.		Unit
		MIN	MAX	
ALE to Data Loading Time	tADL	70	-	ns
ALE Hold Time	tALH	5	-	ns
ALE setup Time	tALS	10	-	ns
#CE Hold Time	tCH	5	-	ns
CLE Hold Time	tCLH	5	-	ns
CLE setup Time	tCLS	10	-	ns
#CE setup Time	tCS	15	-	ns
Data Hold Time	tDH	5	-	ns
Data setup Time	tDS	7	-	ns
Write Cycle Time	tWC	20	-	ns
#WE High Hold Time	tWH	7	-	ns
#WE Pulse Width	tWP	10	-	ns
#WP setup Time	tWW	100	-	ns

Note: 1. tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.

AC timing characteristics for Operation(3.3V)

Parameter	Symbol	Spec.		Unit
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	25	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	30	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Cache read busy time	tRCBSY	3	75	us
Output High-Z to #RE LOW	tIR	0	-	ns
READ PAGE operation time	tR	-	75	us
READ Cycle Time	tRC	20	-	ns
#RE Access Time	tREA	-	16	ns
#RE HIGH Hold Time	tREH	7	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	200	ns
#RE LOW to output hold	tRLOH	0	-	ns
#RE Pulse Width	tRP	10	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	us
#WE HIGH to Busy(3)	tWB	-	200	ns
#WE HIGH to #RE LOW	WHR	60	-	ns

Note 1: Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested

Note 2: Do not issue new command during tWB, even if RY/#BY is ready.

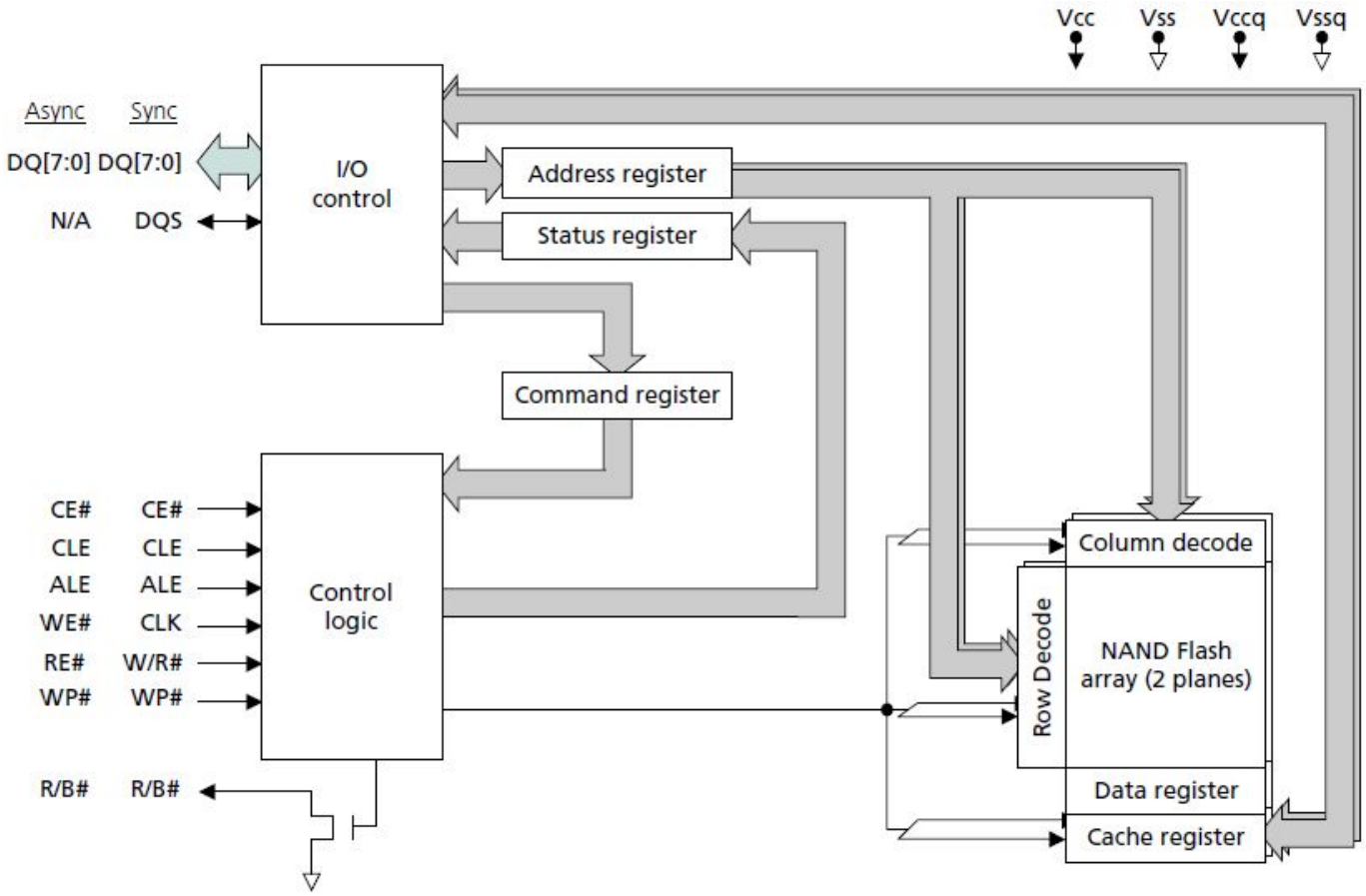
Program and Erase Characteristics

Parameter	Symbol	Spec.		Unit
		TYP	MAX	
Number of partial page programs	NoP	-	1	cycles
Page Program time	tPROG	1300	2600	us
Busy Time for Cache program (1)	tCBSY	-	40	us
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	us
Busy Time for program/erase at locked block	tLBSY	-	3	us
Busy Time for OTP program when OTP is protected	tOBSY	-	40	us
Block Erase Time	tBERS	3.8	10	ms
Last Page Program time (2)	tLPROG	-	-	-
Busy Time for Two Plane page program and Two Plane Block Erase	tDBSY	0.5	1	us

Note: 1. tCBSY maximum time depends on timing between internal program complete and data-in.

Note: 2. tLPROG = Last tPROG + Last -1 tPROG – Last page Address, Command and Data load time.

Block Diagram



Memory Array Organization

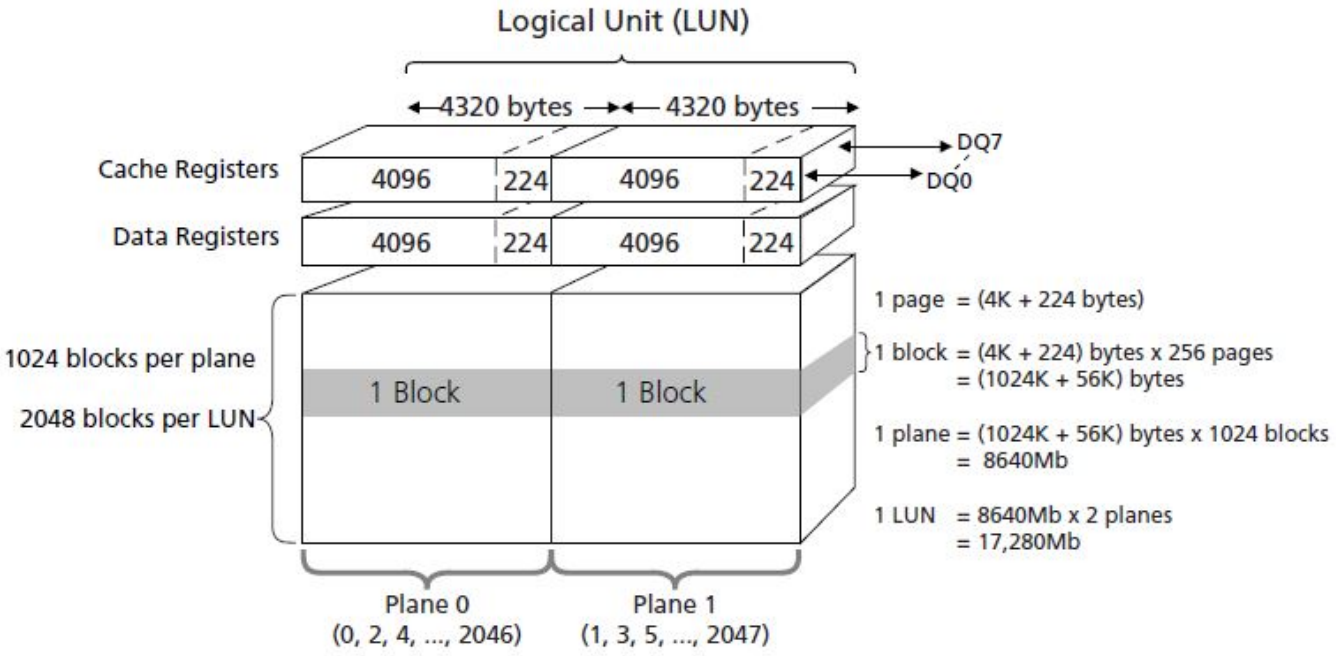


Table 2: Array Addressing for Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	LOW	LOW	CA12[3]	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8[4]
Fifth	LOW	LOW	LOW	LOW	LA0[5]	BA18	BA17	BA16

Notes: 1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.

Notes: 2. When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.

Notes: 3. Column addresses 4320 (10E0h) through 8191 (1FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.

Notes: 4. BA[8] is the plane-select bit:

Plane 0: BA[8] = 0

Plane 1: BA[8] = 1

Notes: 5. LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise, it should be held LOW.

LUN 0: LA0 = 0

LUN 1: LA0 = 1

Mode Selection Table

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}[2]	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L	↑	H	X	input	H	
Address input	L	L	H	↑	H	X	input	H	
Data input	L	L	L	↑	H	X	input	H	
Data output	L	L	L	H	↓	X	output	X	
Write protect	X	X	X	X	X	X	X	L	

Notes: 1. DQS is tri-stated when the asynchronous interface is active.

Notes: 2. WP# should be biased to CMOS LOW or HIGH for standby.

Notes: 3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

Command Table

Command	1st Cycle	Number of Valid Address Cycles	Data Input Cycles	2nd Cycle	Valid While Selected LUN is Busy1	Valid While Other LUNs are Busy2
PAGE READ	00h	5	-	30h		Yes
READ for COPY BACK	00h	5		35h		Yes
SEQUENTIAL CACHE READ	31h	0	-	-		Yes
RANDOM CACHE READ	00h	5	-	31h		Yes
LAST ADDRESS CACHE READ	3Fh	0	-	-		Yes
READ ID	90h	1	-	-		
READ STATUS	70h	0	-	-	Yes	
RESET	FFh	0	-	-	Yes	Yes
PAGE PROGRAM	80h	5	Yes	10h		Yes
PROGRAM for COPY BACK	85h	5	Optional	10h		Yes
CACHE PROGRAM	80h	5	Yes	15h		Yes
BLOCK ERASE	60h	3	-	D0h		Yes
READ PARAMETER PAGE	ECh	1	-	-		
READ UNIQUE ID	EDh	1	-	-		
GET FEATURES	EEh	1	-	-		
SET FEATURES	EFh	1	4	-		
READ STATUS ENHANCED	78h	3	-	-	Yes	Yes
READ PAGE MULTIPLANE	00h	5	-	32h		Yes
TWO PLANE READ FOR COPY BACK	00h	5	-	32h		Yes
TWO PLANE RANDOM DATA READ	00H	5	-	31h		Yes
TWO PLANE PROGRAM	80h	5	Yes	11h		Yes
CACHE PROGRAM	80h	5	Yes	15h		Yes
TWO PLANE PROGRAM FOR COPY BACK	85h	5	Optional	11h		Yes
ERASE BLOCK MULTI-PLANE	60h	3	-	D1h		Yes

Note 1: RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.
Note 2: Any commands that are not in the above table are considered as undefined and are prohibited as inputs.
Note 3: Do not cross plane address boundaries when using Copy Back Read and Program for copy back.

Invalid Block Management

The H7A2AG21C1CX may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks(see below table). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

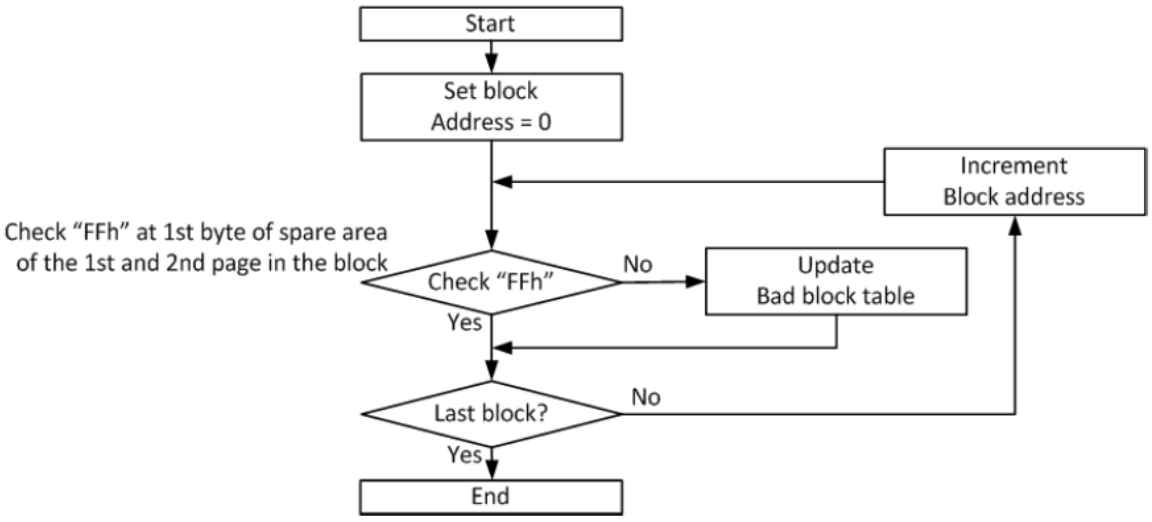
Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	1998	2048	blocks

Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The H7A2AG21C1CX has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart.



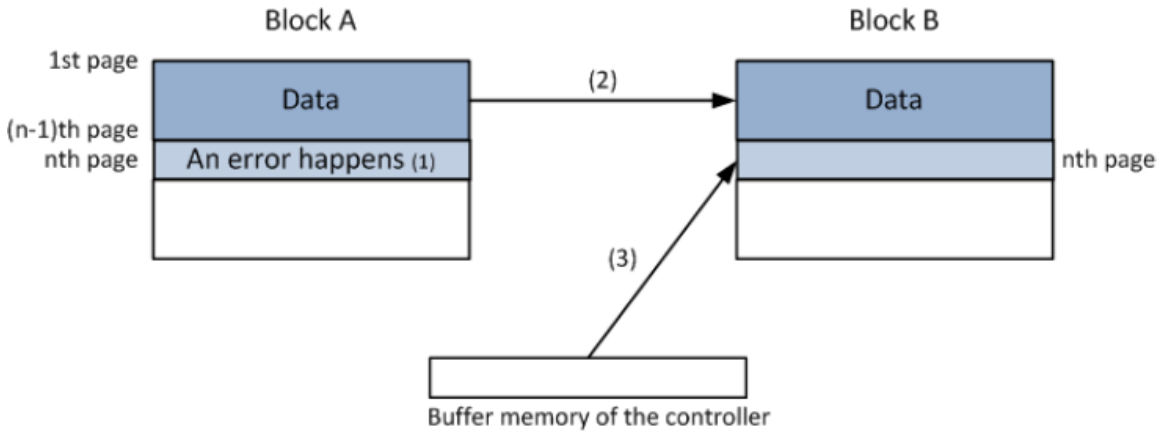
flow chart of create initial invalid block table

Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction



Bad block Replacement

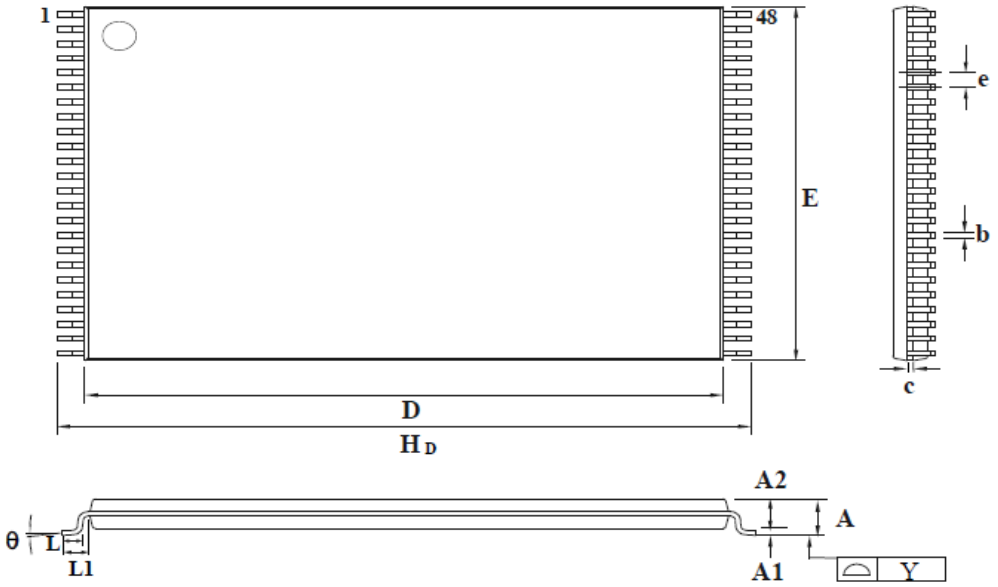
Note 1: An error happens in the nth page of block A during program or erase operation.
Note 2: Copy the data in block A to the same location of block B which is valid block.
Note 3: Copy the nth page data of block A in the buffer memory to the nth page of block B
Note 4: Creating or updating bad block table for preventing further program or erase to block A

Addressing in program operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

Package Description

TSOP 48-pin 12x20



Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
HD	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Nov. 2018	Ternence Chen	N/A
1.0	First SPEC. Release.	Nov. 2018	Ternence Chen	N/A