

## 16Gb (128Mx8Banksx16) DDR4 SDRAM

### Descriptions

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR4 SDRAM uses an 8n-prefetch architecture to achieve high-speed operation. The 8n-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8n-bit wide, four-clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

### Features

- VDD = VDDQ = 1.2V  $\pm$ 60mV
- VPP = 2.5V, -125mV, +250mV
- On-die, internal, adjustable VREFDQ generation
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability

### Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A916G16A6CHOC	1024M X 16	DDR4-2133MHz 15-15-15	96Ball BGA, 10x13mm	Commercial
H2A916G16A6CIOC	1024M X 16	DDR4-2400MHz 17-17-17	96Ball BGA, 10x13mm	Commercial
H2A916G16A6CJOC	1024M X 16	DDR4-2666MHz 19-19-19	96Ball BGA, 10x13mm	Commercial

**Note:** Speed (tck\*) is in order of CL-T<sub>RCD</sub>-T<sub>RP</sub>

### Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDDQ	VSSQ	DQ8	<b>A</b>	UDQS_c	VSSQ	VDDQ
VPP	VSS	VDD	<b>B</b>	UDQS_t	DQ9	VDD
VDDQ	DQ12	DQ10	<b>C</b>	DQ11	DQ13	VSSQ
VDD	VSSQ	DQ14	<b>D</b>	DQ15	VSSQ	VDDQ
VSS	NF/UDM_n /UDBI_n	VSSQ	<b>E</b>	NF/LDM_n /LDBI_n	VSSQ	VSS
VSSQ	VDDQ	LDQS_c	<b>F</b>	DQ1	VDDQ	ZQ
VDDQ	DQ0	LDQS_t	<b>G</b>	VDD	VSS	VDDQ
VSSQ	DQ4	DQ2	<b>H</b>	DQ3	DQ5	VSSQ
VDD	VDDQ	DQ6	<b>J</b>	DQ7	VDDQ	VDD
VSS	CKE	ODT	<b>K</b>	CK_t	CK_c	VSS
VDD	WE_n/A14	ACT_n	<b>L</b>	CS_n	RAS_n/A16	VDD
VREFCA	BG0	A10/AP	<b>M</b>	A12/BC_n	CAS_n/A15	VSS
VSS	BA0	A4	<b>N</b>	A3	BA1	TEN
RESET_n	A6	A0	<b>P</b>	A1	A5	ALERT_n
VDD	A8	A2	<b>R</b>	A9	A7	VPP
VSS	A11	PAR	<b>T</b>	NC	A13	VDD

**96-Ball FBGA – x16 Ball Descriptions**

Pin	Symbol	Description
Input	A[17:0]	<b>(Address inputs)</b> Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts.
Input	A10/AP	<b>(Auto precharge)</b> A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
Input	A12/BC_n	<b>(Burst chop)</b> A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
Input	ACT_n	<b>(Command input)</b> ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
Input	BA[1:0]	<b>(Bank address inputs)</b> Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
Input	BG[1:0]	<b>(Bank group address inputs)</b> Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration

**96-Ball FBGA – x16 Ball Descriptions (Continued)**

Pin	Symbol	Description
Input	C0/CKE1, C1/CS1_n, C2/ODT1	<b>(Stack address inputs)</b> These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
Input	CK_t, CK_c	<b>(Clock)</b> Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
Input	CKE	<b>(Clock enable)</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
Input	CS_n	<b>(Chip select)</b> All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
Input	DM_n, UDM_n LDM_n	<b>(Input data mask)</b> DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section.
Input	ODT	<b>(On-die termination)</b> ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, UDQS_t, UDQS_c, LDQS_t, LDQS_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable RTT.

**96-Ball FBGA – x16 Ball Descriptions (Continued)**

Pin	Symbol	Description
Input	PAR	<b>(Parity for command and address)</b> This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
Input	RAS_n/A16, CAS_n/A15, WE_n/A14	<b>(Command inputs)</b> RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
Input	RESET_n	<b>(Active LOW asynchronous reset)</b> Reset is active when RESET_n is LOW, and inactive when RESET_n HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD (960 mV for DC HIGH and 240 mV for DC LOW).
Input	TEN	<b>(Connectivity test mode)</b> TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW).
I/O	DQ	<b>(Data input/output)</b> Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] the x4, x8, and x16 configurations, respectively. If write CRC is Enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal VREF level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the RTT value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin
I/O	DBI_n, UDBI_n, LDBI_n	<b>(DBI input/output)</b> Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.

**96-Ball FBGA – x16 Ball Descriptions (Continued)**

Type	Symbol	Description
I/O	DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	<b>(Data strobe)</b> Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
Output	ALERT_n	<b>(Alert output)</b> This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/ address parity error and the CRC data error when either of these functions is enabled in the mode register.
Output	TDQS_t, TDQS_c	<b>(Termination data strobe)</b> TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function may be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
Supply	VDD	Power supply: 1.2V $\pm$ 0.060V.
Supply	VDDQ	DQ power supply: 1.2V $\pm$ 0.060V.
Supply	VPP	DRAM activating power supply: 2.5V $-0.125V/+0.250V$ .
Supply	VREFCA	Reference voltage for control, command, and address pins.
Supply	VSS	Ground.
Supply	VSSQ	DQ ground.
Reference	ZQ	Reference ball for ZQ calibration: This ball is tied to an external 240 $\Omega$ resistor (RZQ), which is tied to VSSQ.
-	RFU	Reserved for future use.
-	NC	No connect: No internal electrical connection is present.
-	NF	No function: May have internal connection present but has no function.

### Absolute Maximum Ratings

Symbol	Item	Rating	Units
VIN, VOUT	Input, Output Voltage	-0.4 ~ +1.5	V
VDD	Power Supply Voltage	-0.4 ~ +1.5	V
VDDQ	Power Supply Voltage	-0.4 ~ +1.5	V
VPP	Power Supply Voltage	-0.4 ~ +3.0	V
TOP	Operating Temperature Range	Commercial	0 ~ +85
TSTG	Storage Temperature Range	-55 ~ +150	°C

**Note:** Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Supply voltage	1.14	1.2	1.26	V
V <sub>DDQ</sub>	Supply voltage for output	1.14	1.2	1.26	V
V <sub>PP</sub>	Wordline supply voltage	2.375	2.5	2.750	V

### VDD Slew Rate

Symbol	Min.	Max.	Units	Notes
V <sub>DD_sl</sub>	0.004	600	V/ms	1,2
V <sub>DD_on</sub>	-	200	ms	3

**Notes1:** Measurement made between 300mV and 80% VDD (minimum level).

**Notes2:** The DC bandwidth is limited to 20 MHz.

**Notes3:** Maximum time to ramp VDD from 300 mV to VDD minimum.

## Input/ Output Capacitance

Symbol	Parameters	Min.	Max.	Unit	Notes
CCK	Input capacitance	0.2	0.8	pF	2,3
CDCK	Input capacitance delta	0	0.05	pF	2,3,6
CDI_CTRL	Input capacitance delta	-0.1	0.1	pF	2,3,8,9
CDI_ADD_CMD	Input capacitance delta	-0.1	0.1	pF	1,2,10,11
CIO	Input/output capacitance	0.55	1.4	pF	1,2,3
CI	Input capacitance	0.2	0.8	pF	2,3,4
CDIO	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,4
CDDQS	Input/output capacitance delta	0	0.05	pF	2,3,5
CALERT	Input/output capacitance	0.5	1.5	pF	2,3
CZQ	Input/output pin capacitance, ZQ	-	2.3	pF	2,3,12
CTEN	Input/output capacitance	0.2	2.3	pF	2,3,13

**Notes1:** Although the DM, TDQS\_t, and TDQS\_c pins have different functions, the loading matches DQ and DQS.

**Notes2:** This parameter is not subject to a production test; it is verified by design and characterization.

The capacitance is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with VDD, VDDQ, VSS, and VSSQ applied and all other pins floating (except the pin under test, CKE, RESET\_n and ODT, as necessary). VDD = VDDQ = 1.5V, VBIAS = VDD/2 and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.

**Notes3:** This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.

**Notes4:**  $CDIO = CIO(DQ, DM) - 0.5 \times (CIO(DQS\_t) + CIO(DQS\_c))$ .

**Notes5:** Absolute value of CIO (DQS\_t), CIO (DQS\_c)

**Notes6:** Absolute value of CCK\_t, CCK\_c

**Notes7:** CI applies to ODT, CS\_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS\_n, CAS\_n, ACT\_n, PAR and WE\_n.

**Notes8:** CDI\_CTRL applies to ODT, CS\_n, and CKE.

**Notes9:**  $CDI\_CTRL = CI(CTRL) - 0.5 \times (CI(CLK\_t) + CI(CLK\_c))$ .

**Notes10:** CDI\_ADD\_CMD applies to A[17:0], BA[1:0], BG[1:0], RAS\_n, CAS\_n, ACT\_n, PAR and WE\_n.

**Notes11:**  $CDI\_ADD\_CMD = CI(ADD\_CMD) - 0.5 \times (CI(CLK\_t) + CI(CLK\_c))$ .

**Notes12:** Maximum external load capacitance on ZQ pin: 5pF.

**Notes13:** Only applicable if TEN pin does not have an internal pull-up.

**DRAM Package Electrical Specifications**

Parameters		Symbol	Min.	Max.	Unit	Notes
Input/ output	Zpkg	ZIO	45	85	ohm	1,2,4
	Package delay	TdIO	14	42	ps	1,3,4
	Lpkg	LIO	-	3.3	nH	11
	Cpkg	CIO	-	0.78	pF	11
LDQS_t/ LDQS_c/ UDQS_t/ UDQS_c	Zpkg	ZIO DQS	45	85	ohm	1,2
	Package delay	TdIO DQS	14	42	ps	1,3
	Lpkg	LIO DQS	-	3.3	nH	11
	Cpkg	CIO DQS	-	0.78	pF	11
LDQS_t/ LDQS_c, UDQS_t/ UDQS_c,	Delta Zpkg	DZIO DQS	-	10	ohm	1,2,6
	Delta delay	DTDIO DQS	-	5	ps	1,3,6
Input CTRL pins	Zpkg	ZI CTRL	50	90	ohm	1,2,8
	Package delay	TdI CTRL	14	42	ps	1,3,8
	Lpkg	LI CTRL	-	3.4	nH	11
	Cpkg	CI CTRL	-	0.7	pF	11
Input CMD ADD pins	Zpkg	ZI ADD CMD	50	90	ohm	1,2,7
	Package delay	TdI ADD CMD	14	45	ps	1,3,7
	Lpkg	LI ADD CMD	-	3.6	nH	11
	Cpkg	CI ADD CMD	-	0.74	pF	11

**DRAM Package Electrical Specifications(Continued)**

Parameters		Symbol	Min.	Max.	Unit	Notes
CK_t, CK_c	Zpkg	ZCK	50	90	ohm	1,2
	Package delay	TdCK	14	42	ps	1,3
	Package delay	DZDCK	-	10	ohm	1,2,5
	Delta delay	DTdDCK	-	5	ps	1,3,5
Input CLK	Lpkg	LI CLK	-	3.4	nH	11
	Cpkg	CI CLK	-	0.7	pF	11
ZQ Zpkg		ZO ZQ	-	100	ohm	1,2
ZQ delay		TdO ZQ	20	90	ps	1,3
ALERT Zpkg		ZO ALERT	40	100	ohm	1,2
ALERT delay		TdO ALERT	20	55	ps	1,3

**Notes1:** The package parasitic (L and C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, and VSSQ shorted with all other signal pins floating.

The inductance is measured with VDD, VDDQ, VSS, and VSSQ shorted and all other signal pins shorted at the die, not pin, side.

**Notes2:** Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).

**Notes3:** Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Td/pkg (total per pin) = SQRT (Lpkg × Cpkg).

**Notes4:** ZIO and TdIO apply to DQ, DM, TDQS\_t and TDQS\_c.

**Notes5:** Absolute value of ZCK\_t, ZCK\_c for impedance (Z) or absolute value of TdCK\_t, TdCK\_c for delay (Td).

**Notes6:** Absolute value of ZIO (DQS\_t), ZIO (DQS\_c) for impedance (Z) or absolute value of TdIO (DQS\_t), TdIO (DQS\_c) for delay (Td).

**Notes7:** ZI ADD CMD and TdI ADD CMD apply to A[17:0], BA[1:0], BG[1:0], RAS\_n CAS\_n, and WE\_n.

**Notes8:** ZI CTRL and TdI CTRL apply to ODT, CS\_n, and CKE.

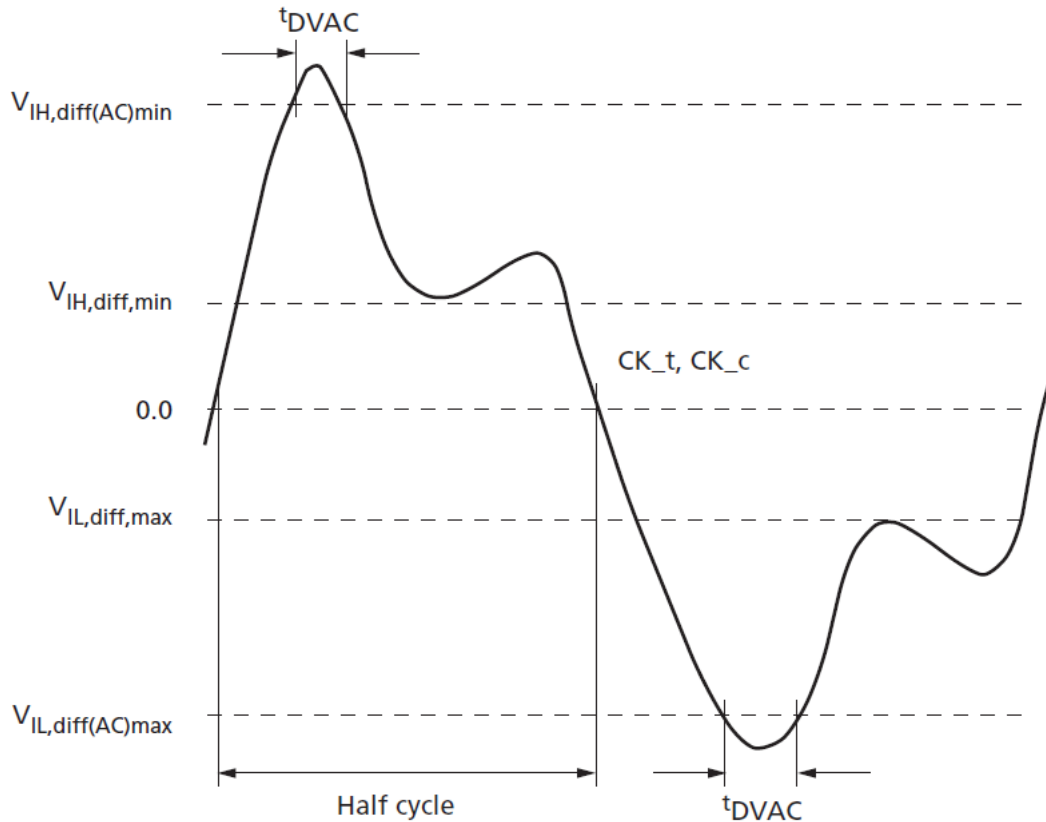
**Notes9:** Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.

**Notes10:** It is assumed that Lpkg can be approximated as  $Lpkg = ZO \times Td$ .

**Notes11:** It is assumed that Cpkg can be approximated as  $Cpkg = Td/ZO$ .

## AC and DC Differential Input Measurement Levels

### Differential Inputs



### Differential Input Swing Requirements for CK\_t, CK\_c

Symbol	Parameter	Min.	Max.	Units	Note
V <sub>IHdiff</sub>	Differential input high	+0.15	See <b>Note3</b>	V	1
V <sub>ILdiff</sub>	Differential input low	See <b>Note3</b>	-0.15	V	1
V <sub>IHdiff (AC)</sub>	AC Differential input high	2x(V <sub>IH(AC)</sub> -V <sub>REF</sub> )	See <b>Note3</b>	V	2
V <sub>ILdiff (AC)</sub>	AC Differential input low	See <b>Note3</b>	2x(V <sub>REF</sub> -V <sub>IL(AC)</sub> )	V	2

**Note1:** Used to define a differential signal slew-rate.

**Note2:** For CK\_t, CK\_c use V<sub>IH(AC)</sub> and V<sub>IL(AC)</sub> of ADD/CMD and V<sub>REFCA</sub>.

**Note3:** These values are not defined; however, the differential signals (CK\_t, CK\_c) need to be within the respective limits, V<sub>IH(DC)</sub>max and V<sub>IL(DC)</sub>min for single-ended signals as well as the limitations for overshoot and undershoot..

Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

Minimum Time AC Time tDVAC for CK

Slew Rate [V/ns]	tDVAC (ps) at [VIH,diff(AC) to VIL,diff(AC)]	
	200mV	TBDmV
>4.0	120	TBD
4.0	115	TBD
3.0	110	TBD
2.0	105	TBD
1.8	100	TBD
1.6	95	TBD
1.4	90	TBD
1.2	85	TBD
1.0	80	TBD
<1.0	80	TBD

**Note:** Below VIL(AC).

Single-Ended Requirements for CK Differential Signals

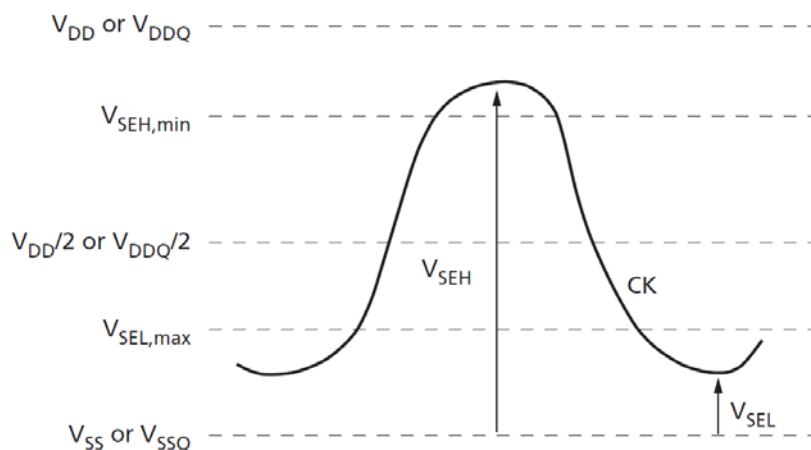
Each individual component of a differential signal (CK, DQS, /CK, /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(AC) / VIL(AC) ) for Address/Command signals) in every half-cycle.

DQS, /DQS have to reach VSEHmin / VSELmax [approximately the ac-levels (VIH(AC) / VIL(AC) ) for DQ signals] in every half-cycle preceding and following a valid transition.

Note that the applicable AC-levels for Address/Command and DQ's might be different per speed-bin etc. E.g., if VIHCA(AC150)/VILCA(AC150) is used for Address/Command signals, then these AC-levels apply also for the single-ended components of differential CK and /CK.

Single-Ended Requirements for CK



### Single-Ended Requirements for CK

Symbol	Parameter	Min.	Max.	Units	Note
VSEH	Single-ended high-level for CK, /CK	$(VDD/2)+0.1$	See <b>Note3</b>	V	1,2
VSEL	Single-ended low-level for CK, /CK	See <b>Note3</b>	$(VDD/2)-0.1$	V	1,2

**Note1:** For CK\_t, CK\_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

**Note2:** ADDR/CMD VIH(AC) and VIL(AC) based on VREFCA.

**Note3:** These values are not defined; however, the differential signal (CK\_t, CK\_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

### AC and DC Output Measurement Levels

Symbol	Parameter	Specification	Units	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	$1.1 \cdot VDDQ$	V	1
VOM(DC)	DC output middle measurement level (for IV curve linearity)	$0.8 \cdot VDDQ$	V	1
VOL(DC)	DC output low measurement level (for IV curve linearity)	$0.5 \cdot VDDQ$	V	1
VOH(AC)	AC output high measurement level (for output slew rate)	$(0.7+0.15) \cdot VDDQ$	V	1
VOL(AC)	AC output low measurement level (for output slew rate)	$(0.7-0.5) \cdot VDDQ$	V	1
VOHdiff(AC)	AC differential output high measurement level (for output slew rate)	$0.3 \cdot VDDQ$	V	2
VOLdiff(AC)	AC differential output low measurement level (for output slew rate)	$-0.3 \cdot VDDQ$	V	2

**Notes1:** The swing of  $\pm 0.15 \times VDDQ$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of  $RZQ/7$  and an effective test load of  $50\Omega$  to  $VTT = VDDQ$ .

**Notes2:** The swing of  $\pm 0.3 \times VDDQ$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of  $RZQ/7$  and an effective test load of  $50\Omega$  to  $VTT = VDDQ$  at each differential output.

### Recommended DC Operating Conditions

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2666	2400	2133	Units
		Max			
I <sub>DD0</sub>	<b>Operating One Bank Active-Precharge Current (AL = 0)</b> CKE: HIGH; External clock: On; tCK, nRC, nRAS, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: VDDQ; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the IDD0 Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	76	75	74	mA
I <sub>PP0</sub>	<b>Operating One Bank Active-Precharge IPP Current (AL = 0)</b> Same conditions as IDD0 above	5	5	5	mA
I <sub>DD1</sub>	<b>Operating One Bank Active-Read-Precharge Current (AL = 0)</b> CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, CL: see the previous table; BL: 8;1, 5 AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the IDD1 Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the following table); Output buffer and RTT: enabled in mode registers;2 ODT Signal stable at 0	97	96	95	mA
I <sub>DD2P</sub>	<b>Precharge Power-Down Current</b> CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	43	43	43	mA
I <sub>DD2N</sub>	<b>Precharge Standby Current (AL = 0)</b> CKE: HIGH; External clock: On; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0; Pattern details: see the IDD2N and IDD3N Measurement-Loop Pattern table	50	49	48	mA

**Recommended DC Operating Conditions(Continued)**

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2666	2400	2133	Units
		Max			
I <sub>DD3P</sub>	<b>Active Power-Down Current (AL = 0)</b> CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	70	69	68	mA
I <sub>DD3N</sub>	<b>Active Standby Current (AL = 0)</b> CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and	3	3	3	mA
I <sub>DD4R</sub>	<b>Operating Burst Read Current (AL = 0)</b> CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS_n: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4R Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the IDD4R Measurement-Loop Pattern table; DM_n stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the IDD4R Measurement-Loop pattern table); Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	284	262	242	mA
I <sub>DD4W</sub>	<b>Operating Burst Write Current (AL = 0)</b> CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4W Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the IDD4W Measurement-Loop Pattern table; DM: stable at 0; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see IDD4W Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers (see note2); ODT signal: stable at HIGH	240	223	209	mA

**Recommended DC Operating Conditions(Continued)**

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2666	2400	2133	Units
		Max			
I <sub>DD5R</sub>	<b>Burst Refresh Current (1X REF)</b> CKE: HIGH; External clock: on; tCK, CL, nREFI: see the previous table; BL: 8;1 AL: 0; CS <sub>n</sub> : HIGH between REF;Command, address, bank group address, bank address inputs: partially toggling according to the IDD5R Measurement-Loop Pattern table; Data I/O: VDDQ; DM <sub>n</sub> : stable at 1; Bank activity: REF command every nREFI (see the IDD5R Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers2; ODT signal:stable at 0	81	81	81	mA
I <sub>PP5R</sub>	<b>Burst Refresh Current (1X REF)</b> Same conditions as IDD5R above	5	5	5	mA
I <sub>DD6N</sub>	<b>Self Refresh Current: Normal Temperature Range</b> TC: 0–85°C; Auto self refresh (ASR): disabled;3 Self refresh temperature range (SRT): normal;4 CKE: LOW; External clock: off; CK <sub>t</sub> and CK <sub>c</sub> : LOW; CL: see the table above; BL: 8;1 AL: 0; CS <sub>n</sub> , command, address, bank group address, bank address, data I/O: VDDQ; DM <sub>n</sub> : stable at 1; Bank activity: SELF REFRESH operation ;Output buffer and RTT: enabled in mode registers;2 ODT signal: midlevel	74	74	74	mA
I <sub>PP6N</sub>	<b>Self Refresh IPP Current: Normal Temperature Range</b> Same conditions as IDD6N above	9	9	9	mA
I <sub>DD7</sub>	<b>Operating Bank Interleave Read Current</b> CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8;15 AL: CL -1; CS <sub>n</sub> : HIGH between ACT and RDA; Command, address, group bank address, bank address inputs: partially toggling according to the IDD7 Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the IDD7 Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the IDD7 Measurement-Loop Pattern table; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	260	255	255	mA

**Recommended DC Operating Conditions(Continued)**

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	2666	2400	2133	Units
		Max			
I <sub>PP7</sub>	<b>Operating Bank Interleave Read IPP Current</b> Same conditions as IDD7 above	11	11	11	mA
I <sub>DD8</sub>	<b>Maximum Power Down Current</b> Place DRAM in MPSM then CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n:stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; 2 ODT signal: stable at 0	40	40	40	mA

**Note 1:** Burst length: BL8 fixed by MRS: set MR0[1:0] 00.

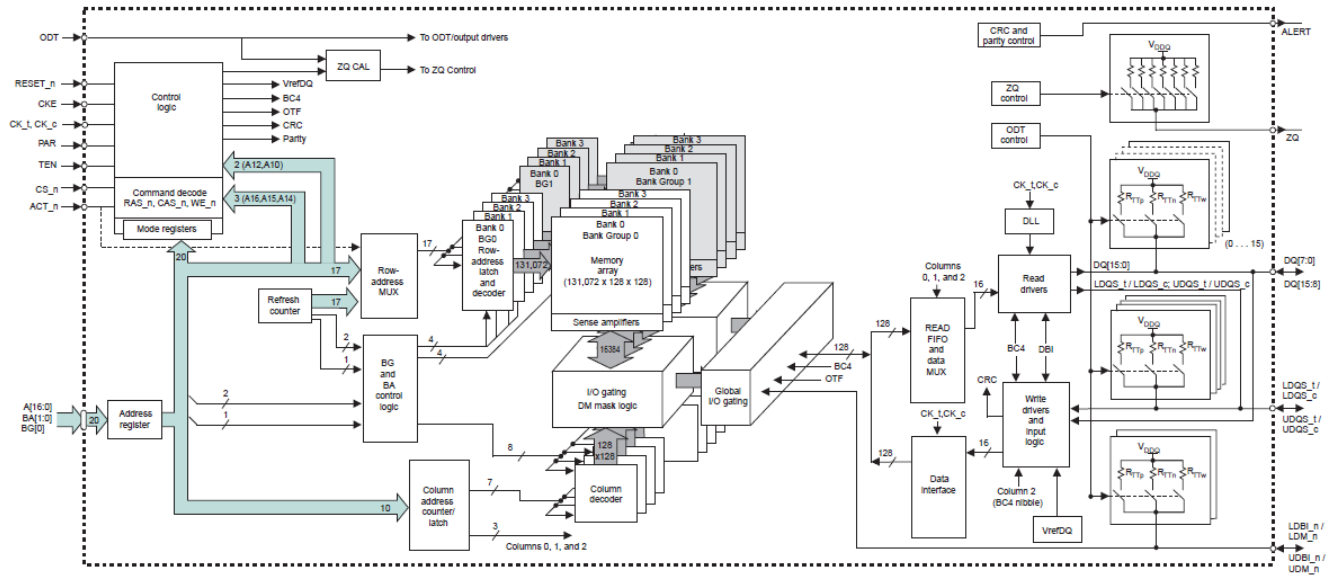
**Note 2:** Output buffer enable: set MR1[12] 0 (output buffer enabled); set MR1[2:1] 00 (RON = RZQ/7); RTT(NOM) enable: set MR1[10:8] 011 (RZQ/6); RTT(WR) enable: set MR2[11:9] 001(RZQ/2), and RTT(Park) enable: set MR5[8:6] 000 (disabled).

**Note 3:** Auto self refresh (ASR): set MR2[6] 0 to disable or MR2[6] 1 to enable feature.

**Note 4:** Self refresh temperature range (SRT): set MR2[7] 0 for normal or MR2[7] 1 for extended temperature range.

**Note 5:** READ burst type: Nibble sequential, set MR0[3] 0.

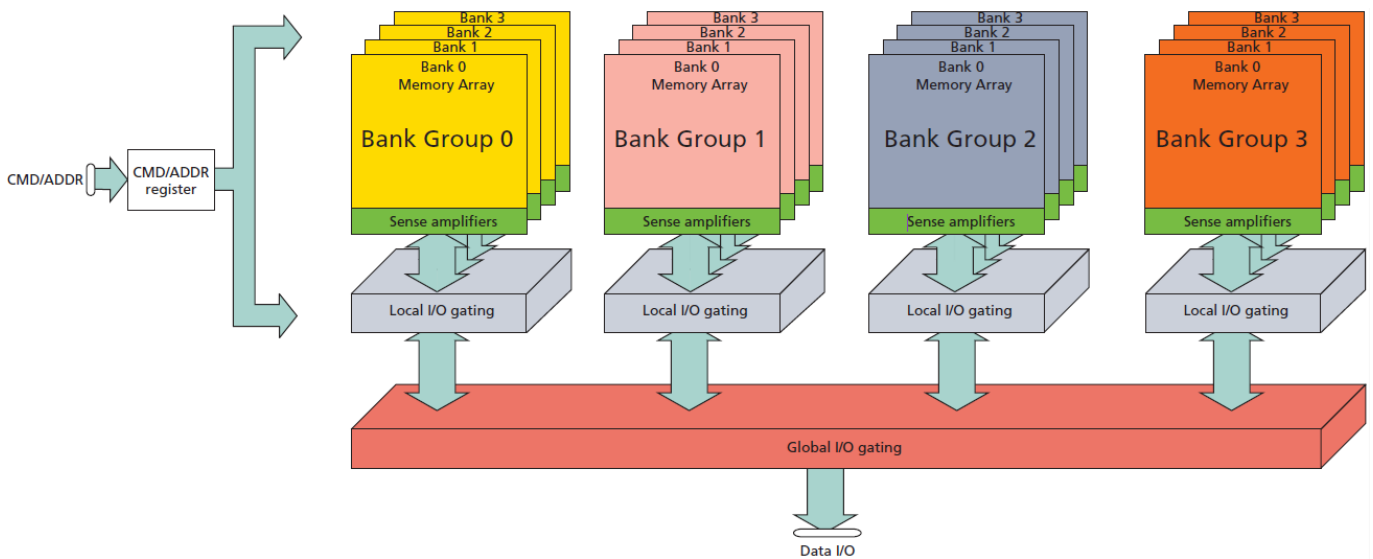
## Functional Block Diagram



## Bank Access Operation

DDR4 supports bank grouping: x4/x8 DRAMs have four bank groups (BG[1:0]), and each bank group is comprised of four subbanks (BA[1:0]); x16 DRAMs have two bank groups (BG[0]), and each bank group is comprised of four subbanks. Bank accesses to different banks' groups require less time delay between accesses than bank accesses to within the same bank's group. Bank accesses to different bank groups require tCCD\_S (or short) delay between commands while bank accesses within the same bank group require tCCD\_L (or long) delay between commands.

### Bank Group x4/x8 Block Diagram



**Note 1:** Bank accesses to different bank groups require tCCD\_S.

**Note 2:** Bank accesses within the same bank group require tCCD\_L.

### Refresh Parameters

Parameter	Symbol	16Gb	Unit	Notes	
REF command to ACT or REF command time	tRFC (All bank groups)	350	ns	-	
Average periodic refresh interval	tREFI	0°C ≤ TC ≤ 85°C	7.8	μs	-
		0°C < TC ≤ 95°C	3.9	μs	*

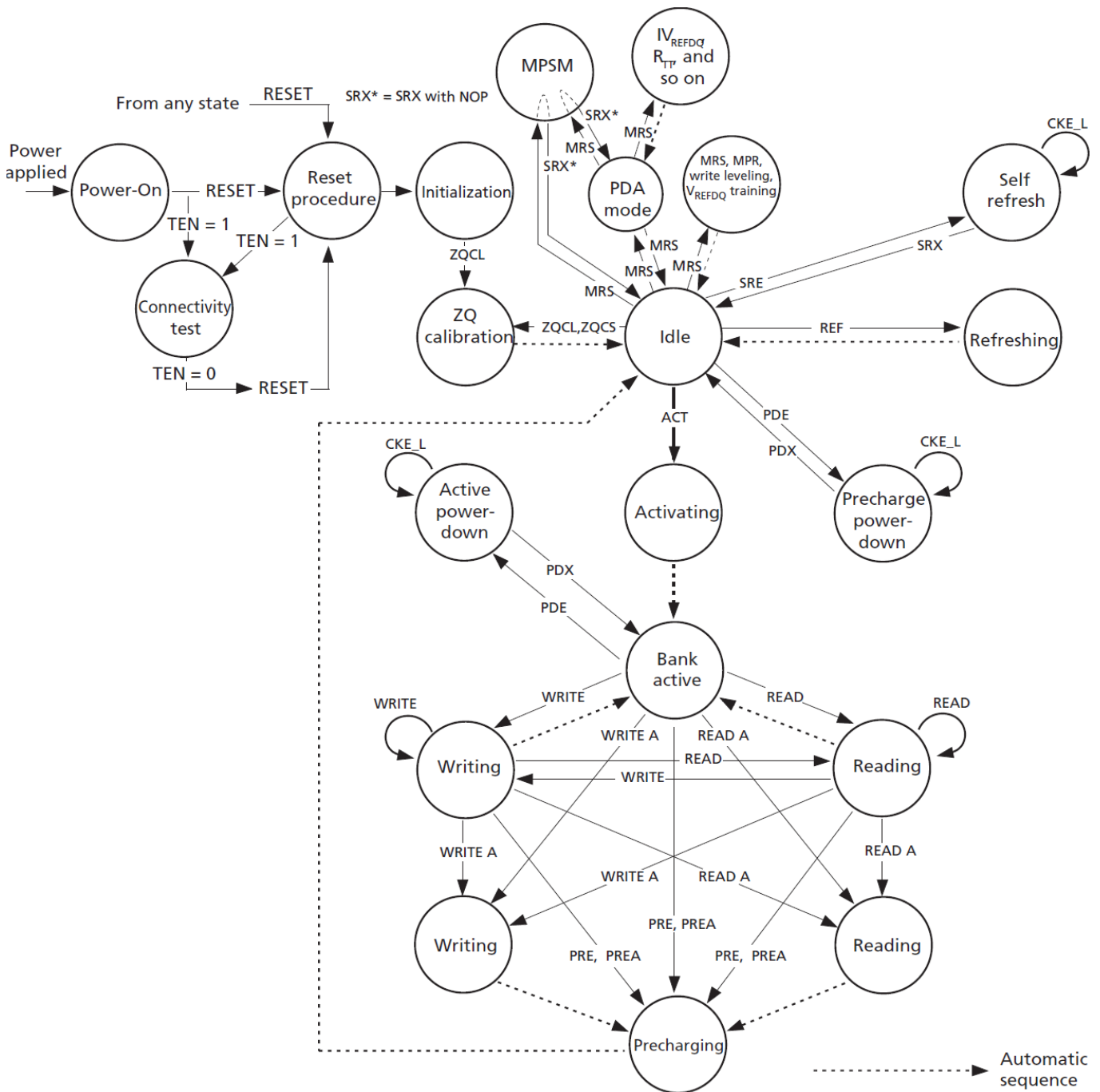
**Note:** Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

**AC Operating Test Characteristics**
**DDR4-2133 & 2400 & 2666 Speed Bins**

VDD = VDDQ = 1.2V ±60mV

Symbol	Speed Bin		(DDR4-2666)		(DDR4-2400)		(DDR4-2133)		Units
	CL-nRCD-nRP		19-19-19		17-17-17		15-15-15		
	Parameter		Min.	Max.	Min.	Max.	Min.	Max.	
tAA	Internal read command to first data		14.25	19	14.16	19	14.06	19	ns
tRCD	Active to read or write delay		14.25	-	14.16	-	14.06	-	ns
tRP	Precharge command period		14.25	-	14.16	-	14.06	-	ns
tRC	Active to active/auto refresh command		tRAS+tRP	-	tRAS+tRP	-	tRAS+tRP	-	ns
tRAS	Active to precharge command period		32	9xtREFI	32	9xtREFI	33	9xtREFI	ns
READ: nonDBI	READ: DBI	WRITE	Min.	Max.	Min.	Max.	Min.	Max.	Units
CL=9	CL=11	CWL=9	Reserved		Reserved		1.5	1.9	ns
CL=10	CL=12	CWL=9	1.5	1.9	1.5	1.9	1.5	1.9	ns
CL=11	CL=13	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=12	CL=14	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=13	CL=15	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=14	CL=16	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=15	CL=18	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=16	CL=19	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=17	CL=20	CWL=12,16	0.833	<0.937	0.833	<0.937	-	-	ns
CL=18	CL=21	CWL=12,16	0.833	<0.937	0.833	<0.937	-	-	ns
CL=19	CL=22	CWL=14,18	0.750	<0.833	-	-	-	-	ns
CL=20	CL=23	CWL=14,18	0.750	<0.833	-	-	-	-	ns
Support CL Settings			10-20		10-18		9-16		nCK
Support CL settings with read DBI			12-16, 18-23		12-16, 18-21		11-16,18,19		nCK
Support CWL Settings			9-12, 14,16,18		9-12, 14,16		9,10,11,12,14		nCK

Simplified State Diagram



**Command Truth Table**

Command	Symbol	Prev. CKE	Pres. CKE	CS <sub>n</sub>	ACT <sub>n</sub>	RAS <sub>n</sub> /A16	CAS <sub>n</sub> /A15	WE <sub>n</sub> /A14	BG[1:0]	BA [1:0]	C[2:0]	A12/BC <sub>n</sub>	A[13,11]	A10/AP	A[9:0]	Notes
MODE REGISTER SET	MRS	H	H	L	H	L	L	L	BG	BA	V	V	V	OP code	V	7
REFRESH	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	8, 9, 10
Self refresh entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	8, 9, 10, 11
Self refresh exit	SRX	L	H	H	X	X	X	X	V	V	V	V	V	V	V	
Single-bank PRECHARGE	PRE	H	H	L	H	L	L	L	BG	BA	V	V	V	L	V	
PRECHARGE all banks	PREA	H	H	L	H	L	L	L	V	V	V	V	V	H	V	
Reserved for future use	RFU	H	H	L	H	L	L	H								
Bank ACTIVATE	ACT	H	H	L	L	L	L	H	BG	BA	V	V	V	Row address (RA)	V	
WRITE	BL8 fixed, BC4 fixed	H	H	L	H	L	L	L	BG	BA	V	V	V	L	CA	
	BC4OTF	H	H	L	H	L	L	L	BG	BA	V	L	V	L	CA	
	BL8OTF	H	H	L	H	L	L	L	BG	BA	V	H	V	L	CA	
WRITE with auto precharge	BL8 fixed, BC4 fixed	H	H	L	H	L	L	L	BG	BA	V	V	V	H	CA	
	BC4OTF	H	H	L	H	L	L	L	BG	BA	V	L	V	H	CA	
READ	BL8OTF	H	H	L	H	L	L	L	BG	BA	V	H	V	H	CA	
	BL8 fixed, BC4 fixed	H	H	L	H	L	L	H	BG	BA	V	V	V	L	CA	
	BC4OTF	H	H	L	H	L	L	H	BG	BA	V	L	V	L	CA	
READ with auto precharge	BL8OTF	H	H	L	H	L	L	L	BG	BA	V	H	V	H	CA	
	BC4OTF	H	H	L	H	L	L	L	BG	BA	V	L	V	H	CA	
NO OPERATION	NOP	H	H	L	H	L	L	H	V	V	V	V	V	V	V	12
Device DESELECTED	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	13
Power-down entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
Power-down exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
ZQ CALIBRATION LONG	ZQCL	H	H	L	H	L	L	L	X	X	X	X	X	H	X	
ZQ CALIBRATION SHORT	ZQCS	H	H	L	H	L	L	L	X	X	X	X	X	L	X	

- Note1:** BG = Bank group address, BA = Bank address, RA = Row address, CA = Column address, BC\_n = Burst chop, X = "Don't Care", V = Valid
- Note2:** All DDR4 SDRAM commands are defined by states of CS\_n, ACT\_n, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, and CKE at the rising edge of the clock. The MSB of BG, BA, RA, and CA are device density- and configuration-dependent. When ACT\_n = H, pins RAS\_n/A16, CAS\_n/A15, and WE\_n/A14 are used as command pins RAS\_n, CAS\_n, and WE\_n, respectively. When ACT\_n = L, pins RAS\_n/A16, CAS\_n/A15, and WE\_n/A14 are used as address pins A16, A15, and A14, respectively.
- Note3:** RESET\_n is enabled LOW and is used only for asynchronous reset and must be maintained HIGH during any function.
- Note4:** Bank group addresses (BG) and bank addresses (BA) determine which bank within a bank group is being operated upon. For MRS commands, the BG and BA selects the specific mode register location.
- Note5:** V means HIGH or LOW (but a defined logic level), and X means either defined or undefined (such as floating) logic level.
- Note6:** READ or WRITE bursts cannot be terminated or interrupted, and fixed/on-the-fly (OTF) BL will be defined by MRS.
- Note7:** During an MRS command, A17 is RFU and is device density- and configuration-dependent.
- Note8:** The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
- Note9:** VPP and VREF (VREFCA) must be maintained during SELF REFRESH operation.
- Note10:** Refer to the Truth Table – CKE table for more details about CKE transition.
- Note11:** Controller guarantees self refresh exit to be synchronous. DRAM implementation has the choice of either synchronous or asynchronous.
- Note12:** The NO OPERATION (NOP) command may be used only when exiting maximum power saving mode or when entering gear-down mode.
- Note13:** The NOP command may not be used in place of the DESELECT command.
- Note14:** The power-down mode does not perform any REFRESH operation.

## CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18

**Note1:** CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

**Note2:** Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.

**Note3:** Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.

**Note4:** All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

**Note5:** The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

**Note6:** During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

**Note7:** DESELECT and NOP are defined in the "Command Truth Table".

**Note8:** On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

**Note9:** Self-Refresh mode can only be entered from the All Banks Idle state.

**Note10:** Must be a legal command as defined in the "Command Truth Table".

**Note11:** Valid commands for power-down entry and exit are NOP and DESELECT only.

**Note12:** Valid commands for self-refresh exit are NOP and DESELECT only.

**Note13:** Self-Refresh can not be entered during Read or Write operations.

**Note14:** The Power-Down does not perform any refresh operations.

**Note15:** "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

**Note16:** VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh.operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.

**Note17:** If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

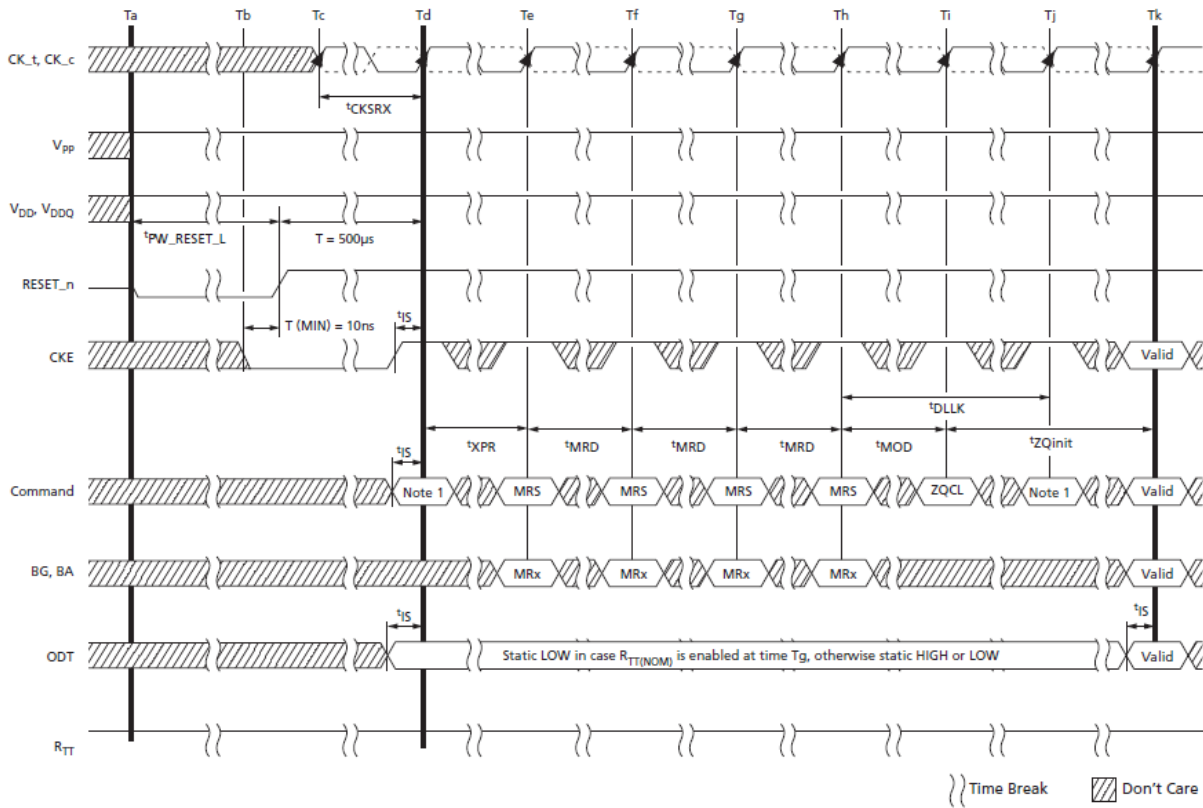
**Note18:** 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

## Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below  $0.2 \times VDD$ ; all other inputs may be undefined). /RESET needs to be maintained for minimum 700 us with stable power. CKE is pulled "Low" anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to  $VDD_{min}$  must be no greater than 200 ms; and during the ramp,  $VDD > VDDQ$  and  $(VDD - VDDQ) < 0.3$  volts.
  - VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
  - Vref tracks  $VDDQ/2$ . OR
  - Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT\_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ( $tXPR = \max(tXS ; 5 \times tCK)$ )
6. Issue MRS command to load MR3 with all application settings, wait tMRD.
7. Issue MRS command to load MR6 with all application settings, wait tMRD.
8. Issue MRS command to load MR5 with all application settings, wait tMRD.
- 9 Issue MRS command to load MR4 with all application settings, wait tMRD.
10. Issue MRS command to load MR2 with all application settings, wait tMRD.
11. Issue MRS command to load MR1 with all application settings, wait tMRD.
12. Issue MRS command to load MR0 with all application settings, wait tMOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for tDLLK and tZQinit to complete.

**Reset and Power up initialization sequence**



**Note 1:** From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.

**Note 2:** MRS commands must be issued to all mode registers that have defined settings.

**Note 3:** In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).

**Note 4:** TEN is not shown; however, it is assumed to be held LOW.

## Mode Register Definition

### Mode Register MR0

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**Note:** RAS\_n, CAS\_n, and WE\_n must be LOW during MODE REGISTER SET command.

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> <b>000 = MR0</b> 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	<b>N/A on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
13,11:9	<b>WR (WRITE recovery)/RTP (READ-to-PRECHARGE)</b> 0000 = 10 / 5 clocks <sup>1</sup> 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks <sup>1</sup> 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks <sup>1</sup> 0101 = 20 / 10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks <sup>1</sup> 1000 = 26 / 13 clocks <sup>1</sup> 1001 = 28 / 14 clocks <sup>2</sup> 1010 through 1111 = Reserved

Mode Register	Description
8	<b>DLL reset</b> 0 = No 1 = Yes
7	<b>Test mode (TM) – Manufacturer use only</b> 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	<b>CAS latency (CL) – Delay in clock cycles from the internal READ command to first data-out</b> 00000 = 9 clocks <sup>1</sup> 00001 = 10 clocks 00010 = 11 clocks <sup>1</sup> 00011 = 12 clocks 00100 = 13 clocks <sup>1</sup> 00101 = 14 clocks 00110 = 15 clocks <sup>1</sup> 00111 = 16 clocks 01000 = 18 clocks 01001 = 20 clocks 01010 = 22 clocks 01011 = 24 clocks 01100 = 23 clocks <sup>1</sup> 01101 = 17 clocks <sup>1</sup> 01110 = 19 clocks <sup>1</sup> 01111 = 21 clocks <sup>1</sup> 10000 = 25 clocks (3DS use only) 10001 = 26 clocks 10010 = 27 clocks (3DS use only) 10011 = 28 clocks 10100 = 29 clocks <sup>1</sup> 10101 = 30 clocks 10110 = 31 clocks <sup>1</sup> 10111 = 32 clocks
3	<b>Burst type (BT) – Data burst ordering within a READ or WRITE burst access</b> 0 = Nibble sequential 1 = Interleave
1:0	<b>Burst length (BL) – Data burst size associated with each read or write access</b> 00 = BL8 (fixed) 01 = BC4 or BL8 (on-the-fly) 10 = BC4 (fixed) 11 = Reserved

**Note 1:** Not allowed when 1/4 rate gear-down mode is enabled.

**Note 2:** If WR requirement exceeds 28 clocks or RTP exceeds 14 clocks, WR should be set to 28 clocks and RTP should be set to 14 clocks.

### ***Burst Length, Type, and Order***

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC\_n.

### Burst Type (A3)

Burst Length	R/W	A2	A1	A0	Sequential Addressing	Interleave Addressing
BC4	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
BL8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

**Note1:** 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.

**Note2:** When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for tWR and tWTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4\_n) meaning that if the OTF MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.

**Note3:** T = Output driver for data and strobes are in High-Z.

V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.

X = "Don't Care."

### CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL):  $RL = AL + CL$ .

### Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer -defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7]= 1.

### DLL Reset

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, tDLLK must be met before functions requiring the DLL can be used, such as READ commands or synchronous ODT operations, for example,).

### Write Recovery

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine tDAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:  $WR (MIN) \text{ cycles} = \text{roundup}(tWR[ns]/tCK[ns])$ . The WR value must be programmed to be equal to or larger than tWR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; tWR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data. Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer:  $RTP (MIN) \text{ cycles} = \text{roundup}(tRTP[ns]/tCK[ns])$ . The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with tRP to determine the ACT timing to the same bank.

### Mode Register MR1

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> 000 = MR0 <b>001 = MR1</b> 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	<b>N/A on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
12	<b>Data output disable (Qoff) – Output buffer disable</b> 0 = Enabled (normal operation) 1 = Disabled (both ODI and $R_{TT}$ )
11	<b>Termination data strobe (TDQS) – Additional termination pins (x8 configuration only)</b> 0 = TDQS disabled 1 = TDQS enabled
10, 9, 8	<b>Nominal ODT (<math>R_{TT(NOM)}</math>) – Data bus termination setting</b> 000 = $R_{TT(NOM)}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
7	<b>Write leveling (WL) – Write leveling mode</b> 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)
13, 6, 5	<b>DQ RX EQ</b> Default = 000; Must be programmed to 000 unless otherwise stated 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
4, 3	<b>Additive latency (AL) – Command additive latency setting</b> 00 = 0 (AL disabled) 01 = CL - 1 <sup>1</sup> 10 = CL - 2 11 = Reserved
2, 1	<b>Output driver impedance (ODI) – Output driver impedance setting</b> 00 = RZQ/7 (34 ohm) 01 = RZQ/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm) 11 = Reserved
0	<b>DLL enable – DLL enable feature</b> 0 = DLL disabled 1 = DLL enabled (normal operation)

**Note:** Not allowed when 1/4 rate gear-down mode is enabled.

### ***DLL Enable/DLL Disable***

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when RTT(WR) is enabled and the DLL is required for proper ODT operation. The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT(NOM) bits MR1[9,6,2] = 000 via an MRS command during DLL off mode. The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set RTT(WR), MR2[10:9] = 00.

### ***ODT Rtt Values***

The device is capable of providing three different termination values: RTT(Park), RTT(NOM), and RTT(WR). The nominal termination value, RTT(NOM), is programmed in MR1. A separate value, RTT(WR), may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITE operations. The RTT(WR) value can be applied during WRITE commands even when RTT(NOM) is disabled. A third RTT value, RTT(Park), is programmed in MR5. RTT(Park) provides a termination value when the ODT signal is LOW.

### ***Additive Latency***

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

### **Additive Latency (AL) Settings**

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

**Note:** AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

### **Write Leveling**

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

### **Output Disable**

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

### **Termination Data Strobe**

Termination data strobe (TDQS) is a feature of the x8 device and provides additional termination resistance outputs that may be useful in some system configurations. Because this function is available only in a x8 configuration, it must be disabled for x4 and x16 configurations.

While TDQS is not supported in x4 or x16 configurations, the same termination resistance function that is applied to the TDQS pins is applied to the DQS pins when enabled via the mode register.

The TDQS, DBI, and DATA MASK (DM) functions share the same pin. When the TDQS function is enabled via the mode register, the DM and DBI functions are not supported. When the TDQS function is disabled, the DM and DBI functions can be enabled separately.

### **TDQS Function Matrix**

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	Enabled or disabled
	Disabled	Enabled	Enabled or disabled
	Disabled	Disabled	Enabled or disabled
Enabled	Disabled	Disabled	Disabled

## Mode Register MR2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**Note:** RAS\_n, CAS\_n, and WE\_n must be LOW during MODE REGISTER SET command.

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> 000 = MR0 001 = MR1 <b>010 = MR2</b> 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	<b>N/A on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
13	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
12	<b>WRITE data bus CRC</b> 0 = Disabled 1 = Enabled

Mode Register	Description
11:9	<b>Dynamic ODT (<math>R_{TT(WR)}</math>) – Data bus termination setting during WRITES</b> 000 = $R_{TT(WR)}$ disabled (WRITE does not affect $R_{TT}$ value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm) 101 = Reserved 110 = Reserved 111 = Reserved
7:6	<b>Low-power auto self refresh (LPASR) – Mode summary</b> 00 = Manual mode - Normal operating temperature range ( $T_C$ : 0°C–85°C) 01 = Manual mode - Reduced operating temperature range ( $T_C$ : 0°C–45°C) 10 = Manual mode - Extended operating temperature range ( $T_C$ : 0°C–95°C) 11 = ASR mode - Automatically switching among all modes
5:3	<b>CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1<sup>st</sup>CK WRITE preamble</b> 000 = 9 (DDR4-1600) <sup>1</sup> 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600) <sup>1</sup> 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	<b>CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2<sup>nd</sup>CK WRITE preamble</b> 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
1:0	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved

**Note:** Not allowed when 1/4 rate gear-down mode is enabled.

### CAS Write Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL):  $WL = AL + PL + CWL$ .

### Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the

dynamic ODT (RTT(WR)) settings in MR2[11:9]. In write leveling mode, only RTT(NOM) is available.

## Mode Register MR3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**Note:** RAS\_n, CAS\_n, and WE\_n must be LOW during MODE REGISTER SET command.

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> 000 = MR0 001 = MR1 010 = MR2 <b>011 = MR3</b> 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	<b>N/A on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
13	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
12:11	<b>Multipurpose register (MPR) – Read format</b> 00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
10:9	<b>WRITE CMD latency when CRC/DM enabled</b> 00 = 4CK (DDR4-1600) 01 = 5CK (DDR4-1866/2133/2400/2666) 10 = 6CK (DDR4-2933/3200) 11 = Reserved

Mode Register	Description
8:6	<b>Fine granularity refresh mode</b> 000 = Normal mode (fixed 1x) 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 110 = On-the-fly 1x/4x 111 = Reserved
5	<b>Temperature sensor status</b> 0 = Disabled 1 = Enabled
4	<b>Per-DRAM addressability</b> 0 = Normal operation (disabled) 1 = Enable
3	<b>Gear-down mode – Ratio of internal clock to external data rate</b> 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	<b>Multipurpose register (MPR) access</b> 0 = Normal operation 1 = Data flow from MPR
1:0	<b>MPR page select</b> 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

## Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MRn registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR.

Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

### ***WRITE Command Latency When CRC/DM is Enabled***

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled. This means at data rates less than or equal to 1600 MT/s then 4nCK is used, 5nCK or 6nCK are not allowed; at data rates greater than 1600 MT/s and less than or equal to 2666 MT/s then 5nCK is used, 4nCK or 6nCK are not allowed; and at data rates greater than 2666 MT/s and less than or equal to 3200 MT/s then 6nCK is used; 4nCK or 5nCK are not allowed.

### ***Fine Granularity Refresh Mode***

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

### ***Temperature Sensor Status***

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

### ***Per-DRAM Addressability***

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

### ***Gear-Down Mode***

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS\_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

## Mode Register 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**Note:** RAS\_n, CAS\_n, and WE\_n must be LOW during MODE REGISTER SET (MRS) command.

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> 000 = MR0 001 = MR1 010 = MR2 011 = MR3 <b>100 = MR4</b> 101 = MR5 110 = MR6 111 = DNU
17	<b>N/A on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
13	<b>Hard Post Package Repair (hPPR mode)</b> 0 = Disabled 1 = Enabled
12	<b>WRITE preamble setting</b> 0 = 1 <sup>t</sup> CK toggle <sup>1</sup> 1 = 2 <sup>t</sup> CK toggle
11	<b>READ preamble setting</b> 0 = 1 <sup>t</sup> CK toggle <sup>1</sup> 1 = 2 <sup>t</sup> CK toggle (When operating in 2 <sup>t</sup> CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable <sup>t</sup> CK range.)
10	<b>READ preamble training</b> 0 = Disabled 1 = Enabled

Mode Register	Description
9	<b>Self refresh abort mode</b> 0 = Disabled 1 = Enabled
8:6	<b>CMD (CAL) address latency</b> 000 = 0 clocks (disabled) 001 = 3 clocks <sup>1</sup> 010 = 4 clocks 011 = 5 clocks <sup>1</sup> 100 = 6 clocks 101 = 8 clocks 110 = Reserved 111 = Reserved
5	<b>soft Post Package Repair (sPPR mode)</b> 0 = Disabled 1 = Enabled
4	<b>Internal V<sub>REF</sub> monitor</b> 0 = Disabled 1 = Enabled
3	<b>Temperature controlled refresh mode</b> 0 = Disabled 1 = Enabled
2	<b>Temperature controlled refresh range</b> 0 = Normal temperature mode 1 = Extended temperature mode
1	<b>Maximum power savings mode</b> 0 = Normal operation 1 = Enabled
0	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved

**Note:** Not allowed when 1/4 rate gear-down mode is enabled.

### ***Hard Post Package Repair Mode***

The hard post package repair (hPPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether hPPR mode is available (A7 = 1) or not available (A7 = 0). hPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is irrevocable so great care should be exercised when using.

### ***Soft Post Package Repair Mode***

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be

repaired. The repair process is revocable by either doing a reset or power-down or by rewriting a new address in the same bank.

### ***WRITE Preamble***

Programmable WRITE preamble,  $t_{WPRE}$ , can be set to 1tCK or 2tCK via the MR4 register. The 1tCK setting is similar to DDR3. However, when operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

### ***READ Preamble***

Programmable READ preamble  $t_{RPRE}$  can be set to 1tCK or 2tCK via the MR4 register. Both the 1tCK and 2tCK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

### ***READ Preamble Training***

Programmable READ preamble training can be set to 1tCK or 2tCK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

### ***Command Address Latency***

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles ( $t_{CAL}$ ) between a CS<sub>n</sub> registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of  $\lceil t_{CK}(ns)/t_{CAL}(ns) \rceil$ .

### ***Internal VREF Monitor***

The device generates its own internal VREFDQ. This mode may be enabled during VREFDQ training, and when enabled, VREF,time-short and VREF,time-long need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

### ***Maximum Power Savings Mode***

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET<sub>n</sub> signal LOW).

### Mode Register 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**Note:** RAS\_n, CAS\_n, and WE\_n must be LOW during MODE REGISTER SET command.

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 <b>101 = MR5</b> 110 = MR6 111 = DNU
17	<b>N/A on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
13	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
12	<b>Data bus inversion (DBI) – READ DBI enable</b> 0 = Disabled 1 = Enabled
11	<b>Data bus inversion (DBI) – WRITE DBI enable</b> 0 = Disabled 1 = Enabled
10	<b>Data mask (DM)</b> 0 = Disabled 1 = Enabled

Mode Register	Description
9	<b>CA parity persistent error mode</b> 0 = Disabled 1 = Enabled
8:6	<b>Parked ODT value (<math>R_{TT(\text{Park})}</math>)</b> 000 = $R_{TT(\text{Park})}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
5	<b>ODT input buffer for power-down</b> 0 = Buffer enabled 1 = Buffer disabled
4	<b>CA parity error status</b> 0 = Clear 1 = Error
3	<b>CRC error status</b> 0 = Clear 1 = Error
2:0	<b>CA parity latency mode</b> 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400/2666) <sup>1</sup> 011 = 6 clocks (DDR4-2933/3200) 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

**Note:** Not allowed when 1/4 rate gear-down mode is enabled

### **Data Bus Inversion**

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12. DBI is not allowed during MPR READ operations.

### ***Data Mask***

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

### ***CA Parity Persistent Error Mode***

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

### ***ODT Input Buffer for Power-Down***

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide RTT(NOM) termination. However, the device may provide RTT(Park) termination depending on the MR settings. This is primarily for additional power savings.

### ***CA Parity Error Status***

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

### ***CRC Error Status***

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

### ***CA Parity Latency Mode***

CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT<sub>n</sub>, RAS<sub>n</sub>/A16, CAS<sub>n</sub>/A15, WE<sub>n</sub>/A14, and the address bus including bank address and bank group bits. The

control signals CKE, ODT, and CS<sub>n</sub> are not included in the parity calculation.

### Mode Register 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Address bus	BG1	BG0	BA1	BA0	A17	RAS <sub>n</sub>	CAS <sub>n</sub>	WE <sub>n</sub>	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**Note:** RAS<sub>n</sub>, CAS<sub>n</sub>, and WE<sub>n</sub> must be LOW during MODE REGISTER SET command.

Mode Register	Description
21	<b>RFU</b> 0 = Must be programmed to 0 1 = Reserved
20:18	<b>MR select</b> 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 <b>110 = MR6</b> 111 = DNU
17	<b>NA on 4Gb and 8Gb, RFU</b> 0 = Must be programmed to 0 1 = Reserved
12:10	<b><sup>t</sup>CCD_L</b> 000 = 4 clocks ( $\leq 1333$ Mb/s) 001 = 5 clocks ( $> 1333$ Mb/s and $\leq 1866$ Mb/s) 010 = 6 clocks ( $> 1866$ Mb/s and $\leq 2400$ Mb/s) 011 = 7 clocks ( $> 2400$ Mb/s and $\leq 2666$ Mb/s) 100 = 8 clocks ( $> 2666$ Mb/s and $\leq 3200$ Mb/s) 101 = Reserved 110 = Reserved 111 = Reserved
13, 9, 8	<b>DQ RX EQ</b> Default = 000; Must be programmed to 000 unless otherwise stated 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
7	<b>V<sub>REF</sub> Calibration Enable</b> 0 = Disable 1 = Enable
6	<b>V<sub>REF</sub> Calibration Range</b> 0 = Range 1 1 = Range 2
5:0	<b>V<sub>REF</sub> Calibration Value</b> See the V <sub>REFDQ</sub> Range and Levels table in the V <sub>REFDQ</sub> Calibration section

### ***tCCD\_L Programming***

The device controller must program the correct tCCD\_L value. tCCD\_L will be programmed according to the value defined per operating frequency in the AC parameter table. Although JEDEC specifies the larger of 5nCK or Xns, Micron's DRAM supports the larger of 4nCK or Xns.

### ***VREFDQ Calibration Enable***

VREFDQ calibration is where the device internally generates its own VREFDQ to be used by the DQ input receivers. The VREFDQ value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal VREFDQ level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ calibration must be used whenever values are being written to the MR6[6:0] register.

### ***VREFDQ Calibration Range***

The device defines two VREFDQ calibration ranges: Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDDQ while Range 2 supports VREFDQ between 45% and 77% of VDDQ, as seen in VREFDQ Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

### ***VREFDQ Calibration Value***

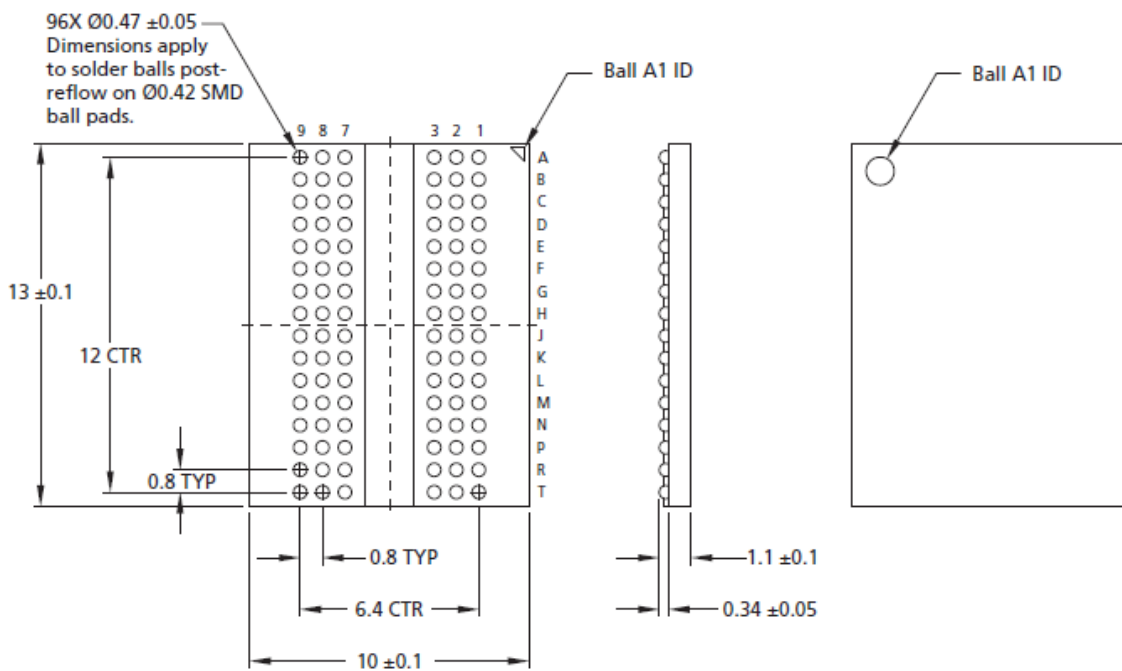
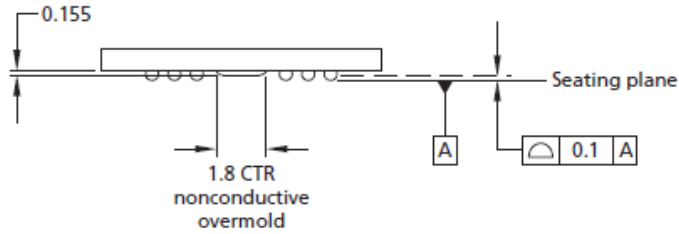
Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ, as seen in VREFDQ Range and Levels table in the VREFDQ Calibration section.

### ***DQ RX EQ***

These settings are reserved for DQ Equalization functionality.

**Package Description: 96Ball-FBGA**

**Solder ball: Lead free (Sn-Ag-Cu)**



- Notes: 1. All dimensions are in millimeters.  
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

**Revision History**

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Feb. 2019	Rico Yang	N/A
1.0	First SPEC. release.	Feb. 2019	Rico Yang	N/A