

8Gb (64Mx8Banksx16) DDR4 SDRAM

Descriptions

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR4 SDRAM uses an 8n-prefetch architecture to achieve high-speed operation. The 8n-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8n-bit wide, four-clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Features

- VDD = VDDQ = 1.2V \pm 60mV
- VPP = 2.5V, -125mV, +250mV
- On-die, internal, adjustable VREFDQ generation
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability

Ordering Information

Part No	Organization	Max. Data Rate	Package	Grade
H2A908G16A6JIWC	512M X 16	DDR4-2400Mbps 17-17-17	96Ball BGA, 7.5x13 mm	Commercial
H2A908G16A6JJWC	512M X 16	DDR4-2666Mbps 19-19-19	96Ball BGA, 7.5x13 mm	Commercial
H2A908G16A6JKWC	512M X 16	DDR4-3200Mbps 22-22-22	96Ball BGA, 7.5x13 mm	Commercial
H2A908G16A6JIWI	512M X 16	DDR4-2400Mbps 17-17-17	96Ball BGA, 7.5x13 mm	Industrial
H2A908G16A6JJWI	512M X 16	DDR4-2666Mbps 19-19-19	96Ball BGA, 7.5x13 mm	Industrial
H2A908G16A6JKWI	512M X 16	DDR4-3200Mbps 22-22-22	96Ball BGA, 7.5x13 mm	Industrial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDDQ	VSSQ	DQU0	A	UDQS_c	VSSQ	VDDQ
VPP	VSS	VDD	B	UDQS_t	DQU1	VDD
VDDQ	DQU4	DQU2	C	DQU3	DQU5	VSSQ
VDD	VSSQ	DQU6	D	DQU7	VSSQ	VDDQ
VSS	UDM_n /UDBI_n	VSSQ	E	LDM_n /LDBI_n	VSSQ	VSS
VSSQ	VDDQ	LDQS_c	F	DQL1	VDDQ	ZQ
VDDQ	DQL0	LDQS_t	G	VDD	VSS	VDDQ
VSSQ	DQL4	DQL2	H	DQL3	DQL5	VSSQ
VDD	VDDQ	DQL6	J	DQL7	VDDQ	VDD
VSS	CKE	ODT	K	CK_t	CK_c	VSS
VDD	WE_n/A14	ACT_n	L	CS_n	RAS_n/A16	VDD
VREFCA	BG0	A10/AP	M	A12/BC_n	CAS_n/A15	VSS
VSS	BA0	A4	N	A3	BA1	TEN
RESET_n	A6	A0	P	A1	A5	ALERT_n
VDD	A8	A2	R	A9	A7	VPP
VSS	A11	PAR	T	NC	A13	VDD

96-Ball FBGA – x16 Ball Descriptions

Pin	Symbol	Description
Input	A[17:0]	(Address inputs) Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts.
Input	A10/AP	(Auto precharge) A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
Input	A12/BC_n	(Burst chop) A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
Input	ACT_n	(Command input) ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
Input	BA[1:0]	(Bank address inputs) Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
Input	BG[1:0]	(Bank group address inputs) Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration

96-Ball FBGA – x16 Ball Descriptions (Continued)

Pin	Symbol	Description
Input	C0/CKE1, C1/CS1_n, C2/ODT1	(Stack address inputs) These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
Input	CK_t, CK_c	(Clock) Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
Input	CKE	(Clock enable) CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
Input	CS_n	(Chip select) All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
Input	DM_n, UDM_n LDM_n	(Input data mask) DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section.
Input	ODT	(On-die termination) ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, UDQS_t, UDQS_c, LDQS_t, LDQS_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable RTT.

96-Ball FBGA – x16 Ball Descriptions (Continued)

Pin	Symbol	Description
Input	PAR	(Parity for command and address) This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
Input	RAS_n/A16, CAS_n/A15, WE_n/A14	(Command inputs) RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
Input	RESET_n	(Active LOW asynchronous reset) Reset is active when RESET_n is LOW, and inactive when RESET_n HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD (960 mV for DC HIGH and 240 mV for DC LOW).
Input	TEN	(Connectivity test mode) TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW).
I/O	DQ	(Data input/output) Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] the x4, x8, and x16 configurations, respectively. If write CRC is Enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal VREF level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the RTT value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin
I/O	DBI_n, UDBI_n, LDBI_n	(DBI input/output) Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.

96-Ball FBGA – x16 Ball Descriptions (Continued)

Type	Symbol	Description
I/O	DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	(Data strobe) Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
Output	ALERT_n	(Alert output) This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/ address parity error and the CRC data error when either of these functions is enabled in the mode register.
Output	TDQS_t, TDQS_c	(Termination data strobe) TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
Supply	VDD	Power supply: 1.2V ±0.060V.
Supply	VDDQ	DQ power supply: 1.2V ±0.060V.
Supply	VPP	DRAM activating power supply: 2.5V –0.125V/+0.250V.
Supply	VREFCA	Reference voltage for control, command, and address pins.
Supply	VSS	Ground.
Supply	VSSQ	DQ ground.
Reference	ZQ	Reference ball for ZQ calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
-	RFU	Reserved for future use.
-	NC	No connect: No internal electrical connection is present.
-	NF	No function: May have internal connection present but has no function.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.3 ~ +1.5		V
VDD	Power Supply Voltage	-0.3 ~ +1.5		V
VDDQ	Power Supply Voltage	-0.3 ~ +1.5		V
VPP	Power Supply Voltage	-0.3 ~ +3.0		V
TOP	Operating Temperature Range	Commercial	0 ~ +85	°C
		Industrial	-40~95	°C
TSTG	Storage Temperature Range	-55 ~ +100		°C

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	Supply voltage	1.14	1.2	1.26	V
VDDQ	Supply voltage for output	1.14	1.2	1.26	V
VPP	Wordline supply voltage	2.375	2.5	2.750	V

Input/ Output Capacitance

Symbol	Parameters	Min.	Max.	Unit	Notes
CCK	Input capacitance	0.2	0.8	pF	2,3
CDCK	Input capacitance delta	0	0.05	pF	2,3,6
CDI_CTRL	Input capacitance delta	-0.1	0.1	pF	2,3,8,9
CDI_ADD_CMD	Input capacitance delta	-0.1	0.1	pF	1,2,10,11
CIO	Input/output capacitance	0.55	1.4	pF	1,2,3
CI	Input capacitance	0.2	0.8	pF	2,3,4
CDIO	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,4
CDDQS	Input/output capacitance delta	0	0.05	pF	2,3,5
CALERT	Input/output capacitance	0.5	1.5	pF	2,3
CZQ	Input/output pin capacitance, ZQ	-	2.3	pF	2,3,12
CTEN	Input/output capacitance	0.2	2.3	pF	2,3,13

Notes1: Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.

Notes2: This parameter is not subject to a production test; it is verified by design and characterization.

The capacitance is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with VDD, VDDQ, VSS, and VSSQ applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). VDD = VDDQ = 1.5V, VBIAS = VDD/2 and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.

Notes3: This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.

Notes4: $CDIO = CIO(DQ, DM) - 0.5 \times (CIO(DQS_t) + CIO(DQS_c))$.

Notes5: Absolute value of CIO (DQS_t), CIO (DQS_c)

Notes6: Absolute value of CCK_t, CCK_c

Notes7: CI applies to ODT, CS_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.

Notes8: CDI_CTRL applies to ODT, CS_n, and CKE.

Notes9: $CDI_CTRL = CI(CTRL) - 0.5 \times (CI(CLK_t) + CI(CLK_c))$.

Notes10: CDI_ADD_CMD applies to A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.

Notes11: $CDI_ADD_CMD = CI(ADD_CMD) - 0.5 \times (CI(CLK_t) + CI(CLK_c))$.

Notes12: Maximum external load capacitance on ZQ pin: 5pF.

Notes13: Only applicable if TEN pin does not have an internal pull-up.

DRAM Package Electrical Specifications

Parameters		Symbol	Min.	Max.	Unit	Notes
Input/ output	Zpkg	ZIO	45	85	ohm	1,2,4
	Package delay	TDIO	14	45	ps	1,3,4
	Lpkg	LIO	-	3.4	nH	11
	Cpkg	CIO	-	0.82	pF	11
LDQS_t/ LDQS_c/ UDQS_t/ UDQS_c	Zpkg	ZIO DQS	45	85	ohm	1,2
	Package delay	TDIO DQS	14	45	ps	1,3
	Lpkg	LIO DQS	-	3.4	nH	11
	Cpkg	CIO DQS	-	0.82	pF	11
LDQS_t/ LDQS_c, UDQS_t/ UDQS_c,	Delta Zpkg	DZDIO DQS	-	10	ohm	1,2,6
	Delta delay	DTdDIO DQS	-	5	ps	1,3,6
Input CTRL pins	Zpkg	ZI CTRL	50	90	ohm	1,2,8
	Package delay	TdI CTRL	14	42	ps	1,3,8
	Lpkg	LI CTRL	-	3.4	nH	11
	Cpkg	CI CTRL	-	0.7	pF	11
Input CMD ADD pins	Zpkg	ZI ADD CMD	50	90	ohm	1,2,7
	Package delay	TdI ADD CMD	14	52	ps	1,3,7
	Lpkg	LI ADD CMD	-	3.9	nH	11
	Cpkg	CI ADD CMD	-	0.86	pF	11

DRAM Package Electrical Specifications(Continued)

Parameters		Symbol	Min.	Max.	Unit	Notes
CK_t, CK_c	Zpkg	ZCK	50	90	ohm	1,2
	Package delay	TdCK	14	42	ps	1,3
	Package delay	DZDCK	-	10	ohm	1,2,5
	Delta delay	DTdDCK	-	5	ps	1,3,5
Input CLK	Lpkg	LI CLK	-	3.4	nH	11
	Cpkg	CI CLK	-	0.7	pF	11
ZQ Zpkg		ZO ZQ	-	100	ohm	1,2
ZQ delay		TdO ZQ	20	90	ps	1,3
ALERT Zpkg		ZO ALERT	40	100	ohm	1,2
ALERT delay		TdO ALERT	20	55	ps	1,3

Notes1: The package parasitic (L and C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, and VSSQ shorted with all other signal pins floating.

The inductance is measured with VDD, VDDQ, VSS, and VSSQ shorted and all other signal pins shorted at the die, not pin, side.

Notes2: Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).

Notes3: Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Td/pkg (total per pin) = SQRT (Lpkg × Cpkg).

Notes4: ZIO and TdIO apply to DQ, DM, TDQS_t and TDQS_c.

Notes5: Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).

Notes6: Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).

Notes7: ZI ADD CMD and TdI ADD CMD apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, and WE_n.

Notes8: ZI CTRL and TdI CTRL apply to ODT, CS_n, and CKE.

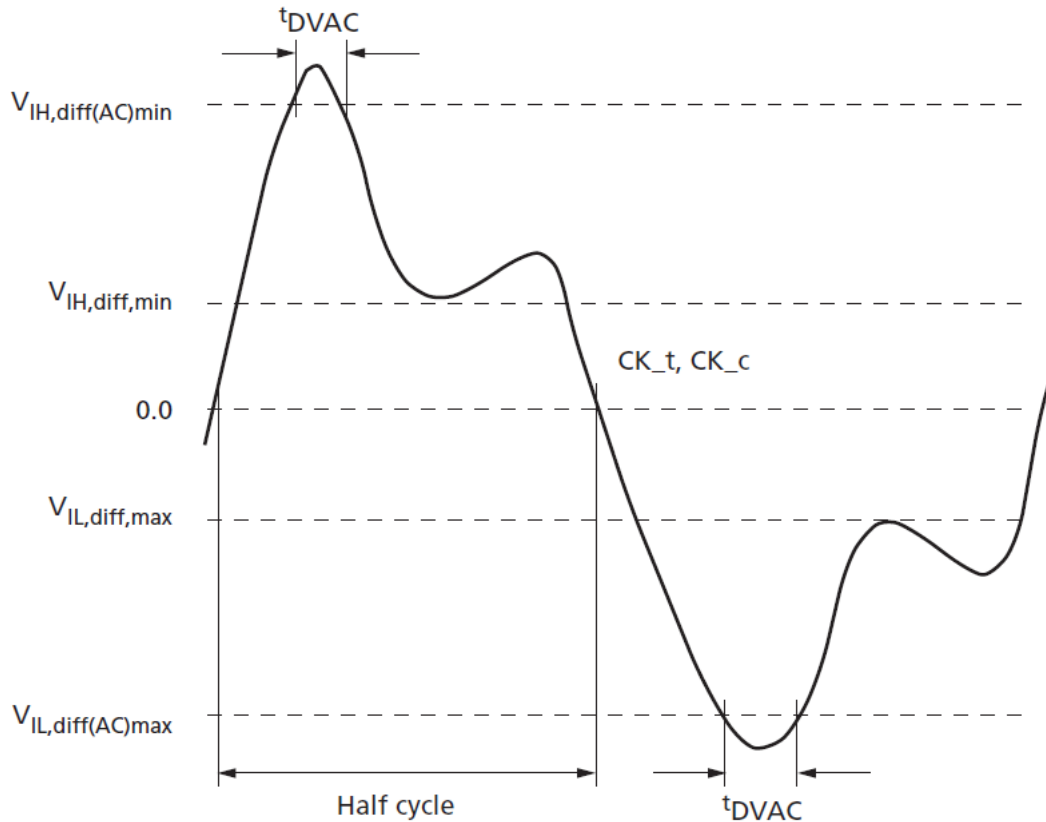
Notes9: Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.

Notes10: It is assumed that Lpkg can be approximated as $Lpkg = ZO \times Td$.

Notes11: It is assumed that Cpkg can be approximated as $Cpkg = Td/ZO$.

AC and DC Differential Input Measurement Levels

Differential Inputs



Differential Input Swing Requirements for CK_t, CK_c

Symbol	Parameter	Min.	Max.	Units	Note
V _{IHdiff}	Differential input high	+0.15	See Note3	V	1
V _{ILdiff}	Differential input low	See Note3	-0.15	V	1
V _{IHdiff (AC)}	AC Differential input high	2x(V _{IH(AC)} -V _{REF})	See Note3	V	2
V _{ILdiff (AC)}	AC Differential input low	See Note3	2x(V _{REF} -V _{IL(AC)})	V	2

Note1: Used to define a differential signal slew-rate.

Note2: For CK_t, CK_c use V_{IH(AC)} and V_{IL(AC)} of ADD/CMD and V_{REFCA}.

Note3: These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (V_{IH.CA(DC)} max, V_{IL.CA(DC)}min) for single-ended signals as well as the limitations for overshoot and undershoot.

Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

Minimum Time AC Time tDVAC for CK

Slew Rate [V/ns]	tDVAC (ps) at [VIH,diff(AC) to VIL,diff(AC)]	
	200mV	TBDmV
>4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
<1.0	80	-

Note: Below VIL(AC).

Single-Ended Requirements for CK Differential Signals

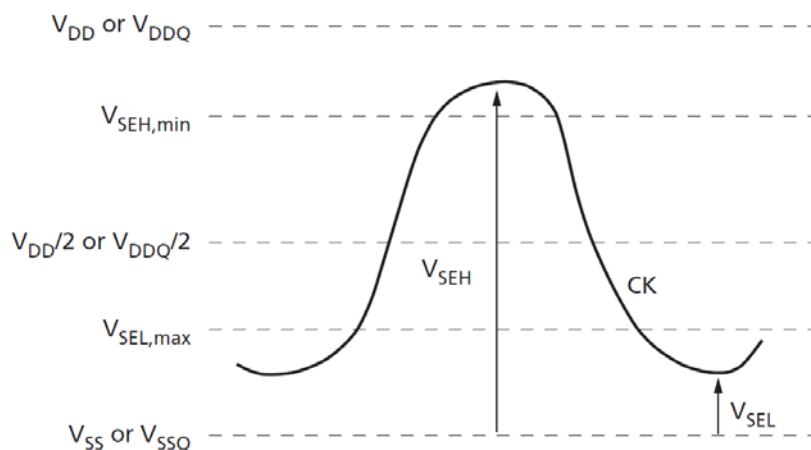
Each individual component of a differential signal (CK, DQS, /CK, /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(AC) / VIL(AC)) for Address/Command signals) in every half-cycle.

DQS, /DQS have to reach VSEHmin / VSELmax [approximately the ac-levels (VIH(AC) / VIL(AC)) for DQ signals] in every half-cycle preceding and following a valid transition.

Note that the applicable AC-levels for Address/Command and DQ's might be different per speed-bin etc. E.g., if VIHCA(AC150)/VILCA(AC150) is used for Address/Command signals, then these AC-levels apply also for the single-ended components of differential CK and /CK.

Single-Ended Requirements for CK



Single-Ended Requirements for CK

Symbol	Parameter	Min.	Max.	Units	Note
VSEH	Single-ended high-level for CK, /CK	$(VDD/2)+0.1$	See Note3	V	1,2
VSEL	Single-ended low-level for CK, /CK	See Note3	$(VDD/2)-0.095$	V	1,2

Note1: For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

Note2: ADDR/CMD VIH(AC) and VIL(AC) based on VREFCA.

Note3: These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

AC and DC Output Measurement Levels

Symbol	Parameter	Specification	Units	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	$1.1 \times VDDQ$	V	1
VOM(DC)	DC output middle measurement level (for IV curve linearity)	$0.8 \times VDDQ$	V	1
VOL(DC)	DC output low measurement level (for IV curve linearity)	$0.5 \times VDDQ$	V	1
VOH(AC)	AC output high measurement level (for output slew rate)	$(0.7+0.15) \times VDDQ$	V	1
VOL(AC)	AC output low measurement level (for output slew rate)	$(0.7-0.5) \times VDDQ$	V	1
VOHdiff(AC)	AC differential output high measurement level (for output slew rate)	$0.3 \times VDDQ$	V	2
VOLdiff(AC)	AC differential output low measurement level (for output slew rate)	$-0.3 \times VDDQ$	V	2

Notes1: The swing of $\pm 0.15 \times VDDQ$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7$ and an effective test load of 50Ω to $VTT = VDDQ$.

Notes2: The swing of $\pm 0.3 \times VDDQ$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7$ and an effective test load of 50Ω to $VTT = VDDQ$ at each differential output.

Recommended DC Operating Conditions

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	3200	2666	2400	Units
		Max			
I _{DD0}	Operating One Bank Active-Precharge Current (AL = 0) CKE: HIGH; External clock: On; tCK, nRC, nRAS, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: VDDQ; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the IDD0 Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	47	45	44	mA
I _{PP0}	Operating One Bank Active-Precharge IPP Current (AL = 0) Same conditions as IDD0 above	9.5	9.5	9.5	mA
I _{DD1}	Operating One Bank Active-Read-Precharge Current (AL = 0) CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, CL: see the previous table; BL: 8;1, 5 AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the IDD1 Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the following table); Output buffer and RTT: enabled in mode registers;2 ODT Signal stable at 0	63	61	60	mA
I _{DD2P}	Precharge Power-Down Current CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	22	20	18	mA
I _{DD2N}	Precharge Standby Current (AL = 0) CKE: HIGH; External clock: On; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0; Pattern details: see the IDD2N and IDD3N Measurement-Loop Pattern table	30	28	27	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	3200	2666	2400	Units
		Max			
I _{DD3P}	Active Power-Down Current (AL = 0) CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	33	31	29	mA
I _{DD3N}	Active Standby Current (AL = 0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: all banks open; Output buffer and	41	38	37	mA
I _{DD4R}	Operating Burst Read Current (AL = 0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS_n: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4R Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the IDD4R Measurement-Loop Pattern table; DM_n stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the IDD4R Measurement-Loop pattern table);Output buffer and RTT: Enabled in mode registers;2 ODT signal: stable at 0	235	200	195	mA
I _{DD4W}	Operating Burst Write Current (AL = 0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4W Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the IDD4W Measurement-Loop Pattern table; DM: stable at 0; Bank activity: all banks open, WR commands cycling throu banks: 0, 0, 1, 1, 2, 2, ... (see IDD4W Measurement-Loop Pattern table);Output buffer and RTT: enabled in mode registers (see note2); ODT signal: stable at HIGH	179	160	150	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	3200	2666	2400	Units
		Max			
I _{DD5R}	Burst Refresh Current (1X REF) CKE: HIGH; External clock: on; tCK, CL, nREFI: see the previous table; BL: 8;1 AL: 0; CS_n: HIGH between REF;Command, address, bank group address, bank address inputs: partially toggling according to the IDD5R Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: REF command every nREFI (see the IDD5R Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers2; ODT signal:stable at 0	199	197	196	mA
I _{PP5R}	Burst Refresh Current (1X REF) Same conditions as IDD5R above	63	63	63	mA
I _{DD6N}	Self Refresh Current: Normal Temperature Range TC: 0–85°C; Auto self refresh (ASR): disabled;3 Self refresh temperature range (SRT): normal;4 CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8;1 AL: 0; CS_n, command, address, bank group address, bank address, data I/O: VDDQ; DM_n: stable at 1; Bank activity: SELF REFRESH operation ;Output buffer and RTT: enabled in mode registers;2 ODT signal: midlevel	21	21	21	mA
I _{PP6N}	Self Refresh IPP Current: Normal Temperature Range Same conditions as IDD6N above	5	5	5	mA
I _{DD7}	Operating Bank Interleave Read Current CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8;15 AL: CL -1; CS_n: HIGH between ACT and RDA; Command, address, group bank address, bank address inputs: partially toggling according to the IDD7 Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the IDD7 Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the IDD7 Measurement-Loop Pattern table; Output buffer and RTT: enabled in mode registers;2 ODT signal: stable at 0	197	189	175	mA

Recommended DC Operating Conditions(Continued)

VDD = VDDQ = 1.2V ±60mV

Symbol	Parameter & Test Conditions	3200	2666	2400	Units
		Max			
I _{PP7}	Operating Bank Interleave Read IPP Current Same conditions as IDD7 above	24	24	24	mA
I _{DD8}	Maximum Power Down Current Place DRAM in MPSM then CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8;1 AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM_n:stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; 2 ODT signal: stable at 0	12	12	12	mA

Note 1: Burst length: BL8 fixed by MRS: set MR0[1:0] 00.

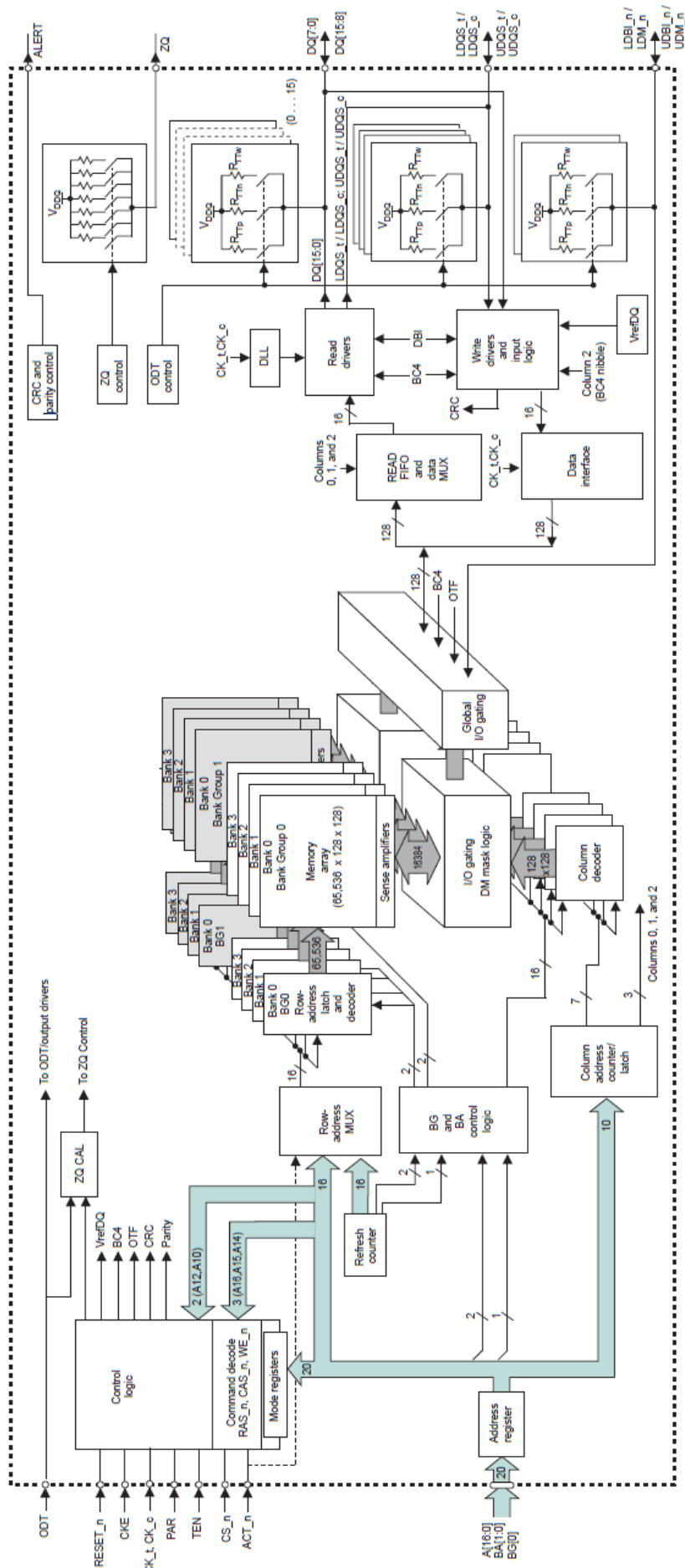
Note 2: Output buffer enable: set MR1[12] 0 (output buffer enabled); set MR1[2:1] 00 (RON = RZQ/7); RTT(NOM) enable: set MR1[10:8] 011 (RZQ/6); RTT(WR) enable: set MR2[11:9] 001(RZQ/2), and RTT(Park) enable: set MR5[8:6] 000 (disabled).

Note 3: Auto self refresh (ASR): set MR2[6] 0 to disable or MR2[6] 1 to enable feature.

Note 4: Self refresh temperature range (SRT): set MR2[7] 0 for normal or MR2[7] 1 for extended temperature range.

Note 5: READ burst type: Nibble sequential, set MR0[3] 0.

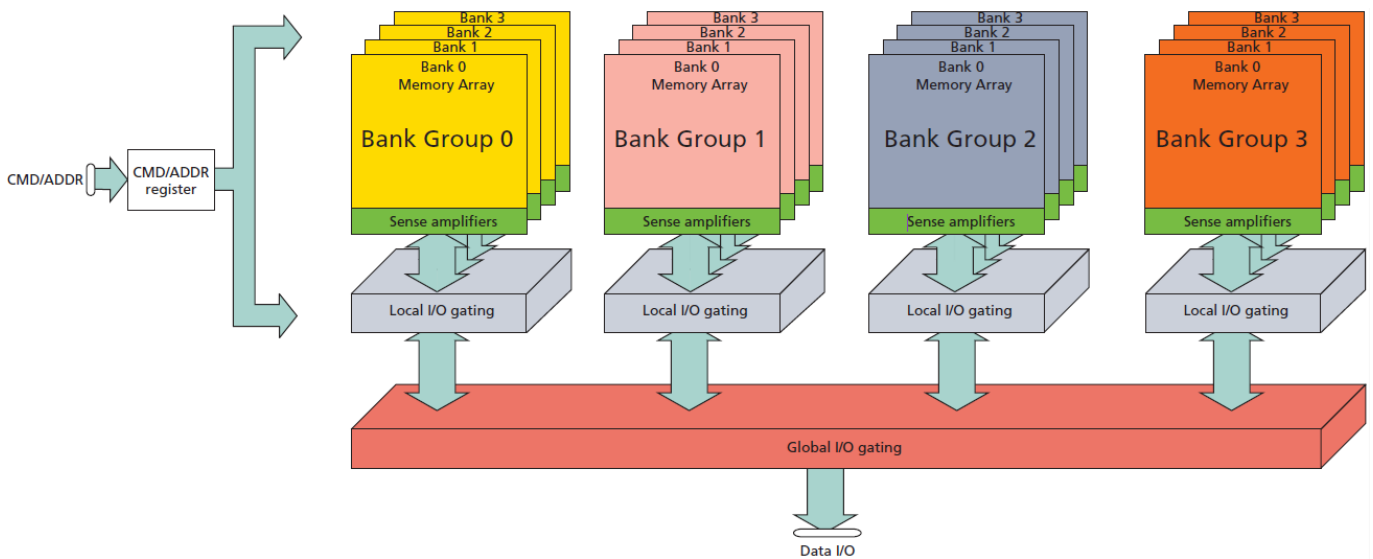
Functional Block Diagram



Bank Access Operation

DDR4 supports bank grouping: x4/x8 DRAMs have four bank groups (BG[1:0]), and each bank group is comprised of four subbanks (BA[1:0]); x16 DRAMs have two bank groups (BG[0]), and each bank group is comprised of four subbanks. Bank accesses to different banks' groups require less time delay between accesses than bank accesses to within the same bank's group. Bank accesses to different bank groups require tCCD_S (or short) delay between commands while bank accesses within the same bank group require tCCD_L (or long) delay between commands.

Bank Group x4/x8 Block Diagram



Note 1: Bank accesses to different bank groups require tCCD_S.

Note 2: Bank accesses within the same bank group require tCCD_L.

Refresh Parameters

Parameter	Symbol	8G	Unit	Notes	
REF command to ACT or REF command time	tRFC (All bank groups)	350	ns	-	
Average periodic refresh interval	tREFI	0°C ≤ TC ≤ 85°C	7.8	μs	-
		85°C < TC ≤ 95°C	3.9	μs	*

Note: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

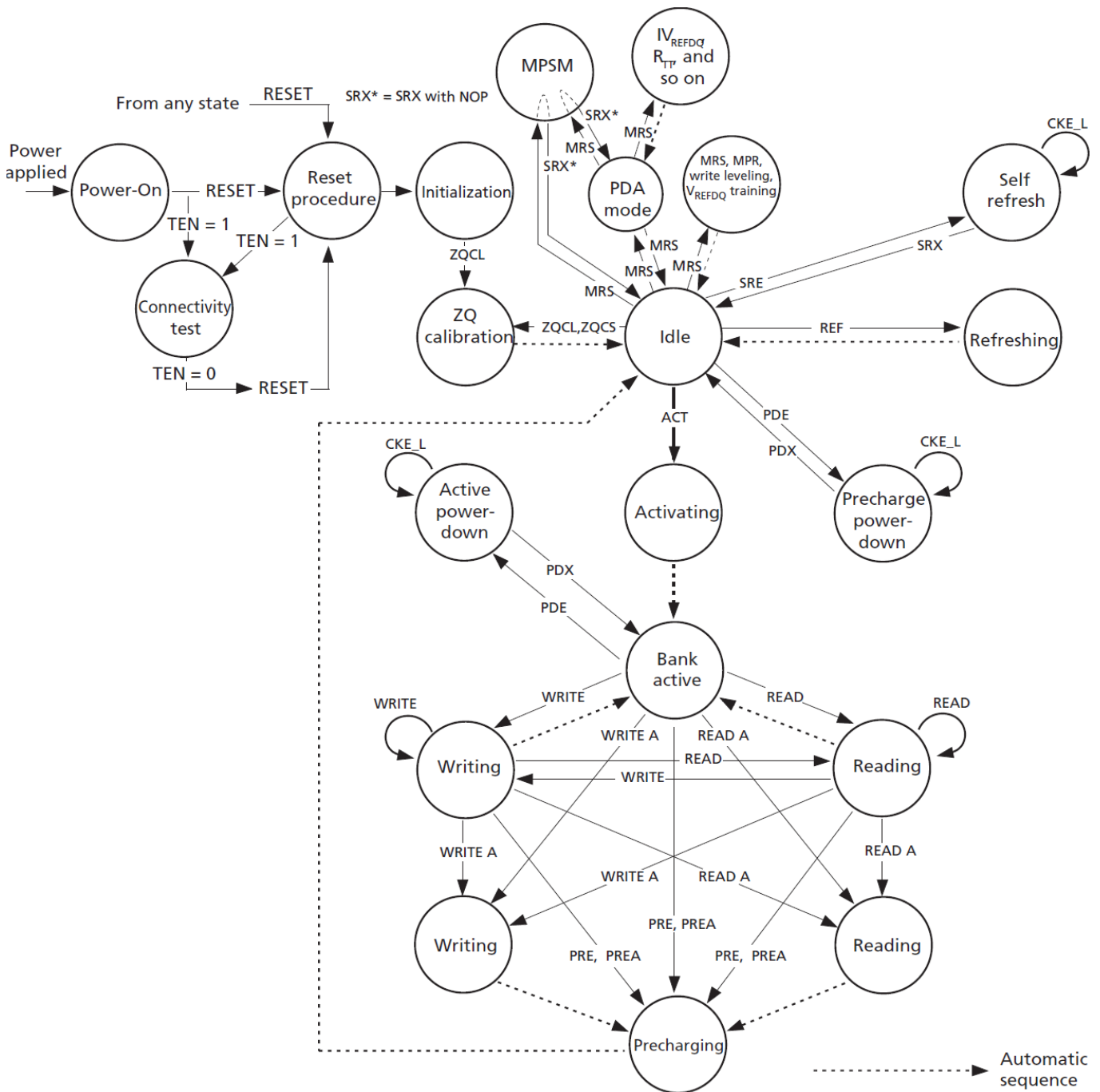
AC Operating Test Characteristics

DDR4-2400 & 2666 & 3200 Speed Bins

VDD = VDDQ = 1.2V \pm 60mV

Symbol	Speed Bin		(DDR4-3200)		(DDR4-2666)		(DDR4-2400)		Units
	CL-nRCD-nRP		22-22-22		19-19-19		17-17-17		
	Parameter		Min.	Max.	Min.	Max.	Min.	Max.	
tAA	Internal read command to first data		13.75	18	14.25	18	14.16	18	ns
tRCD	Active to read or write delay		13.75	-	14.25	-	14.16	-	ns
tRP	Precharge command period		13.75	-	14.25	-	14.16	-	ns
tRC	Active to active/auto refresh command		45.75	-	46.25	-	46.16	-	ns
tRAS	Active to precharge command period		32	9xtREFI	32	9xtREFI	32	9xtREFI	ns
READ: nonDBI	READ: DBI	WRITE	Min.	Max.	Min.	Max.	Min.	Max.	Units
CL=9	CL=11	CWL=9	Reserved		Reserved		Reserved		Reserved
CL=10	CL=12	CWL=9	Reserved		1.5	1.6	1.5	1.6	ns
CL=11	CL=13	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=12	CL=14	CWL=9,11	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL=13	CL=15	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=14	CL=16	CWL=10,12	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL=15	CL=18	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=16	CL=19	CWL=11,14	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL=17	CL=20	CWL=12,16	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL=18	CL=21	CWL=12,16	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL=19	CL=22	CWL=14,18	0.750	<0.833	0.750	<0.833	-	-	ns
CL=20	CL=23	CWL=14,18	0.750	<0.833	0.750	<0.833	-	-	ns
CL=22	CL=26	CWL=16,20	0.625	<0.75	-	-	-	-	
CL=24	CL=28	CWL=16,20	0.625	<0.75	-	-	-	-	
Support CL Settings			10-22,24		10-20		10-18		
Support CL settings with read DBI			12-16, 18-26,28		12-16, 18-23		12-16,18-21		
Support CWL Settings			9-12,14,16,18,20		9-12, 14,16,18		9,10,11,12,14,16		

Simplified State Diagram



Command Truth Table

Function	Abbreviation	CKE		CS _n	ACT _n	RAS _n /A16	CAS _n /A15	WE _n A14	BG0- BG1	BA0- BA1	C2-C0	A12/ BC _n	A17, A13, A11	A10/ AP	A0-A9	NOTE	
		Previous Cycle	Current Cycle														
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12	
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V		
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V		7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V		
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V		
RFU	RFU	H	H	L	H	L	H	H	RFU								
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address (RA)					
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA		
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA		
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA		
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA		
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA		
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA		
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA		
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA		
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA		
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA		
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA		
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA		
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V		10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X		
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X		6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X		6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V		
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V		

- Note1:** All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When ACT_n = H; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n respectively. When ACT_n = L; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14 respectively
- Note2:** RESET_n is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Note3:** Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
- Note4:** "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
- Note5:** Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
- Note6:** The Power Down Mode does not perform any refresh operation.
- Note7:** The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- Note8:** Controller guarantees self refresh exit to be synchronous.
- Note9:** VPP and VREF(VrefCA) must be maintained during Self Refresh operation.
- Note10:** The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit
- Note11:** Refer to the CKE Truth Table for more detail with CKE transition.
- Note12:** During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18

Note1: CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

Note2: Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.

Note3: Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.

Note4: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note5: The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

Note6: During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

Note7: DESELECT and NOP are defined in the "Command Truth Table".

Note8: On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

Note9: Self-Refresh mode can only be entered from the All Banks Idle state.

Note10: Must be a legal command as defined in the "Command Truth Table".

Note11: Valid commands for power-down entry and exit are NOP and DESELECT only.

Note12: Valid commands for self-refresh exit are NOP and DESELECT only.

Note13: Self-Refresh can not be entered during Read or Write operations.

Note14: The Power-Down does not perform any refresh operations.

Note15: "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

Note16: VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh.operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note17: If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

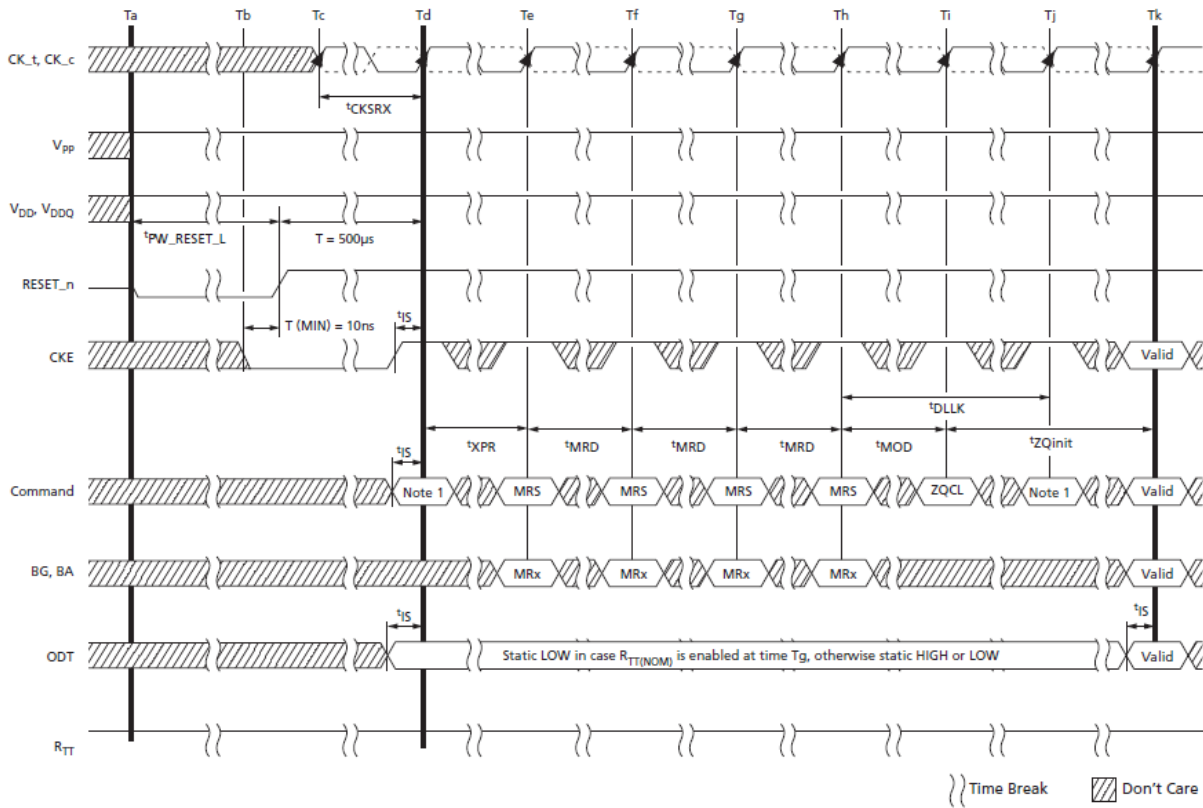
Note18: 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). /RESET needs to be maintained for minimum 700 us with stable power. CKE is pulled “Low” anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDD_{min} must be no greater than 200 ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ volts.
 - VDD and VDDQ are driven from a single power converter output, AND
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
 - Vref tracks $VDDQ/2$. OR
 - Apply VDD without any slope reversal before or at the same time as VDDQ.
 - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ($tXPR = \max(tXS ; 5 \times tCK)$)
6. Issue MRS command to load MR3 with all application settings, wait tMRD.
7. Issue MRS command to load MR6 with all application settings, wait tMRD.
8. Issue MRS command to load MR5 with all application settings, wait tMRD.
- 9 Issue MRS command to load MR4 with all application settings, wait tMRD.
10. Issue MRS command to load MR2 with all application settings, wait tMRD.
11. Issue MRS command to load MR1 with all application settings, wait tMRD.
12. Issue MRS command to load MR0 with all application settings, wait tMOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for tDLLK and tZQinit to complete.

Reset and Power up initialization sequence



Note 1: From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.

Note 2: MRS commands must be issued to all mode registers that have defined settings.

Note 3: In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).

Note 4: TEN is not shown; however, it is assumed to be held LOW.

Mode Register Definition

Mode Register MR0

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS	
A13 ⁵ , A11:A9	WR and RTP ^{2, 3}	Write Recovery and Read to Precharge for auto precharge(see Table 2)	
A8	DLL Reset	0 = NO	1 = Yes
A7	TM	0 = Normal	1 = Test
A12, A6:A4,A2	CAS Latency ⁴	(see Table 3)	
A3	Read Burst Type	0 = Sequential	1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) Abbreviated BL8MRS 01 = BC4 or 8 (on the fly) Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbreviated BC4MRS 11 = Reserved	

NOTE:

- Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
- WR (write recovery for autoprecharge)min in clock cycles is calculated following rounding algorithm defined in Section 11.5. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
- The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
- The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency. Cas Latency controlled by A12 is optional for 4Gb device.
- A13 for WR and RTP setting is optional for 4Gb.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Burst Type (A3)

Burst Length	R/W	A2	A1	A0	Sequential Addressing	Interleave Addressing
BC4	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
BL8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

Note1: 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.

Note2: When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for tWR and tWTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.

Note3: T = Output driver for data and strobes are in High-Z.

V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.

X = "Don't Care."

CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): $RL = AL + CL$.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7]= 1.

DLL Reset

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, tDLLK must be met before functions requiring the DLL can be used, such as READ commands or synchronous ODT operations, for example,).

Write Recovery

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine tDAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: $WR (MIN) \text{ cycles} = \text{roundup}(tWR[ns]/tCK[ns])$. The WR value must be programmed to be equal to or larger than tWR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; tWR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data. Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer: $RTP (MIN) \text{ cycles} = \text{roundup}(tRTP[ns]/tCK[ns])$. The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with tRP to determine the ACT timing to the same bank.

Mode Register MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ³
A17	RFU	0 = must be programmed to 0 during MRS
A13, A6, A5	Rx EQ Control ⁴⁾	(see Table 6)
A12	Qoff ¹	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 4)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A4, A3	Additive Latency	00 = 0(AL disabled) 10 = CL-2 01 = CL-1 11 = Reserved
A2, A1	Output Driver Impedance Control	(see Table 5)
A0	DLL Enable	0 = Disable ² 1 = Enable

Note:

1. Outputs disabled - DQs, DQS_ts, DQS_cs.
2. States reversed to "0 as Disable" with respect to DDR4.
3. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
4. Rx EQ Control is an optional feature and SK hynix supports CTLE for it. It is designed for 2933Mbps and 3200Mbps. please contact SK hynix if you need more information

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Note: AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Termination Data Strobe

Termination data strobe (TDQS) is a feature of the x8 device and provides additional termination resistance outputs that may be useful in some system configurations. Because this function is available only in a x8 configuration, it must be disabled for x4 and x16 configurations.

While TDQS is not supported in x4 or x16 configurations, the same termination resistance function that is applied to the TDQS pins is applied to the DQS pins when enabled via the mode register.

The TDQS, DBI, and DATA MASK (DM) functions share the same pin. When the TDQS function is enabled via the mode register, the DM and DBI functions are not supported. When the TDQS function is disabled, the DM and DBI functions can be enabled separately.

TDQS Function Matrix

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	Enabled or disabled
	Disabled	Enabled	Enabled or disabled
	Disabled	Disabled	Enabled or disabled
Enabled	Disabled	Disabled	Disabled

Mode Register MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11, A10:A9	RTT_WR	(see Table 7)
A8, A2	RFU	0 = must be programmed to 0 during MRS
A7:A6	Low Power Auto Self Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	(see Table 8)
A1:A0	RFU	0 = must be programmed to 0 during MRS

Note:

- Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR:

Note: Not allowed when 1/4 rate gear-down mode is enabled.

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CAS Write Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): $WL = AL + PL + CWL$.

Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT (RTT(WR)) settings in MR2[11:9]. In write leveling mode, only RTT(NOM) is available.

Mode Register MR3

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12:A11	MPR Read Format	00 = Serial 01 = Parallel	10 = Staggered 11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 10)	
A8:A6	Fine Granularity Refresh Mode	(see Table 9)	
A5	Temperature sensor readout	0 : disabled	1: enabled
A4	Per DRAM Addressability	0 = Disable	1 = Enable
A3	Geardown Mode	0 = 1/2 Rate	1 = 1/4 Rate
A2	MPR Operation	0 = Normal	1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 01 = Page1 (see Table 11)	10 = Page2 11 = Page3

Note: 1. Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MRn registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled. This means at data rates less than or equal to 1600 MT/s then 4nCK is used, 5nCK or 6nCK are not allowed; at data rates greater than 1600 MT/s and less than or equal to 2666 MT/s then 5nCK is used, 4nCK or 6nCK are not allowed; and at data rates greater than 2666 MT/s and less than or equal to 3200 MT/s then 6nCK is used; 4nCK or 5nCK are not allowed.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

Mode Register 4

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS	
A13	hPPR	0 = Disable	1 = Enable
A12	Write Preamble	0 = 1 nCK	1 = 2 nCK
A11	Read Preamble	0 = 1 nCK	1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable	1 = Enable
A9	Self Refresh Abort	0 = Disable	1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 (See Table 12)	100 = 6 101 = 8 110 = Reserved 111 = Reserved
A5	sPPR	0 = Disable	1 = Enable
A4	Internal Vref Monitor	0 = Disable	1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable	1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal	1 = Extended
A1	Maximum Power Down Mode	0 = Disable	1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS	

Note:

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Hard Post Package Repair Mode

The hard post package repair (hPPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [13] indicates whether hPPR mode is available (A13 = 1) or not available (A13 = 0). hPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is irrevocable so great care should be exercised when using.

Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [5] indicates whether sPPR mode is available (A5 = 1) or not available (A5 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is revocable by either doing a reset or power-down or by rewriting a new address in the same bank.

WRITE Preamble

Programmable WRITE preamble, t_{WPRE} , can be set to 1tCK or 2tCK via the MR4 register. The 1tCK setting is similar to DDR3. However, when operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble

Programmable READ preamble t_{RPRE} can be set to 1tCK or 2tCK via the MR4 register. Both the 1tCK and 2tCK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

READ Preamble Training

Programmable READ preamble training can be set to 1tCK or 2tCK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (t_{CAL}) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of $\lceil t_{CK}(ns)/t_{CAL}(ns) \rceil$.

Internal VREF Monitor

The device generates its own internal VREFDQ. This mode may be enabled during VREFDQ training, and when enabled, $V_{REF,time-short}$ and $V_{REF,time-long}$ need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

Mode Register 5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable 1 = Enable
A8:A6	RTT_PARK	(see Table 13)
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	(see Table 14)

Note:

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12. DBI is not allowed during MPR READ operations.

Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide RTT(NOM) termination. However, the device may provide RTT(Park) termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600,1866,2133
0	1	0	5	2400,2666
0	1	1	6	2933,3200
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Mode Register 6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	(see Table 15)
A9, A8	RFU	0 = must be programmed to 0 during MRS
A7	VrefDQ Training Enable	0 = Disable(Normal operation Mode) 1 = Enable(Training Mode)
A6	VrefDQ Training Range	(see Table 16)
A5:A0	VrefDQ Training Value	(see Table 17)

Note: 1. Reserved for Register control word setting . DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond.

tCCD_L & tDLLK

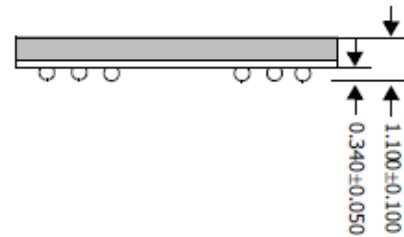
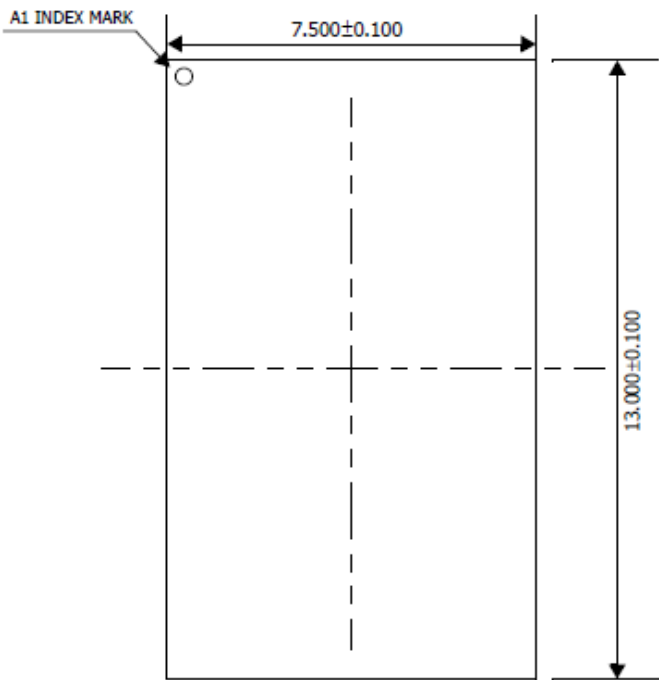
A12	A11	A10	tCCD_L.min (nCK) ¹	tDLLKmin (nCK) ¹	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≤ 2666Mbps (2666Mbps)
1	0	0	8		2666Mbps < Data rate ≤ 3200Mbps (2933/3200Mbps)
1	0	1	Reserved		
1	1	0			
1	1	1			

VREFDQ Training : Range

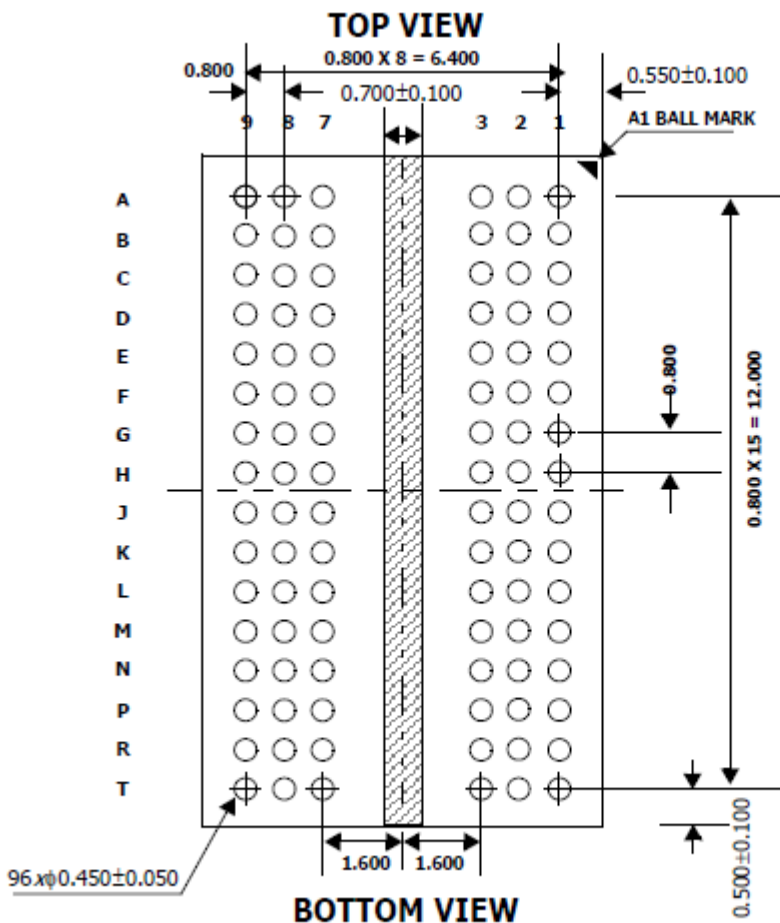
A6	VrefDQ Range
0	Range 1
1	Range 2

Package Description: 96Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



SIDE VIEW



BOTTOM VIEW

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2018	Rico Yang	N/A
1.0	First SPEC. release.	Aug. 2018	Rico Yang	N/A