

## 4Gb (64Mx8Banksx8) DDR3 SDRAM

### Descriptions

The 4Gb Double-Data-Rate-3 (DDR3) DRAMs is a high-speed CMOS Double Data Rate32 SDRAM Containing 4,294,967,296 bits. It is internally configured as an octal-bank DRAM.

The 4Gb chip is organized as 64Mbit x 8 I/O x 8 banks. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3 DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V power supply and are available in BGA packages.

### Features

- JEDEC Standard VDD/VDDQ = 1.5V±0.075V
- 8 Internal memory banks (BA0-BA2)
- Differential clock input (CK,/CK)
- Bust length: 4 with Burst Chop (BC) and 8.
- CAS Write Latency (CWL): 5, 6, 7, 8, 9
- CAS Latency (CL): 6, 7, 8, 9, 10, 11, 12, 13
- POSTED CAS ADDITIVE Programmable Additive Latency (AL): 0, CL-1, CL-2 clock
- Programmable Sequential / Interleave Burst Type
- 8n-bit prefetch architecture
- Output Driver Impedance Control
- Differential bidirectional data strobe
- Internal(self) calibration:Internal self calibration
- OCD Calibration
- Dynamic ODT (Rtt\_Nom & Rtt\_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS compliance and Halogen free
- Packages: 78-Balls BGA for x8 components

### Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A404G0866AD8C	512M X 8	DDR3-1333MHz 9-9-9	78Ball BGA, 9x10.5mm	Commercial
H2A404G0866AF8C	512M X 8	DDR3-1600MHz 11-11-11	78Ball BGA, 9x10.5mm	Commercial
H2A404G0866AG8C	512M X 8	DDR3-1866MHz 13-13-13	78Ball BGA, 9x10.5mm	Commercial

**Note:** Speed (tck\*) is in order of CL-T<sub>RCD</sub>-T<sub>RP</sub>

### Ball Assignments and Descriptions

78-Ball FBGA – x8 (Top View)

1	2	3		7	8	9
VSS	VDD	NC	A	NU,/TDQS	VSS	VDD
VSS	VSSQ	DQ0	B	DM,TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS	C	DQ1	DQ3	VSSQ
VSSQ	DQ6	/DQS	D	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	E	DQ7	DQ5	VDDQ
NC	VSS	/RAS	F	CK	VSS	NC
ODT	VDD	/CAS	G	/CK	VDD	CKE
NC	/CS	/WE	H	A10,AP	ZQ	NC
VSS	BA0	BA2	J	A15	VREFCA	VSS
VDD	A3	A0	K	A12,/BC	BA1	VDD
VSS	A5	A2	L	A1	A4	VSS
VDD	A7	A9	M	A11	A6	VDD
VSS	/RESET	A13	N	A14	A8	VSS

## 78-Ball FBGA - x8 Ball Descriptions

Pin	Symbol	Description
F7,G7	CK, /CK	<b>(System Clock)</b> CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK.
H2	/CS	<b>(Chip Select)</b> All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple memory ranks. /CS is considered part of the command code.
G9	CKE	<b>(Clock Enable)</b> CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK,/CK,ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
K3,L7,L3,K2, L8,L2,M8,M2, N8,M3,H7,M7, K7,N3,N7,J7	A0~A9,A10(AP), A11,A12(/BC ), A13,A14,A15	<b>(Address)</b> Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/□/BC have additional function as below. The address inputs also provide the op-code during Mode Register Set commands.
J2,K8,J3	BA0, BA1,BA2	<b>(Bank Address)</b> BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
G1	ODT	<b>(On Die Termination)</b> ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS,/DQS and DM/TDQS, NU/□/TDQS (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.

C3,D3	DQL,DQU, DQS,/DQS, DQSL,/DQSL, DQSU,/DQSU	<b>(Data Strobe)</b> output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS, DQSL, DQSU are paired with differential signals /DQS,/DQSL,/DQSU, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
B7,A7	TDQS, /TDQS	<b>(Termination Data Strobe)</b> When enabled via Mode Register A11=1 in <b>MR1</b> , DRAM will enable the same termination resistance function on TDQS /TDQS that is applied to DQS/DQS. When disabled via mode register A11=0 in <b>MR1</b> , DM/TDQS will provide the data mask function and /TDQS is not used.
F3, G3, H3	/RAS,/CAS, /WE	<b>(Command Inputs)</b> /RAS,/CAS and /WE (along with /CS) define the command being entered.
B3,C7,C2,C8,E3, E8,D2,E7	DQ0~7	<b>(Data Input/Output)</b> Bi-directional data bus.
A2,A9,D7,G2,G8, K1,K9,M1,M9/A1, A8,B1,D8,F2,F8, J1,J9,L1,L9,N1,N9	VDD,VSS	<b>(Power Supply/Ground)</b> VDD and VSS are power supply for internal circuits.
B9,C1,E2,E9 /B2,B8,C9,D1,D9	VDDQ VSSQ	<b>(DQ Power Supply/DQ Ground)</b> VDDQ and VSSQ are power supply for the output buffers.
H8	ZQ	<b>(ZQ Calibration)</b> Reference pin for ZQ calibration
N2	/RESET	<b>(Active Low Asynchronous Reset)</b> Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
E1	VREFDQ	<b>(Reference Voltage)</b> Reference voltage for DQ
J8	VREFCA	<b>(Reference Voltage)</b> Reference voltage for CA
A3,F1,H1,F9, H9	NC	<b>(No Connection)</b> No internal electrical connection is present.

Note: Input balls only BA0~BA2, A0~A13, /RAS, /CAS, /WE, /CS, CKE, ODT and /RESET do not supply termination.

### ***Absolute Maximum Ratings***

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.4 ~ +1.975		V
VDD	Power Supply Voltage	-0.4 ~ +1.975		V
VDDQ	Power Supply Voltage	-0.4 ~ +1.975		V
TOP	Operating Temperature Range	Commercial	0 ~ +85	°C
TSTG	Storage Temperature Range	-55 ~ +100		°C

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

### ***Recommended DC Operating Conditions***

Symbol	Parameter	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Power Supply Voltage	1.425	1.5	1.575	V
V <sub>DDQ</sub>	Power Supply for I/O Voltage	1.425	1.5	1.575	V

### Input/ Output Capacitance

Symbol	Parameters	Pins	Min.	Max.	Unit	Notes
CCK	Input pin capacitance, CK, /CK	CK, /CK	0.8	1.4	pF	1,3
CDCK	Delta input pin capacitance, CK, /CK		0	0.15	pF	1,2
CIN_CTRL	Input pin capacitance, control pins	/CS,CKE,ODT	0.75	1.3	pF	1
CDIN_CTRL	Delta input pin capacitance, control pins		-0.4	0.2	pF	1,4
CIN_ADD_CMD	Input pin capacitance, address and command pins	/RAS,/CAS,/WE, Address	0.75	1.3	pF	1
CDIN_ADD_CMD	Delta input pin capacitance, address and command pins		-0.4	0.4	pF	1,5
CIO	Input/output pins capacitance	DQ,DQS,/DQS TDQS,/TDQS, DM	1.4	2.5	pF	1,6
CDIO	Delta input/output pins capacitance		-0.5	0.3	pF	1,7,8
CDDQS	Delta input/output pins capacitance	DQS, /DQS	0	0.15	pF	1,10
CZQ	Input/output pin capacitance, ZQ	ZQ	-	3	pF	1,9

**Notes1:** VDD, VDDQ, VSS, VSSQ applied and all other pins (except the pin under test) floating. VDD = VDDQ =1.5V, VBIAS=VDD/2.

**Notes2:** Absolute value of CCK(CK-pin) - CCK(/CK-pin).

**Notes3:** CCK (min.) will be equal to CIN (min.)

**Notes4:** CDIN\_CTRL = CIN\_CTRL - 0.5\*(CCK(CK-pin) + CCK(/CK-pin))

**Notes5:** CDIN\_ADD\_CMD = CIN\_ADD\_CMD - 0.5\*(CCK(CK-pin) + CCK(/CK-pin))

**Notes6:** Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.

**Notes7:** DQ should be in high impedance state.

**Notes8:** CDIO = CIO (DQ, DM) - 0.5\*(CIO(DQS-pin) + CIO(/DQS-pin)).

**Notes9:** Maximum external load capacitance on ZQ pin is 5pF.

**Notes10:** Absolute value of CIO(DQS) - CIO(/DQS).

## Recommended DC Operating Conditions

VDD/VDDQ = 1.5V±0.075V

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I <sub>DD0</sub>	<b>Operating Current 0</b> One Bank Activate-> Precharge	29	28	27	mA
I <sub>DD1</sub>	<b>Operating One Bank Active-Read-Precharge Current:</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	44	43	42	mA
I <sub>DD2P1</sub>	<b>Precharge Power-Down Current Fast Exit:</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL:8; AL: 0; /CS: stable at 1; Command,Address: stable at 0; Data IO: FLOATING;DM:stable at 0;Bank Activity:all banks closed;Output Buffer and RTT:Enabled in Mode Registers;ODT Signal:stable at 0; Pre-charge Power Down Mode: Fast Exit	11	11	11	mA
I <sub>DD2N</sub>	<b>Precharge Standby Current:</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	17	16	15	mA
I <sub>DD3P</sub>	<b>Active Power-Down Current:</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	15	15	15	mA
I <sub>DD4W</sub>	<b>Operating Burst Write Current:</b> CKE:High; External clock:On; tCK, CL:see timing used table; BL: 8; AL:0; /CS:High between WR; Command, Address: partially toggling; Data IO:seamless write data burst with different data between one burst and the next one;DM: stable at 0; Bank Activity:all banks open, WR commands cycling through banks:0,0,1,1,2,2,...;Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	90	90	85	mA
I <sub>DD4R</sub>	<b>Operating Burst Read Current:</b> CKE:High;External clock:On; tCK, CL:see timing used table; BL: 8; AL:0; /CS:High between RD; Command, Address: par-tially toggling; Data IO:seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity:all banks open, RD commands cycling through banks:0,0,1,1,2,2,...;Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	90	90	85	mA

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I <sub>DD5B</sub>	<b>Burst Refresh Current:</b> CKE:High; External clock: On; tCK, CL, nRFC: see timing used table; BL:8; AL:0; /CS: High between REF; Command, Address: partially toggling; Data IO:FLOATING;DM: stable at 0; Bank Activity: REF command every nRFC;Output Buffer and RTT:Enabled in Mode Registers; ODT Signal: stable at 0	152	152	152	mA
I <sub>DD6</sub>	<b>Self Refresh Current: Normal Temperature Range;</b> TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	15	15	15	mA
I <sub>DD7</sub>	<b>Operating Bank Interleave Read Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	146	130	125	mA

**Note 1:** Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

**Note 2:** Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B; RTT\_Wr enable: set MR2 A[10,9] = 10B

**Note 3:** Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit

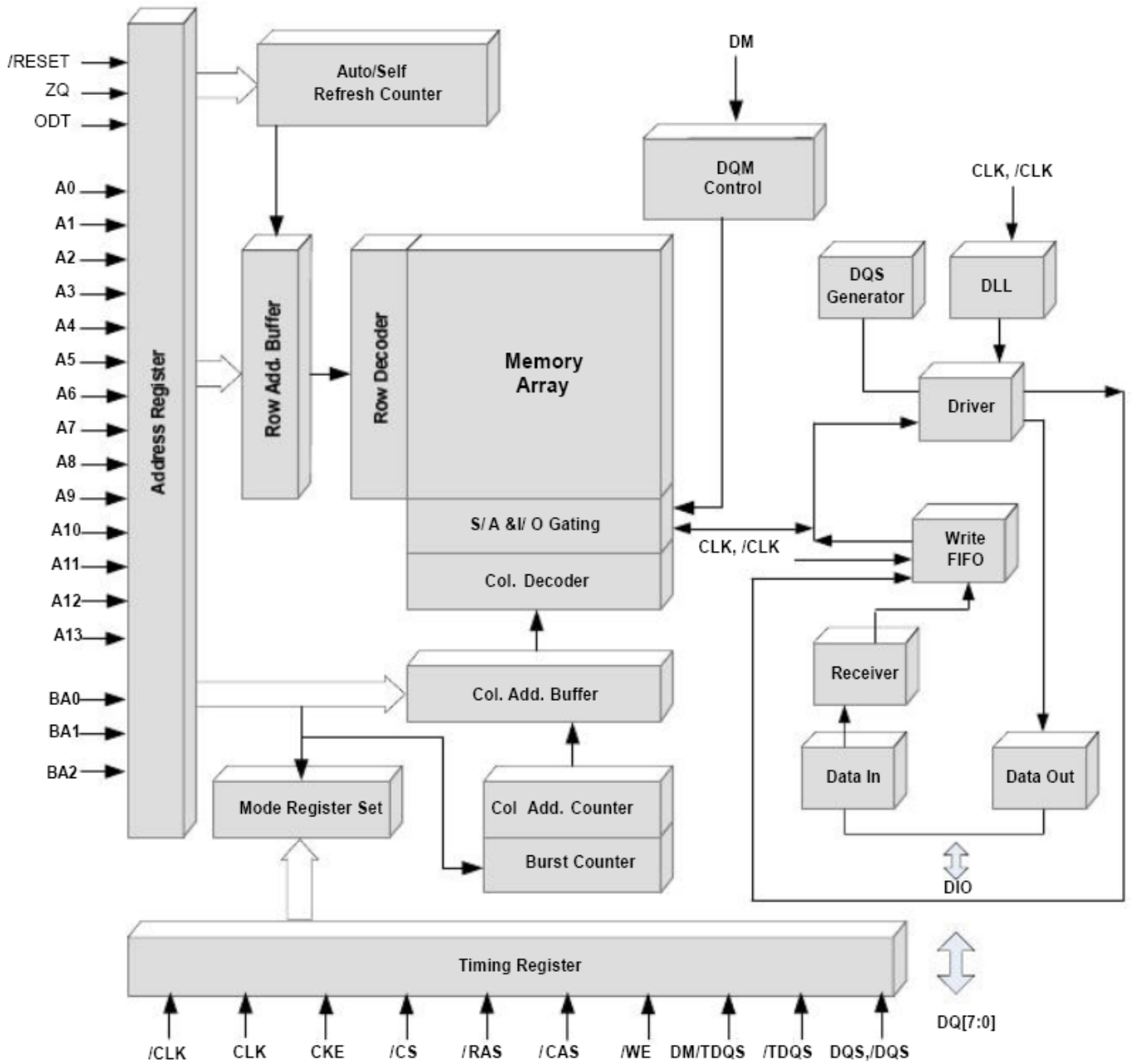
**Note 4:** Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

**Note 5:** Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range

**Note 6:** Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM

**Note 7:** Read Burst type : Nibble Sequential, set MR0 A[3]=0B

**Block Diagram**



## AC Operating Test Characteristics

### DDR3-1333 & DDR3-1600 & DDR3-1866 Speed Bins

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
tAA	Internal read command to first data	13.91	20	13.750	20	13.125	20	ns	8
tRCD	Active to read or write delay	13.91	-	13.750	-	13.125	-	ns	8
tRP	Precharge command period	13.91	-	13.750	-	13.125	-	ns	8
tRC	Active to active/auto refresh command	47.91	-	48.750	-	49.125	-	ns	8
tRAS	Active to precharge command period	34	9*tREFI	35	9*tREFI	36	9*tREFI	ns	7
tCK (AVG)	Average Clock Cycle, CL=6, CWL=5	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,5,6
tCK (AVG)	Average Clock Cycle, CL=7, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1,2,3,4,5,6
tCK (AVG)	Average Clock Cycle, CL=8, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1,2,3,5,6
tCK (AVG)	Average Clock Cycle, CL=9, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,4,6
tCK (AVG)	Average Clock Cycle, CL=10, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,6
tCK (AVG)	Average Clock Cycle, CL=11, CWL=8	1.25	<1.5	1.25	<1.5	-	-	ns	1,2,3
tCK (AVG)	Average Clock Cycle, CL=13, CWL=9	1.07	<1.25	-	-	-	-	ns	
-	Support CL Settings	6,7,8,9,10,11,13		6,7,8,9,10,11		6,7,8,9,10		nCK	
-	Support CWL Settings	5,6,7,8,9		5,6,7,8		5,6,7		nCK	

**Notes1:** The CL setting and CWL setting result in tCK (avg) (min.) and tCK (avg) (max.) requirements. When making a selection of tCK (avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

**Notes2:** tCK (avg) (min.) limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (avg) value (2.5, 1.875, 1.5, or 1.25ns) when calculating CL (nCK) = tAA (ns) / tCK (avg)(ns), rounding up to the next 'Supported CL'.

**Notes3:** tCK (avg) (max.) limits: Calculate tCK (avg) + tAA (max.)/CL selected and round the resulting tCK (avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is tCK (avg) (max.) corresponding to CL selected.

**Notes4:** 'Reserved' settings are not allowed. User must program a different value.

**Notes5:** Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.

**Notes6:** Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.

**Notes7:** tREFI depends on operating case temperature (TC).

**Notes8:** For devices supporting optional down binning to CL = 7 and CL = 9, tAA/tRCD/tRP(min.) must be 13.125 ns or lower. SPD settings must be programmed to match.

## AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9		
	Parameter	Min.	Min.	Min.	Max.	Min.	Max.	
tCK	Minimum clock cycle, DLL-off mode	8	-	8	-	8	-	ns
tCH, tCL (AVG)	Average CK high/low level width	0.47	0.53	0.47	0.53	0.47	0.53	ns
tRRD	Active bank A to active bank B command period	5	-	6	-	6	-	ns
		4	-	4	-	4	-	tCK
tFAW	Four Activate Window	27	-	30	-	30	-	ns
t <sub>IH</sub> (base) DC100	Address and Control input hold time (VIH/VIL(DC100) levels)	100	-	120	-	140	-	ps
t <sub>IS</sub> (base) AC175	Address and Control input setup time (VIH/VIL(AC175) levels)	-	-	45	-	65	-	ps
t <sub>IS</sub> (base) AC150	Address and Control input setup time (VIH/VIL(AC150) levels)	150	-	170	-	215	-	ps
t <sub>DH</sub> (base)	DQ and DM input hold time (VIH/VIL(DC) levels)	-	-	45	-	65	-	ps
t <sub>DS</sub> (base)	DQ and DM input setup time (VIH/VIL(AC) levels)	68	-	10	-	10	-	ps
t <sub>IPW</sub>	Address and control input pulse width for each input	535	-	560	-	620	-	ps

t <sub>DIPW</sub>	DQ and DM input pulse width for each input	320	-	360	-	400	-	ps
t <sub>HZ(DQ)</sub>	DQ high impedance time	-	195	-	225	-	250	ps
t <sub>LZ(DQ)</sub>	DQ low impedance time	-390	195	-450	225	-500	250	ps
t <sub>HZ(DQS)</sub>	DQS,/DQS high impedance time RL+BL/2 reference	-	195	-	225	-	250	ps
t <sub>LZ(DQS)</sub>	DQS,/DQS low impedance time RL-1 reference	-390	195	-450	225	-500	250	ps
t <sub>DQSQ</sub>	DQS,/DQS to DQ skew per group, per access	-	85	-	100	-	125	ps
t <sub>CCD</sub>	/CAS to /CAS command delay	4	-	4	-	4	-	nCK
t <sub>QH</sub>	DQ output hold time from DQS, /DQS	0.38	-	0.38	-	0.38	-	t <sub>CK</sub> (avg)
t <sub>DQSK</sub>	DQS,/DQS rising edge output access time from rising CK,/CK	-195	195	-225	225	-255	255	ps
t <sub>DQSS</sub>	DQS latch rising transitions to associated clock edges	-0.27	0.27	-0.27	0.27	-0.25	0.25	t <sub>CK</sub> (avg)
t <sub>DQSH</sub>	DQS input high pulse width	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub> (avg)

## AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9		
	Parameter	Min.	Min.	Min.	Max.	Min.	Max.	
t <sub>DSH</sub>	DQS falling edge hold time from rising CK	0.18	-	0.18	-	0.2	-	t <sub>CK</sub> (avg)
t <sub>DSS</sub>	DQS falling edge setup time to rising CK	0.18	-	0.18	-	0.2	-	t <sub>CK</sub> (avg)
t <sub>DQSL</sub>	DQS input low pulse width	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub> (avg)
t <sub>QSH</sub>	DQS output high time	0.40	-	0.40	-	0.40	-	t <sub>CK</sub> (avg)
t <sub>QSL</sub>	DQS output low time	0.40	-	0.40	-	0.40	-	t <sub>CK</sub> (avg)
t <sub>MRD</sub>	Mode register set command cycle	4	-	4	-	4	-	nCK
t <sub>MOD</sub>	Mode register set command update delay	15	-	15	-	15	-	ns
		12	-	12	-	12	-	nCK
t <sub>RPRE</sub>	Read preamble time	0.9	-	0.9	-	0.9	-	t <sub>CK</sub> (avg)
t <sub>RPST</sub>	Read postamble time	0.3	-	0.3	-	0.3	-	t <sub>CK</sub> (avg)
t <sub>WPRE</sub>	Write preamble time	0.9	-	0.9	-	0.9	-	t <sub>CK</sub> (avg)
t <sub>WPST</sub>	Write postamble time	0.3	-	0.3	-	0.3	-	t <sub>CK</sub> (avg)
t <sub>WR</sub>	Write recovery time	15	-	15	-	15	-	ns
t <sub>DAL(min)</sub>	Auto precharge write recovery+precharge time	WR + roundup[t <sub>TRP</sub> / t <sub>CK</sub> (avg)]						nCK
t <sub>MPPRR</sub>	Multi purpose register recovery time	1	-	1	-	1	-	nCK
t <sub>WTR</sub>	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns
		4	-	4	-	4	-	nCK
t <sub>TRTP</sub>	Internal read to precharge command delay	7.5	-	7.5	-	7.5	-	ns
		4	-	4	-	4	-	nCK
t <sub>CKESR</sub>	Minimum CKE low width for self-refresh entry to exit	t <sub>CKE</sub> (min) +1	-	t <sub>CKE</sub> (min) +1	-	t <sub>CKE</sub> (min) +1	-	nCK
t <sub>CKSRE</sub>	Valid clock requirement after self-refresh entry or power-down entry	10	-	10	-	10	-	ns
		5	-	5	-	5	-	nCK
t <sub>CKSRX</sub>	Valid clock requirement before self-refresh exit or power-down exit	10	-	10	-	10	-	ns
		5	-	5	-	5	-	nCK

## AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin CL-nRCD-nRP	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units
		13-13-13		11-11-11		9-9-9		
		Parameter	Min.	Min.	Min.	Max.	Min.	
t <sub>XS</sub>	Exit self-refresh to commands not requiring a locked DLL	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	ns
		5	-	5	-	5	-	nCK
t <sub>XS<sub>DLL</sub></sub>	Exit self-refresh to Commands requiring a locked DLL	t <sub>DLL</sub> (min)	-	t <sub>DLL</sub> (min)	-	t <sub>DLL</sub> (min)	-	nCK
t <sub>RFC</sub>	Auto-refresh to active/auto-refresh command	260	-	260	-	260	-	ns
t <sub>REFI</sub>	Average periodic refresh Interval 0°C ≤ T <sub>c</sub> ≤ +85°C	-	7.8	-	7.8	-	7.8	μs
t <sub>CKE</sub>	CKE minimum high and low pulse width	5	-	5	-	5.625	-	ns
		3	-	3	-	3	-	nCK
t <sub>XPR</sub>	Exit reset from CKE high to a valid command	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	ns
		5	-	5	-	5	-	nCK
t <sub>DLLK</sub>	DLL locking time	512	-	512	-	512	-	nCK
t <sub>PD</sub>	Power-down entry to exit time	t <sub>CKE</sub> (min)	9*t <sub>REFI</sub>	t <sub>CKE</sub> (min)	9*t <sub>REFI</sub>	t <sub>CKE</sub> (min)	9*t <sub>REFI</sub>	
t <sub>XP<sub>DLL</sub></sub>	Exit precharge power-down with DLL frozen to commands requiring a locked DLL	24	-	24	-	24	-	ns
		10	-	10	-	10	-	nCK
t <sub>XP</sub>	Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	6	-	6	-	6	-	ns
		3	-	3	-	3	-	nCK
t <sub>WRP<sub>DEN</sub></sub> (min)	Timing of WR command to power-down entry(BL8OTF, BL8MRS, BL4OTF)	WL + 4 + [t <sub>WR</sub> / t <sub>CK</sub> (avg)]						nCK
t <sub>WRP<sub>DEN</sub></sub> (min)	Timing of WR command to power-down entry (BC4MRS)	WL + 2 + [t <sub>WR</sub> / t <sub>CK</sub> (avg)]						nCK
t <sub>WRAP<sub>DEN</sub></sub>	Timing of WRA command to power-down entry (BL8OTF, BL8MRS, BL4OTF)	WL + 4 + WR + 1						-
t <sub>WRAP<sub>DEN</sub></sub>	Timing of WRA command to power-down entry (BC4MRS)	WL + 2 + WR + 1						-

## AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9		
	Parameter	Min.	Min.	Min.	Max.	Min.	Max.	
tREFPDEN	Timing of REF command to power-down entry	1	-	1	-	1	-	nCK
tMRSPDEN	Timing of MRS command to power-down entry	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	
tCPDED	Command pass disable delay	1	-	1	-	1	-	nCK
tACTPDEN	Timing of ACT command to power-down entry	1	-	1	-	1	-	nCK
tPRPDEN	Timing of PRE command to power-down entry	1	-	1	-	1	-	nCK
tRDPDEN	Timing of RD/RDA command to power-down entry	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
tAON	RTT turn-on	-195	195	-250	250	-300	300	ps
tAONPD	Asynchronous RTT turn-on delay (Power-down with DLL frozen)	2	8.5	2	8.5	2	8.5	ns
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)
tAOFPD	Asynchronous RTT turn-off delay (Power-down with DLL frozen)	2	8.5	2	8.5	2	8.5	ns
ODTH4	ODT high time without Write command or with write command and BC4	4	-	4	-	4	-	nCK
ODTH8	ODT high time with write Command and BL8	6	-	6	-	6	-	nCK
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)
tzQinit	Power-up and reset calibration time	512	-	512	-	512	-	tCK
tzQoper	Normal operation full calibration time	256	-	256	-	256	-	tCK
tzQCS	Normal operation short Calibration time	64	-	64	-	64	-	tCK
twLMRD	First DQS pulse rising edge after write leveling mode is programmed	40	-	40	-	40	-	nCK
twLDQSEN	DQS./DQS delay after write leveling mode is programmed	25	-	25	-	25	-	nCK
tRTW	Read to write command Delay (BC4MRS, BC4OTF)	RL+tcc D/2+ 2nCK- WL	-	RL+tcc D/2+ 2nCK- WL	-	RL+tcc D/2+ 2nCK- WL	-	

t <sub>RTW</sub>	Read to write command Delay (BL8MRS, BL8OTF)	RL +tcc D/2+ 2nCK- WL	-	RL +tcc D/2+ 2nCK- WL	-	RL+tcc D/2 + 2nCK- WL	-	
t <sub>RAP</sub>	Active to read with auto Precharge command delay	t <sub>RCD</sub> min	-	t <sub>RCD</sub> min	-	t <sub>RCD</sub> min	-	

## AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	(DDR3-1866)		(DDR3-1600)		(DDR3-1333)		Units
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9		
	Parameter	Min.	Min.	Min.	Max.	Min.	Max.	
tWLS	Write leveling setup time From rising CK,/CK crossing to rising DQS,/DQS crossing	140	-	165	-	195	-	ps
tWLH	Write leveling hold time From rising DQS,/DQS crossing to rising CK,/CK crossing	140	-	165	-	195	-	ps
tWLO	Write leveling output delay	0	7.5	0	7.5	0	9	ns
tWLOE	Write leveling output error	0	2	0	2	0	2	ns
tCK (abs)	Absolute clock period	tCK (avg)min+ tJIT(per)min	tCK (avg)max + tJIT (per)max	tCK (avg)min+ tJIT(per)min	tCK (avg)max + tJIT (per)max	tCK (avg)min+ tJIT (per)min	tCK (avg)max + tJIT (per)max	ps
tCH (abs)	Absolute clock high pulse width	0.43	-	0.43	-	0.43	-	tCK (avg)
tCL (abs)	Absolute clock low pulse width	0.43	-	0.43	-	0.43	-	tCK (avg)
tJIT (per)	Clock period jitter	-60	60	-70	70	-80	80	ps
tJIT (per,lck)	Clock period jitter during DLL locking period	-50	50	-60	60	-70	70	ps
tJIT (cc)	Cycle to cycle period jitter	120		140		160		ps
tJIT (cc,lck)	Cycle to cycle period jitter During DLL locking period	100		120		140		ps
tERR (nper)	Cumulative error across n= 2,14,... 49,50 cycles	$tERR (nper)min=(1+0.68ln(n))*tJIT (per)min$ $tERR (nper)max=(1+0.68ln(n))*tJIT (per)max$						ps
tANPD	ODT to power-down entry/ exit latency	WL-1	-	WL-1	-	WL-1	-	nCK
ODTLon	ODT turn on latency	WL-2	WL-2	WL-2	WL-2	WL-2	WL-2	nCK
ODTLoff	ODT turn off latency	WL-2	WL-2	WL-2	WL-2	WL-2	WL-2	nCK
ODTLcwnw	ODT latency for changing from RTT_Nom to RTT_WR	WL-2	WL-2	WL-2	WL-2	WL-2	WL-2	nCK
ODTL cwn4	ODT latency for changing from RTT_WR to RTT_Nom (BC4)	-	4+ODTLoff	-	4+ODTLoff	-	4+ODTLoff	nCK
ODTL cwn8	ODT latency for changing from RTT_WR to RTT_Nom (BL8)	-	6+ODTLoff	-	6+ODTLoff	-	6+ODTLoff	nCK

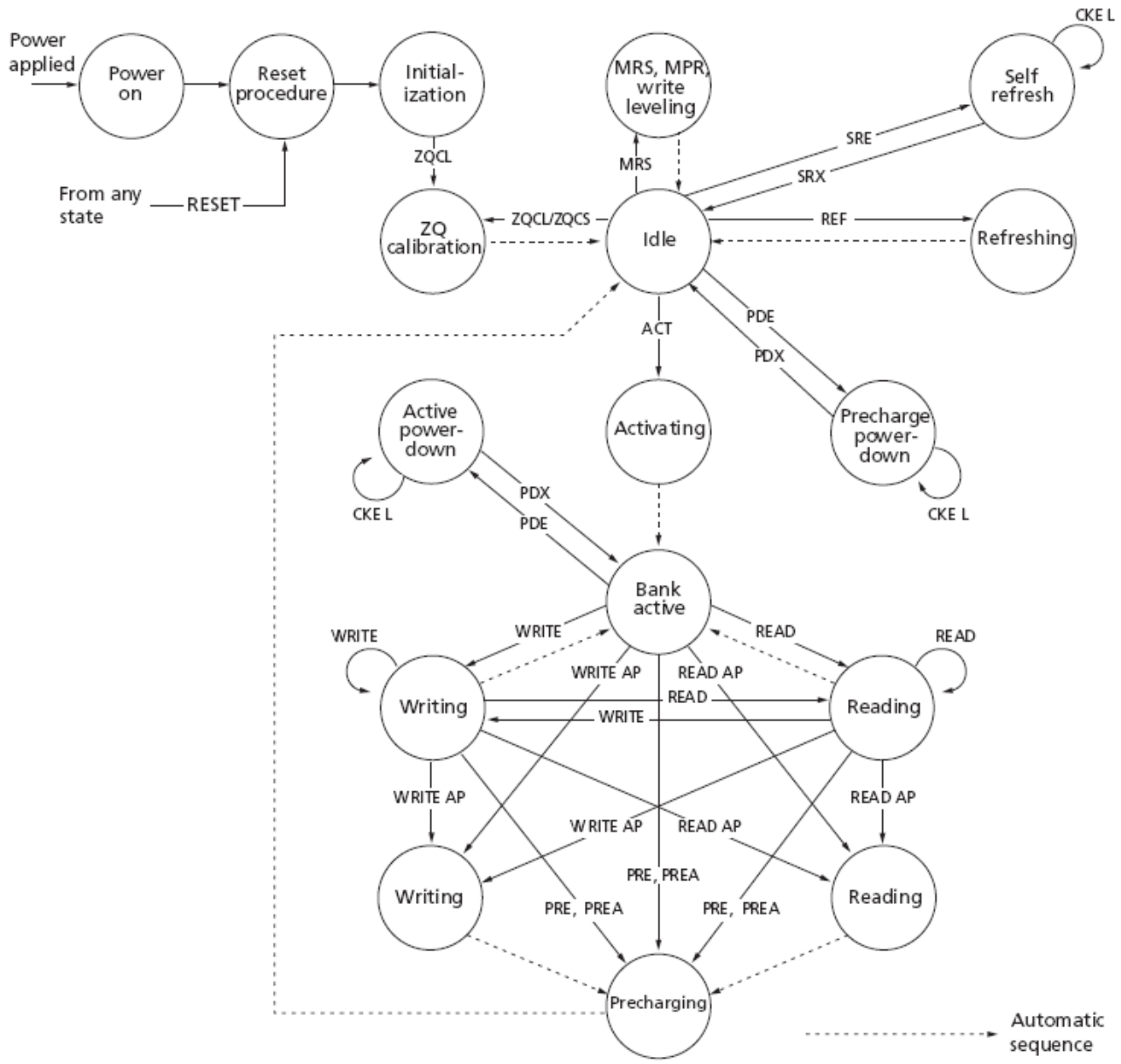
- Note 1:** Actual value dependant upon measurement level definitions which are TBD.
- Note 2:** Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
- Note 3:** The max values are system dependent.
- Note 4:** WR as programmed in mode register.
- Note 5:** Value must be rounded-up to next higher integer value.
- Note 6:** There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
- Note 7:** ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.
- Note 8:** ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.
- Note 9:** tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
- Note 10:** WR in clock cycles as programmed in MR0.
- Note 11:** The maximum read postamble is bound by tDQCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
- Note 12:** Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
- Note 13:** Value is only valid for RON34.
- Note 14:** Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
- Note 15:** tREFI depends on operating case temperature (Tc).
- Note 16:** tIS(base) and tIH(base) values are for 1V/ns command/ addresss single-ended slew rate and 2V/ns CK, /CK differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.
- Note 17:** tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. Note for DQ and DM signals, VREF(DC)= VREFDQ(DC).For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and and Slew Rate Derating section.
- Note 18:** Start of internal write transaction is defined as follows ;  
For BL8 (fixed by MRS and on-the-fly, OTF) : Rising clock edge 4 clock cycles after WL.  
For BC4 (on-the-fly, OTF) : Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
- Note 19:** The maximum read preamble is bound by tLZDQS(min) on the left side and tDQCK(max) on the right side.
- Note 20:** CKE is allowed to be registered low while operations such as row activation, precharge, auto precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
- Note 21:** Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
- Note 22:** Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
- Note 23:** One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the "Output Driver Voltage and Temperature Sensitivity" and "ODT Voltage and Temperature Sensitivity" tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS ommands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where  $TSens = \max(dRTTdT, dRONdTM)$  and  $VSens = \max(dRTTdV, dRONdVM)$  define the SDRAM temperature and voltage sensitivities.

- Note 24:** The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point  $[(175 \text{ mV} - 150 \text{ mV}) / 1 \text{ V/ns}]$ .
- Note 25:** Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
- Note 26:**  $t_{DQSL}$  describes the instantaneous differential input low pulse width on DQS - /DQS, as measured from one falling edge to the next consecutive rising edge.
- Note 27:**  $t_{DQSH}$  describes the instantaneous differential input high pulse width on DQS - /DQS, as measured from one rising edge to the next consecutive falling edge.
- Note 28:**  $t_{DQSH,act} + t_{DQSL,act} = 1 t_{CK,act}$  ; with  $t_{XYZ,act}$  being the actual measured value of the respective timing parameter in the application.
- Note 29:**  $t_{DSSH,act} + t_{DSS,act} = 1 t_{CK,act}$  ; with  $t_{XYZ,act}$  being the actual measured value of the respective timing parameter in the application.
- Note 30:**  $t_{CH(abs)}$  is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
- Note 31:**  $t_{CL(abs)}$  is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
- Note 32:** n = from 13 cycles to 50 cycles. This row defines 38 parameters.

**Simplified State Diagram**



-----> Automatic sequence  
 -----> Command sequence

ACT = ACTIVATE  
 MPR = Multipurpose register  
 MRS = Mode register set  
 PDE = Power-down entry  
 PDX = Power-down exit  
 PRE = PRECHARGE

PREA = PRECHARGE ALL  
 READ = RD, RDS4, RDS8  
 READ AP = RDAP, RDAPS4, RDAPS8  
 REF = REFRESH  
 RESET = START RESET PROCEDURE  
 SRE = Self refresh entry

SRX = Self refresh exit  
 WRITE = WR, WRS4, WRS8  
 WRITE AP = WRAP, WRAPS4, WRAPS8  
 ZQCL = ZQ LONG CALIBRATION  
 ZQCS = ZQ SHORT CALIBRATION

**Command Truth Table**

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0~BA2	A10	A12, A10~A0
		n-1	N							
Device Deselect	DES	H	H	H	X	X	X	X	X	X,X
No Operation	NOP	H	H	L	H	H	H	V	V	V,V
Read (fixed BL8/BC4)	RD	H	H	L	H	L	H	BA	L	V,CA
Read (BC4, OTF)	RDS4	H	H	L	H	L	H	BA	L	L,CA
Read (BL8, OTF)	RDS8	H	H	L	H	L	H	BA	L	H,CA
Read with Auto Pre-charge (fixed BL8/BC4)	RDA	H	H	L	H	L	H	BA	H	V,CA
Read with Auto Pre-charge (BC4, OTF)	RDAS4	H	H	L	H	L	H	BA	H	L,CA
Read with Auto Pre-charge (BL8, OTF)	RDAS8	H	H	L	H	L	H	BA	H	H,CA
Write (fixed BL8/BC4)	WR	H	H	L	H	L	L	BA	L	V,CA
Write (BC4, OTF)	WRS4	H	H	L	H	L	L	BA	L	L,CA
Write (BL8,OTF)	WRS8	H	H	L	H	L	L	BA	L	H,CA
Write with Auto Pre-charge (fixed BL8/BC4)	WRA	H	H	L	H	L	L	BA	H	V,CA
Write with Auto Pre-charge (BC4, OTF)	WRAS4	H	H	L	H	L	L	BA	H	L,CA
Write with Auto Pre-charge (BL8, OTF)	WRAS8	H	H	L	H	L	L	BA	H	H,CA
Bank Activate	ACT	H	H	L	L	H	H	BA	RA	
Pre-charge Single Bank	PRE	H	H	L	L	H	L	BA	L	V,V
Pre-charge All Banks	PREA	H	H	L	L	H	L	V	H	V,V
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code	
Refresh	REF	H	H	L	L	L	H	V	V	V,V
Self Refresh entry	SRE	H	L	L	L	L	H	V	V	V,V
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X,X
				L	H	H	H	V	V	V,V
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X,X
		H	L	L	H	H	H	V	V	V,V
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X,X
		L	H	L	H	H	H	V	V	V,V
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	H	X,X
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	L	X,X

H = High level, L = Low level, X = Don't care, V = Valid, BA=Bank Address, CA=Column Address, RA=Row Address

- Note1:** All DDR3 SDRAM commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
- Note2:** /RESET is low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Note3:** Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
- Note4:** "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
- Note5:** Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly (OTF) BL will be defined by MRS.
- Note6:** The Power Down Mode does not perform any refresh operation.
- Note7:** The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- Note8:** Self Refresh Exit is asynchronous.
- Note9:** VREF(Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
- Note10:** The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
- Note11:** The Deselect command performs the same function as No Operation command.
- Note12:** Refer to the CKE Truth Table for more detail with CKE transition.

## CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18
For more details with all signals, see "Command Truth Table"					10

**Note1:** CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

**Note2:** Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.

**Note3:** Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.

**Note4:** All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

**Note5:** The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

**Note6:** During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

**Note7:** DESELECT and NOP are defined in the "Command Truth Table".

**Note8:** On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

**Note9:** Self-Refresh mode can only be entered from the All Banks Idle state.

**Note10:** Must be a legal command as defined in the "Command Truth Table".

**Note11:** Valid commands for power-down entry and exit are NOP and DESELECT only.

**Note12:** Valid commands for self-refresh exit are NOP and DESELECT only.

**Note13:** Self-Refresh can not be entered during Read or Write operations.

**Note14:** The Power-Down does not perform any refresh operations.

**Note15:** "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

**Note16:** VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh.operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.

**Note17:** If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

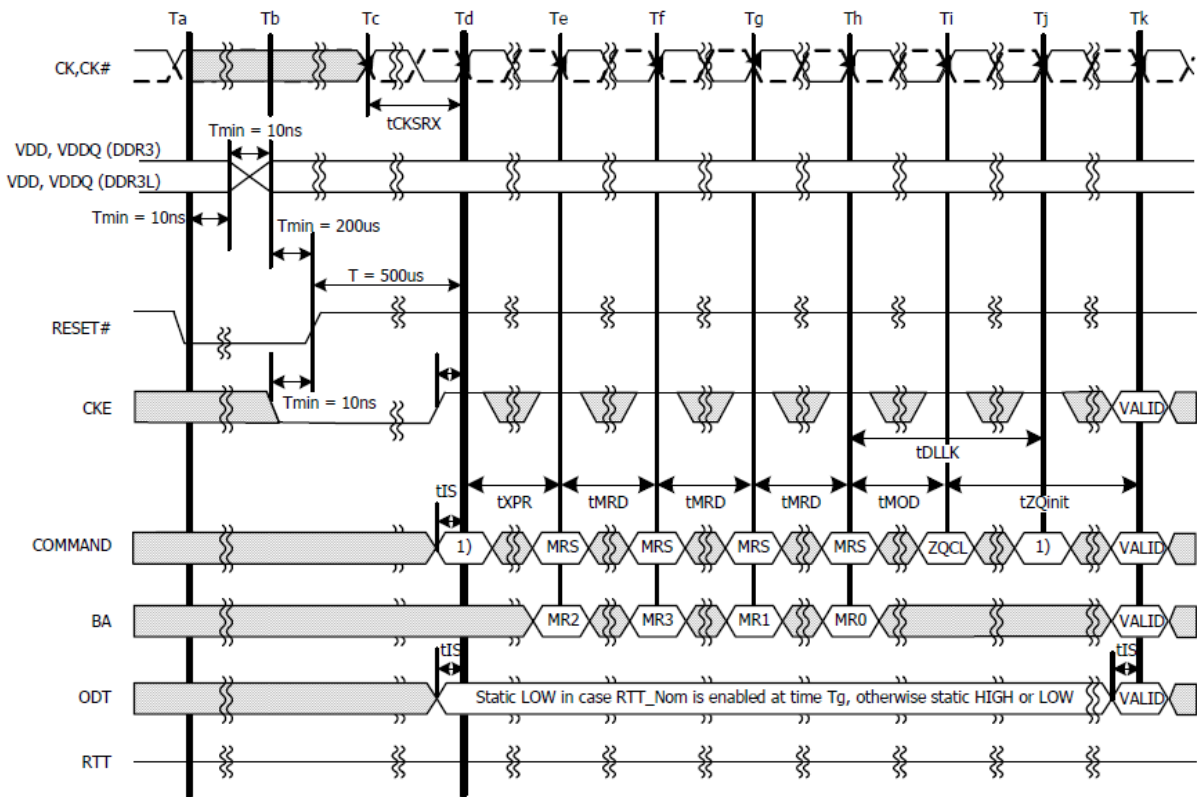
**Note18:** 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

## Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below  $0.2 \times VDD$ ; all other inputs may be undefined). /RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp,  $VDD > VDDQ$  and  $(VDD - VDDQ) < 0.3$  volts.
  - VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
  - Vref tracks VDDQ/2. OR
  - Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT\_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ( $tXPR = \max(tXS ; 5 \times tCK)$ )
6. Issue MRS Command to load **MR2** with all application settings. (To issue MRS command for **MR2**, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load **MR3** with all application settings. (To issue MRS command for **MR3**, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load **MR1** with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load **MR0** with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

### Reset and Power up initialization sequence



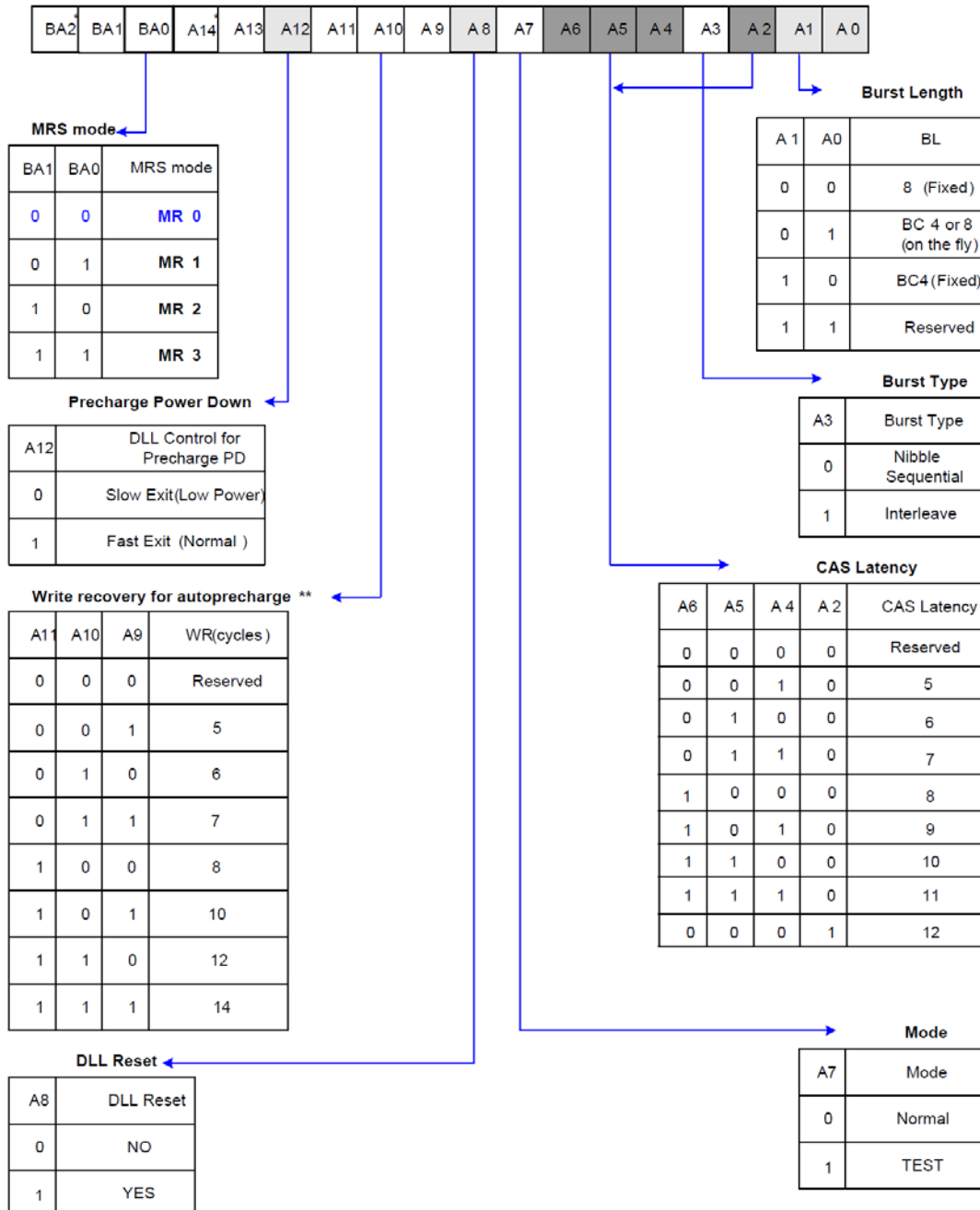
NOTE 1: From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

|| TIME BREAK    ■ DON'T CARE

## Mode Register Definition

### Mode Register MR0

The Mode Register **MR0** stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below



**Note1:** BA2 and A14 are reserved for future use and must be set to 0 when programming the MR.

**Note2:** WR(write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR(ns) by tCK( ns) and rounding up to the next integer :

$Wrmin[ \text{cycles} ] = \text{Roundup}(tWR / tCK)$ . The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

### Burst Type (A3)

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

**Note1:** In case of burst length being fixed to 4 by *MRO* setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12 (/BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

**Note2:** 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

**Note3:** T: Output driver for data and strobes are in high impedance.

**Note4:** V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

**Note5:** X: Don't Care.

## **CAS Latency**

The CAS Latency is defined by **MRO** (bits A9-A11). CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL);  $RL = AL + CL$ .

## **Test Mode**

The normal operating mode is selected by **MRO** (bit A7 = 0) and rest bits set to the desired values. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM factory and should NOT be used. No operations or functionality is specified if A7 = 1.

## **DLL Reset**

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

## **Write Recovery**

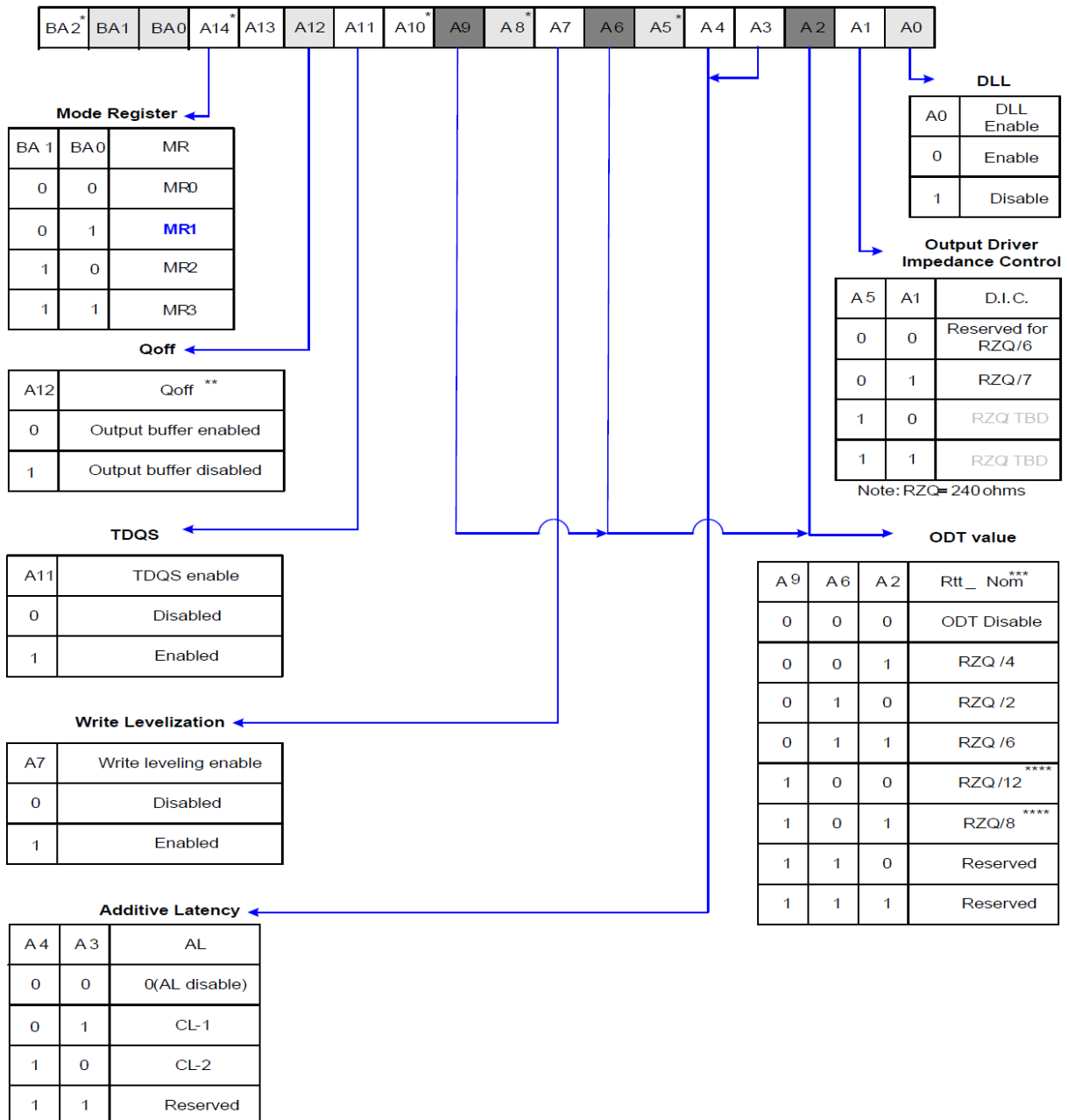
The programmed WR value **MRO** (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:  $WR_{min}[cycles] = Roundup(tWR[ns] / tCK[ns])$ . The WR must be programmed to be equal to or larger than tWR(min).

## **Precharge PD DLL**

**MRO** (bit A12) is used to select the DLL usage during precharge power-down mode. When **MRO** (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When **MRO** (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

## Mode Register MR1

The Mode Register **MR1** stores the data for enabling or disabling the DLL, output driver strength, RTT\_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



**Note1:** BA2 ,A5 ,A8 ,A10 , and A13 are reserved for future use and must be set to 0 when programming the MR.

**Note2:** Outputs disabled DQs, DQSs, /DQSs

**Note3:** In Write leveling Mode(MR1[ bit7]=1)with MR1[bit12]=1,all RTT\_ Nom settings are allowed ; in Write Leveling Mode (MR1 [ bit 7 ]= 1 ) with MR1[ bit12]=0,only RTT\_ Nom settin gof RZQ /2,RZQ/4,and RZQ/6 are allowed.

**Note4:** If RTT\_ Nom is used during Writes, only the values RZQ/2,RZQ/4,RZQ/6 are allowed.

## ***DLL Enable***

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with **MR1** (A0 = 0), the DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT\_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refers to “DLL-off Mode”. The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT\_Nom bits **MR1**{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode. The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt\_WR, **MR2** {A10, A9} = {0,0}, to disable Dynamic ODT externally.

## ***ODT Rtt Values***

DDR3 SDRAM is capable of providing two different termination values (Rtt\_Nom and Rtt\_WR). The nominal termination value Rtt\_Nom is programmed in MR1. A separate value (Rtt\_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled.

## ***Additive Latency***

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, It allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings.

### ***Write Leveling***

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

### ***Output Disable***

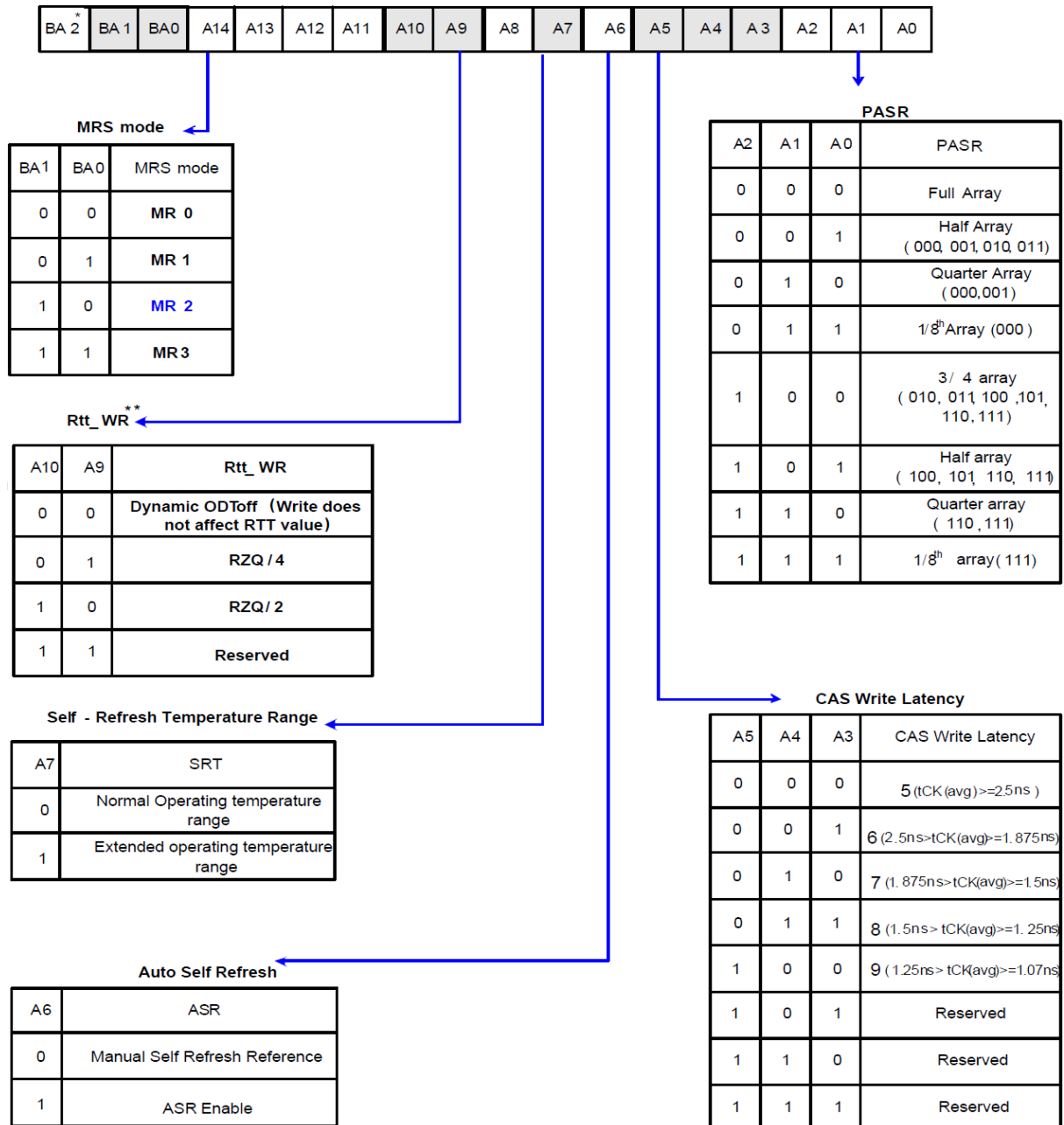
The outputs may be enabled/disabled by MR1 (bit A12). When this feature is enabled (A12 = 1), all output pins (DQs, DQS, /DQS, etc.) are disconnected from the device, thus removing any loading of the output drivers. For normal operation, A12 should be set to '0'.

### ***TQS, /TDQS***

TDQS (Termination Data Strobe) provides additional termination resistance outputs that may be useful in some system configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS & /TDQS pins that is applied to the DQS & /DQS pins. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS. The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the /TDQS pin is not used.

## Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, including RTT\_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



**Note1:** BA2 , A5 , A8, A 11-A14 are reserved for future use and must be set to 0 when programming the MR.

**Note2:** The Rtt\_WR value can be applied during writes even when Rtt\_ Nom is disabled . During write leveling, Dynamic ODT is not available

### CAS Write Latency (CWL)

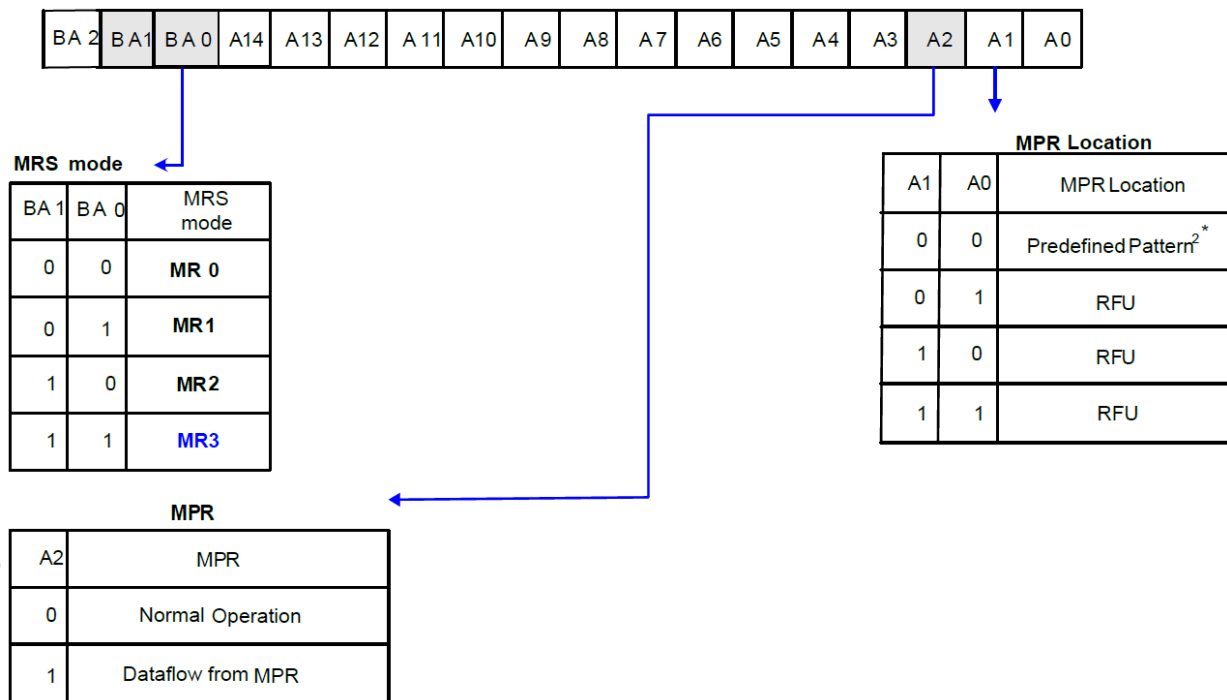
The CAS Write Latency is defined by **MR2** (bits A3-A5). CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL);  $WL = AL + CWL$ .

### Dynamic ODT (Rtt<sub>WR</sub>)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. **MR2** Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT<sub>Nom</sub> is available.

### Mode Register MR3

The Mode Register **MR3** controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



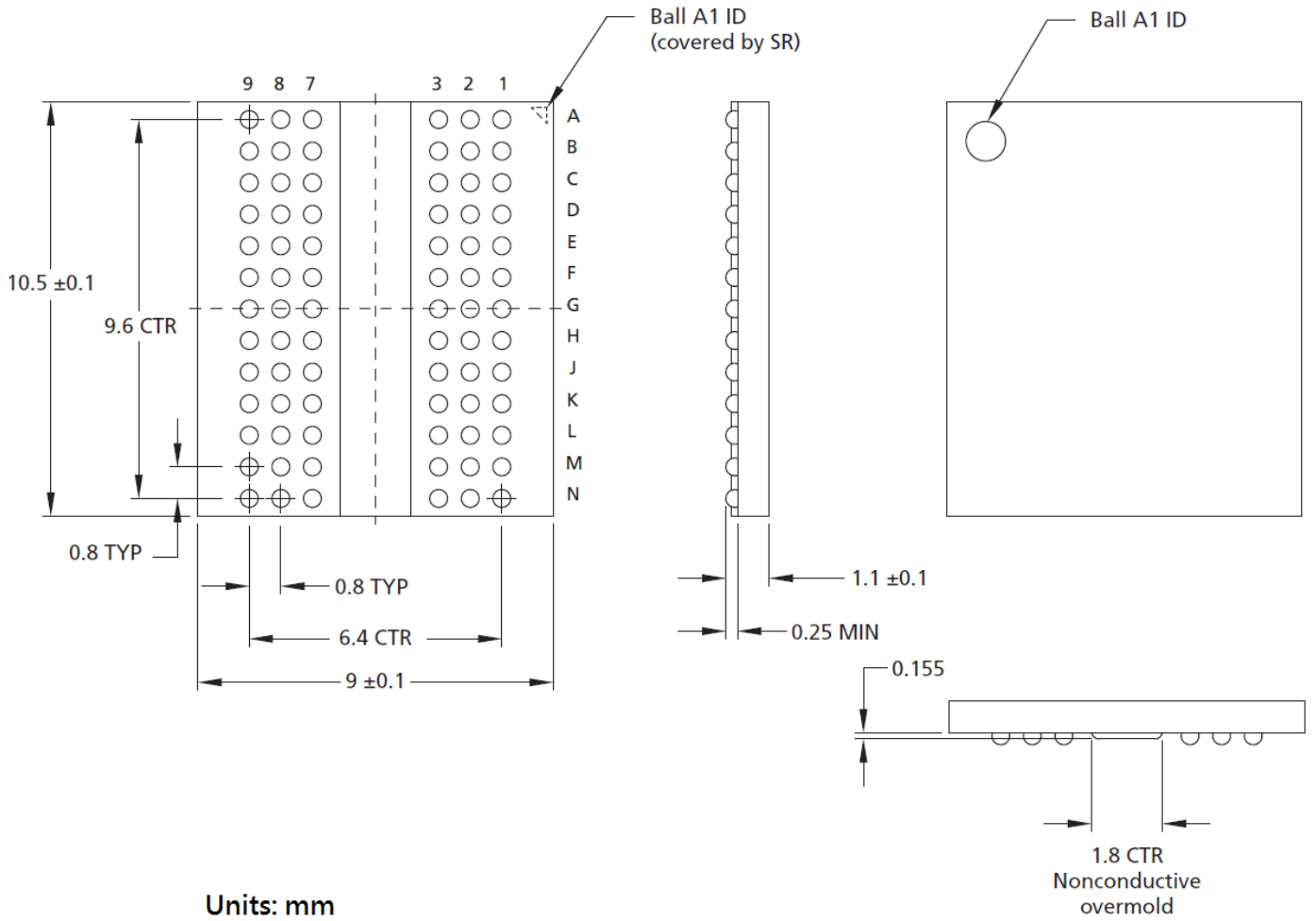
**Note1:** BA2,A3-A14are reserved for future use and must be set to 0 when programming the MR.

### Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to **MR3** Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (**MR3** bit A2 = 0). Power-down mode, self-refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

**Package Description: 78Ball-FBGA**

**Solder ball: Lead free (Sn-Ag-Cu)**



**Revision History**

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Aug. 2014	Ternence Chen	N/A
1.0	First SPEC. release.	Aug. 2014	Ternence Chen	N/A
2.1	Add 1866MHz definition	Aug. 2017	Hermon Chen	N/A