2Gb (16Mx8Banksx16) DDR3 SDRAM

Descriptions

The H2A402G1666C is a high speed Double Date Rate 3 (DDR3) low voltage Synchronous DRAM fabricated with ultra high performance CMOS process containing 2,147,483,648 bits which organized as 16Mbits x 8 banks by 16 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin (DDR3-1866) for general applications. The chip is designed to comply with the following key DDR3 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) On Die Termination, (4) programmable driver strength data,(5) seamless BL4 access with bank-grouping. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional differential data strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style. The 2Gb DDR3 devices operates with a single power supply: 1.5V±0.075V VDD and VDDQ.

Features

- JEDEC Standard VDD/VDDQ = 1.5V±0.075V
- All inputs and outputs are compatible with SSTL_15 interface.
- Fully differential clock inputs (CK, /CK) operation.
- Eight Banks
- Posted CAS by programmable additive latency
- Bust length: 4 with Burst Chop (BC) and 8.
- CAS Write Latency (CWL): 5, 6, 7, 8
- CAS Latency (CL): 6, 7, 8, 9, 10, 11,13
- Write Latency (WL) =Read Latency (RL) -1.
- Bi-directional Differential Data Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available both for 8 & 4 with BC.
- Multi Purpose Register (MPR) for pre-defined pattern read out
- On Die Termination (ODT) options: Synchronous ODT, Dynamic ODT, and Asynchronous ODT
- Auto Refresh and Self Refresh
- Refresh Interval: 7.8us Tcase between -40°C ~ 85°C
  Refresh Interval: 3.9us Tcase between 85°C ~ 95°C
- RoHS Compliance

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A402G1666CDMC	128M X 16	DDR3-1333MHz 9-9-9	96Ball BGA, 8x14mm	Commercial
H2A402G1666CFMC	128M X 16	DDR3-1600MHz 11-11-11	96Ball BGA, 8x14mm	Commercial
H2A402G1666CGMC	128M X 16	DDR3-1866MHz 13-13-13	96Ball BGA, 8x14mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

96-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDDQ	DQU5	DQU7	A	DQU4	VDDQ	VSS
VSSQ	VDD	VSS	B	/DQSU	DQU6	VSSQ
VDDQ	DQU3	DQU1	C	DQSU	DQU2	VDDQ
VSSQ	VDDQ	DMU	D	DQU0	VSSQ	VDD
VSS	VSSQ	DQL0	E	DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL	F	DQL1	DQL3	VSSQ
VSSQ	DQL6	/DQSL	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4	H	DQL7	DQL5	VDDQ
NC	VSS	/RAS	J	CK	VSS	NC
ODT	VDD	/CAS	K	/CK	VDD	CKE
NC	/CS	/WE	L	A10 , AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12 , /BC	BA1	VDD
VSS	A5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	/RESET	A13	T	NC	A8	VSS

96-Ball FBGA – x16 Ball Descriptions

Pin	Symbol	Description
J7,K7	CK, /CK	**(System Clock)** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK . Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
L2	/CS	**(Chip Select)** All commands are masked when /CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
K9	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self- refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including self-refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self -refresh.
N3,P7,P3,N2, P8,P2,R8,R2, T8,R3,L7,R7, N7,T3	A0~A9,A10(AP), A11,A12(/BC), A13	**(Address)** Provided the row address (RA0 – RA13) for active commands and the column address (CA0-CA9) and auto precharge bit for read/write commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). The address inputs also provide the op-code during Mode Register Set commands. A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
M2,N8,M3	BA0, BA1,BA2	**(Bank Address)** BA0 – BA2 define to which bank an active, read, write or precharge command is being applied. Bank address also determines if the mode register is to be accessed during a MRS cycle.
K1	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS , DM/TDQS, and TDQS signal. The ODT pin will be ignored if the Mode Register ***MR1*** is programmed to disable ODT.

E3, F7, F2, F8, H3, H8, G2, H7, D7, C3, C8, C2 F3, G3, C7, B7	DQL, DQU, DQS, /DQS DQSL /DQSL DQSU,/DQSU	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, DQSU are paired with differential signals /DQS, /DQSL, /DQSU to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
D3,E7	/DMU, DML	**(Termination Data Strobe)** When enabled via Mode Register A11=1 in ***MR1***, DRAM will enable the same termination resistance function on TDQS /TDQS that is applied DQS/DQS. When disabled via mode register A11=0 in ***MR1***, DM/TDQS will provide the data mask function and /TDQS is not used.
J3, K3, L3	/RAS ,/CAS , /WE	**(Command Inputs)** /RAS , /CAS and /WE (along with /CS) define the command being entered.
E3, F7, F2, F8, H3, H8, G2, H7	DQL0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
E1, N1, R1, T1, B2, J2, K2,B3, G7, J8, K8, A9, D9,M9, N9, P9, R9, T9	VDD,VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
A1, C1, F1, D2, H2, A8, C9,E9, H9, B1, D1, G1, E2, C8,E8, B9, F9, G9	VDDQ VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
L8	ZQ	**(ZQ Calibration)** Reference pin for ZQ calibration

N2	/RESET	**(Active Low Asynchronous Reset)** Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VD i.e. 1.20V for DC high and 0.30V for DC low.
H1	VREFDQ	**(Reference Voltage)** Reference voltage for DQ
M8	VREFCA	**(Reference Voltage)** Reference voltage for CA
J1, L1, T7, J9, L9	NC	**(No Connection)** No internal electrical connection is present.

Note: Input balls only BA0~BA2, A0~A15, /RAS, /CAS, /WE, /CS, CKE, ODT and /RESET do not supply termination.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
VIN, VOUT	Input, Output Voltage	-0.4 ~ +1.975		V
VDD	Power Supply Voltage	-0.4 ~ +1.975		V
VDDQ	Power Supply Voltage	-0.4 ~ +1.975		V
TOP	Operating Temperature Range	Commercial	0 ~ +85	°C
TSTG	Storage Temperature Range	-55 ~ +155		°C

Note: 1. VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 × VDDQ. When VDD and VDDQ are <500mV, VREF can be ≤300mV.

2. MAX operating case temperature. TC is measured in the center of the package.

3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Power Supply for I/O Voltage	1.425	1.5	1.575	V

Note: 1. VDD and VDDQ must track one another. VDDQ must be ≤ VDD. VSS = VSSQ.

2. VDD and VDDQ may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.

Input/ Output Capacitance

Symbol	Parameters	Pins	Min.	Max.	Unit	Notes
CCK	Input pin capacitance, CK, /CK	CK, /CK	0.8	1.4	pF	1,3
CDCK	Delta input pin capacitance, CK, /CK		0	0.15	pF	1,2
CIN_CTRL	Input pin capacitance, control pins	/CS,CKE,ODT	0.75	1.3	pF	1
CDIN_CTRL	Delta input pin capacitance, control pins		-0.4	0.2	pF	1,4
CIN_ADD_CMD	Input pin capacitance, address and command pins	/RAS,/CAS,/WE, Address	0.75	1.3	pF	1
CDIN_ADD_CMD	Delta input pin capacitance, address and command pins		-0.4	0.4	pF	1,5
CIO	Input/output pins capacitance	DQ,DQS,/DQS TDQS,/TDQS, DM	1.5	2.5	pF	1,6
CDIO	Delta input/output pins capacitance		-0.5	0.3	pF	1,7,8
CDDQS	Delta input/output pins capacitance	DQS, /DQS	0	0.15	pF	1,10
CZQ	Input/output pin capacitance, ZQ	ZQ	-	3	pF	1,9

Notes1: VDD, VDDQ, VSS, VSSQ applied and all other pins (except the pin under test) floating. VDD = VDDQ =1.5V, VBIAS=VDD/2.

Notes2: Absolute value of CCK(CK-pin) - CCK(/CK-pin).

Notes3: CCK (min.) will be equal to CIN (min.)

Notes4: CDIN_CTRL = CIN_CTRL - 0.5*(CCK(CK-pin) + CCK(/CK-pin))

Notes5: CDIN_ADD_CMD = CIN_ADD_CMD - 0.5*(CCK(CK-pin) + CCK(/CK-pin))

Notes6: Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.

Notes7: DQ should be in high impedance state.

Notes8: CDIO = CIO (DQ, DM) - 0.5*(CIO(DQS-pin) + CIO(/DQS-pin)).

Notes9: Maximum external load capacitance on ZQ pin is 5pF.

Notes10: Absolute value of CIO(DQS) - CIO(/DQS).

Recommended DC Operating Conditions

VDD/VDDQ = 1.5V±0.075V

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I_{DD0}	**Operating One Bank Active-Precharge Current:** CKE: High; External clock: On; BL: 8(1); AL: 0;/CS : High between ACT and PRE; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0, 0, 1,1,2,2... Output Buffer and RTT: Enabled in Mode Registers (2); ODT Signal: stable at 0.	51	49	48	mA
I_{DD1}	**Operating One Bank Active-Read-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	72	69	67	mA
I_{DD2P1}	**Precharge Power-Down Current Fast Exit:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	15	15	15	mA
I_{DD2N}	**Precharge Standby Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	23	23	23	mA
I_{DD3P}	**Active Power-Down Current:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	22	22	22	mA
I_{DD4W}	**Operating Burst Write Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	164	146	127	mA
I_{DD4R}	**Operating Burst Read Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between RD; Command, Address: par-tially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	155	135	115	mA

Symbol	Parameter & Test Conditions	1866	1600	1333	Units
		Max			
I_{DD5B}	**Burst Refresh Current:** CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; /CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	184	182	181	mA
I_{DD6}	**Self Refresh Current: Normal Temperature Range;** TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	12	12	12	mA
I_{DD7}	**Operating Bank Interleave Read Current;** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	226	202	179	mA

Note 1: TC = 85°C; SRT and ASR are disabled

Note 2: Enabling ASR could increase IDDx by up to an additional 2mA

Note 3: Restricted to TC MAX = 85°C.

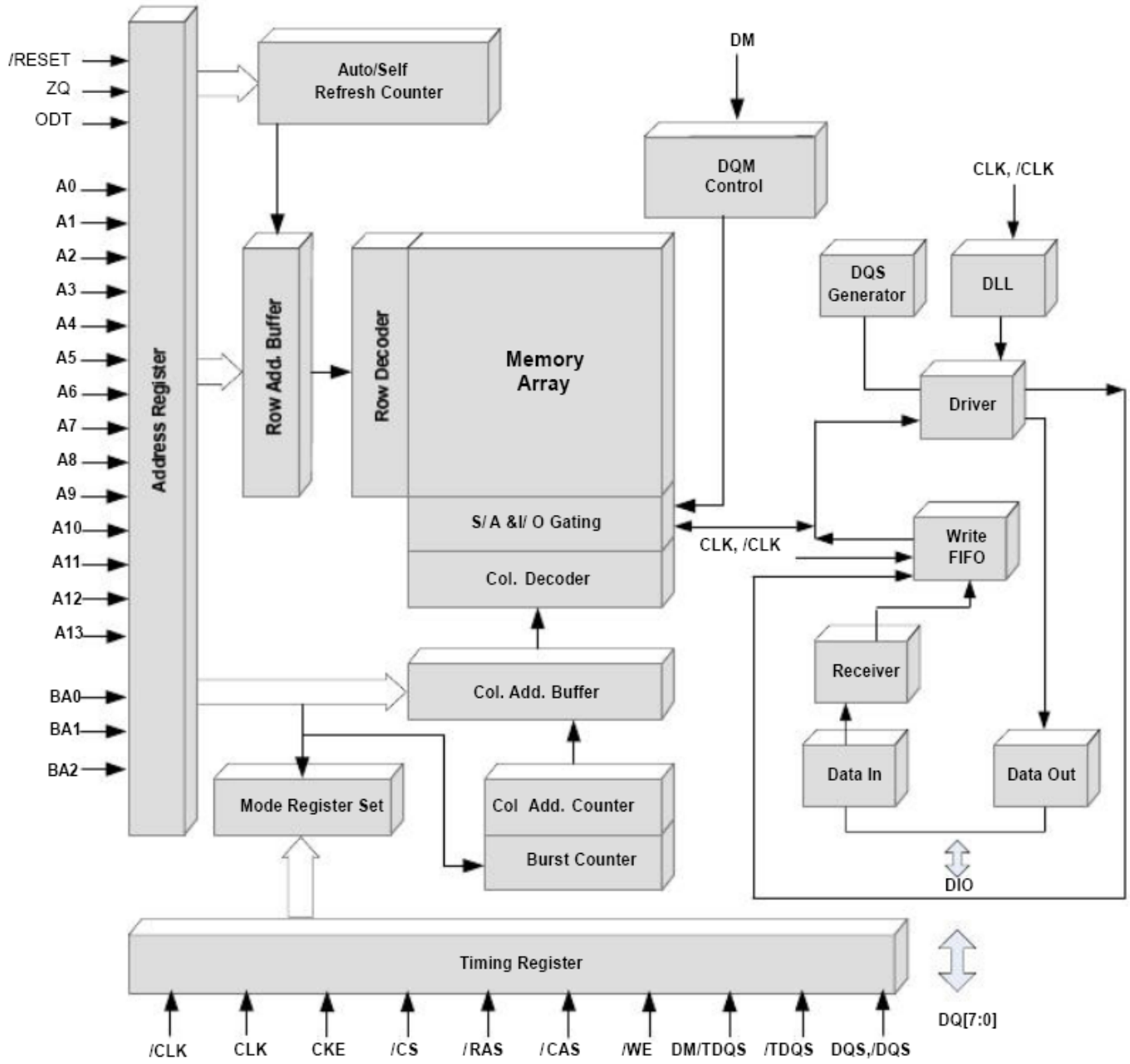
Note 4: TC = 85°C; ASR and ODT are disabled; SRT is enabled.

Note 5: The IDD values must be derated (increased) on IT-option devices when operated outside the range 0°C ≤ TC ≤ +85°C:

5a. When TC < 0°C: IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6, IDD6ET and IDD7 must be derated by 7%.

5b. When TC > 85°C: IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; and IDD2Px must be derated by 30%.

Block Diagram



AC Operating Test Characteristics

DDR3-1333 & DDR3-1600 & DDR3-1866 Speed Bins

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	1866		1600		1333		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
tAA	Internal read command to first data	13.91	20	13.75	-	13.5	-	ns	8
tRCD	Active to read or write delay	13.91	-	13.75	-	13.5	-	ns	8
tRP	Precharge command period	13.91	-	13.75	-	13.5	-	ns	8
tRC	Active to active/auto refresh command	47.91	-	48.75	-	49.5	-	ns	8
tRAS	Active to precharge command period	34	9*t_{REFI}	35	9*t_{REFI}	36	9*t_{REFI}	ns	7
tCK (AVG)	Average Clock Cycle, CL=6, CWL=5	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3, 5.6
tCK (AVG)	Average Clock Cycle, CL=7, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1,2,3, 4,5,6
tCK (AVG)	Average Clock Cycle, CL=8, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1,2,3, 5,6
tCK (AVG)	Average Clock Cycle, CL=9, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3 ,4,6
tCK (AVG)	Average Clock Cycle, CL=10, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3 ,6
tCK (AVG)	Average Clock Cycle, CL=11, CWL=8	1.25	<1.5	1.25	<1.5	-	-	ns	1,2,3
tCK (AVG)	Average Clock Cycle, CL=13, CWL=9	1.07	<1.25	-	-	-	-	ns	1,2,3, 4,8
-	Support CL Settings	5~11,13		5,6,7,8,9,10,11		5,6,7,8,9,10		nCK	
-	Support CWL Settings	5,6,7,8,9		5,6,7,8		5,6,7		nCK	

Notes1: The CL setting and CWL setting result in tCK (avg) (min.) and tCK (avg) (max.) requirements. When making a selection of tCK (avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

Notes2: tCK (avg) (min.) limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (avg) value (2.5, 1.875, 1.5, 1.25 or 1.07ns) when calculating CL (nCK) = tAA (ns) / tCK (avg)(ns), rounding up to the next 'Supported CL'.

Notes3: tCK (avg) (max.) limits: Calculate tCK (avg) + tAA (max.)/CL selected and round the resulting tCK (avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns or 1.07ns). This result is tCK (avg) (max.) corresponding to CL selected.

Notes4: 'Reserved' settings are not allowed. User must program a different value.

Notes5: Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.

Notes6: Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the

table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.

Notes7: tREFI depends on operating case temperature (TC).

Notes8: For devices supporting optional down binning to CL = 7 and CL = 9, tAA/tRCD/tRP(min.) must be 13.125 ns or lower. SPD settings must be programmed to match.

Command Truth Table

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]	Notes
			Prev. Cycle	Next Cycle										
MODE REGISTER SET		MRS	H	H	L	L	L	L	BA	OP code				
REFRESH		REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	L	L	H	V	V	V	V	V	6
Self refresh exit		SRX	L	H	H	V	V	V	V	V	V	V	V	6, 7
					L	H	H	H						
Single-bank PRECHARGE		PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	L	H	L	V		V	H	V	
Bank ACTIVATE		ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	8
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA	8
READ	BL8MRS, BC4MRS	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	8
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA	8
NO OPERATION		NOP	H	H	L	H	H	H	V	V	V	V	V	9
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	10
Power-down entry		PDE	H	L	L	H	H	H	V	V	V	V	V	6
					H	V	V	V						
Power-down exit		PDX	L	H	L	H	H	H	V	V	V	V	V	6, 11
					H	V	V	V						
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Note1: Commands are defined by the states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-, density-, and configurationdependent.

Note2: RESET# is enabled LOW and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.

Note3: The state of ODT does not affect the states described in this table.

Note4: Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.

Note5: "V" means "H" or "L" (a defined logic level), and "X" means "Don't Care."

Note6: See Table 71 (page 118) for additional information on CKE transition.

Note7: Self refresh exit is asynchronous.

Note8: Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.

Note9: The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.

Note10: The DES and NOP commands perform similarly..

Note11: The power-down mode does not perform any REFRESH operations.

Note12:ZQ CALIBRATION LONG is used for either ZQinit (first ZQCL command during initialization) or ZQoper (ZQCL command after initialization).

CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18
For more details with all signals, see “Command Truth Table”					10

Note1: CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

Note2: Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.

Note3: Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.

Note4: All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note5: The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

Note6: During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

Note7: DESELECT and NOP are defined in the “Command Truth Table”.

Note8: On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

Note9: Self-Refresh mode can only be entered from the All Banks Idle state.

Note10: Must be a legal command as defined in the “Command Truth Table”.

Note11: Valid commands for power-down entry and exit are NOP and DESELECT only.

Note12: Valid commands for self-refresh exit are NOP and DESELECT only.

Note13: Self-Refresh can not be entered during Read or Write operations.

Note14: The Power-Down does not perform any refresh operations.

Note15: "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

Note16: VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh. operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operati on or first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note17: If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

Note18: 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). /RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2. OR
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

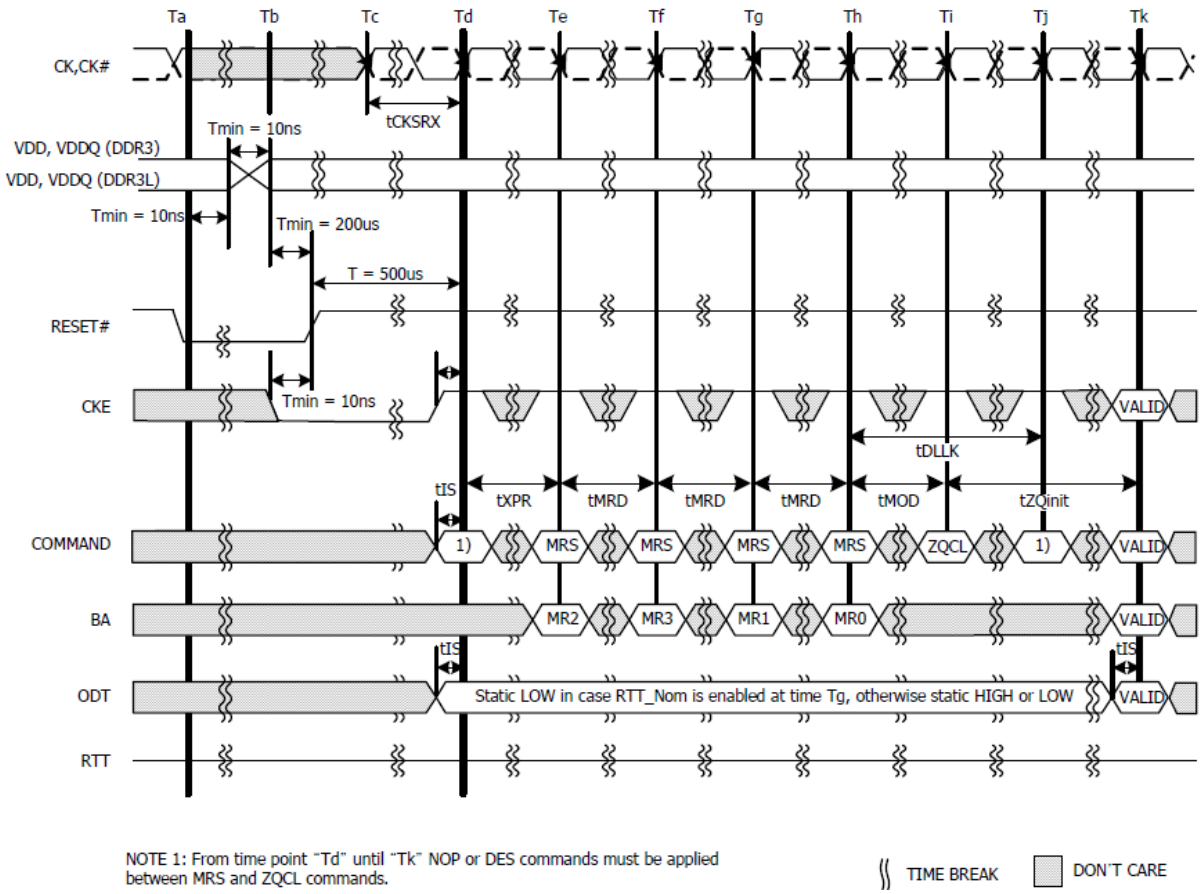
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. *(tXPR=max (tXS ; 5 x tCK)*

6. Issue MRS Command to load ***MR2*** with all application settings. (To issue MRS command for ***MR2***, provide

"Low" to BA0 and BA2, "High" to BA1.)

7. Issue MRS Command to load ***MR3*** with all application settings. (To issue MRS command for ***MR3***, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load ***MR1*** with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load ***MR0*** with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

Reset and Power up initialization sequence



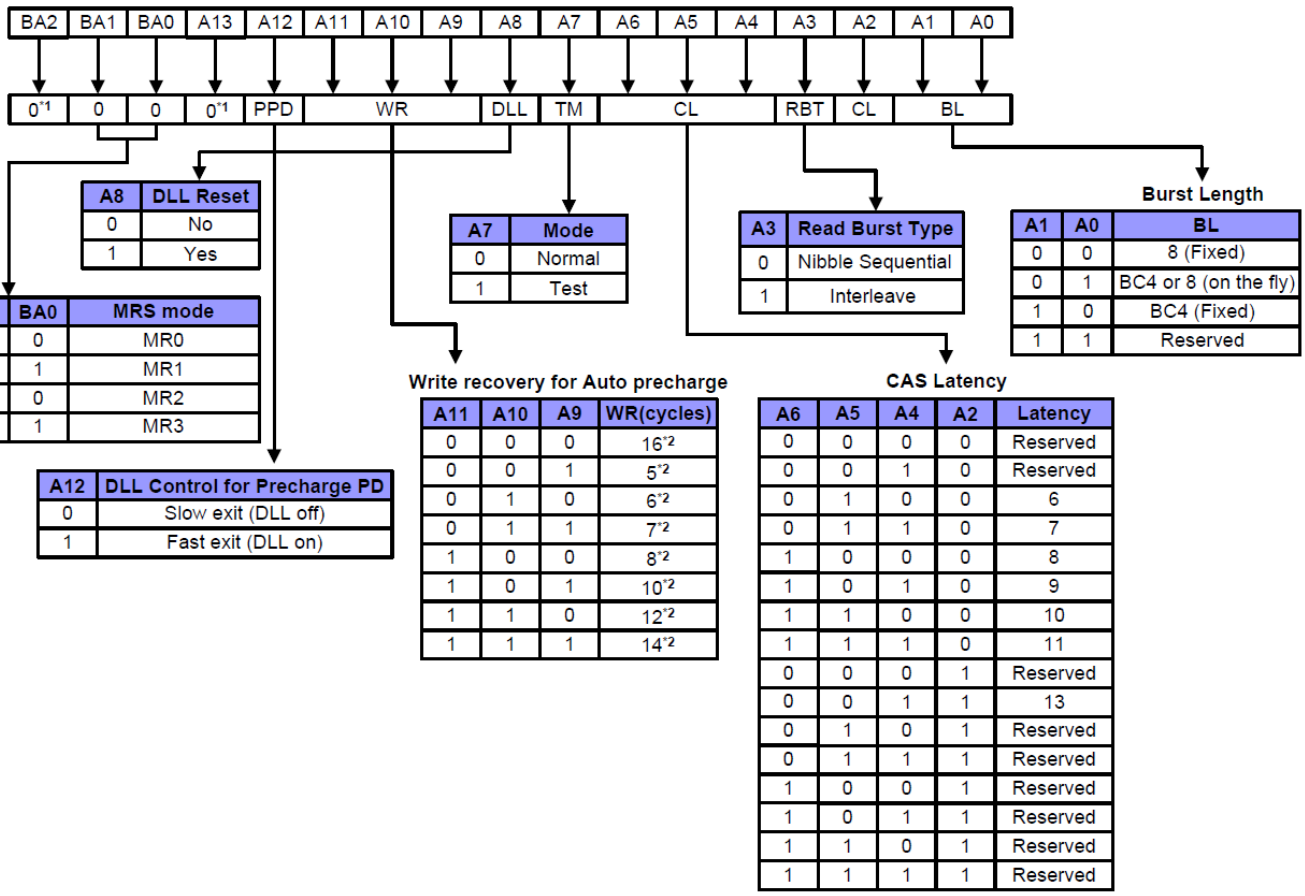
NOTE 1: From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Mode Register Definition

Mode Register MR0

The Mode Register ***MR0*** stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below



A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

Burst Length

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Write recovery for Auto precharge

A11	A10	A9	WR(cycles)
0	0	0	16*2
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

CAS Latency

A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	Reserved
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	Reserved
0	0	1	1	13
0	1	0	1	Reserved
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

Note1: BA2 and A13 are reserved for future use and must be programmed to 0 during MRS.

Note2: WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[ns]/t_{CK}[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.

Burst Type (A3)

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

Note1: In case of burst length being fixed to 4 by ***MR0*** setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12 (/BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Note2: 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

Note3: T: Output driver for data and strobes are in high impedance.

Note4: V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

Note5: X: Don't Care.

CAS Latency

The CAS Latency is defined by ***MR0*** (bits A9-A11). CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by ***MR0*** (bit A7 = 0) and rest bits set to the desired values. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM factory and should NOT be used. No operations or functionality is specified if A7 = 1.

DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

Write Recovery

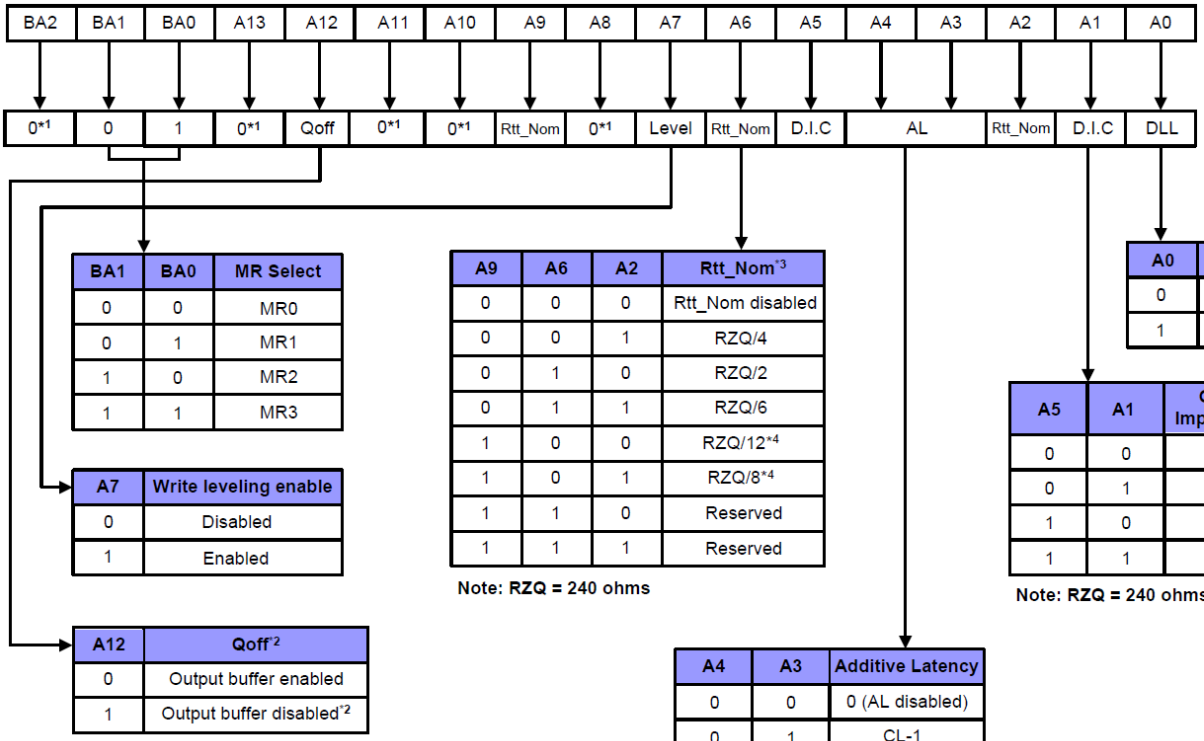
The programmed WR value ***MR0*** (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/ tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When ***MR0*** (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When ***MR0*** (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register ***MR1*** stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A7	Write leveling enable
0	Disabled
1	Enabled

A12	Qoff*2
0	Output buffer enabled
1	Output buffer disabled*2

A9	A6	A2	Rtt_Nom*3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240 ohms

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Note: RZQ = 240 ohms

Note1: BA2, A8, A10 and A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Note2: Qoff: Outputs disabled - DQs, DQSs, /DQSs.

Note3: In Write leveling Mode (***MR1***[bit7] = 1) with ***MR1***[bit12] = 1, all RTT_Nom settings are allowed; in Write Leveling Mode (***MR1***[bit7] = 1) with ***MR1***[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

Note4: New RON value is defined as RON48=RZQ/5.

DLL Enable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with ***MR1*** (A0 = 0), the DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refers to “DLL-off Mode”.
The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits ***MR1***{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode. The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, ***MR2*** {A10, A9} = {0,0}, to disable Dynamic ODT externally.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, It allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings.

Write Leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

Output Disable

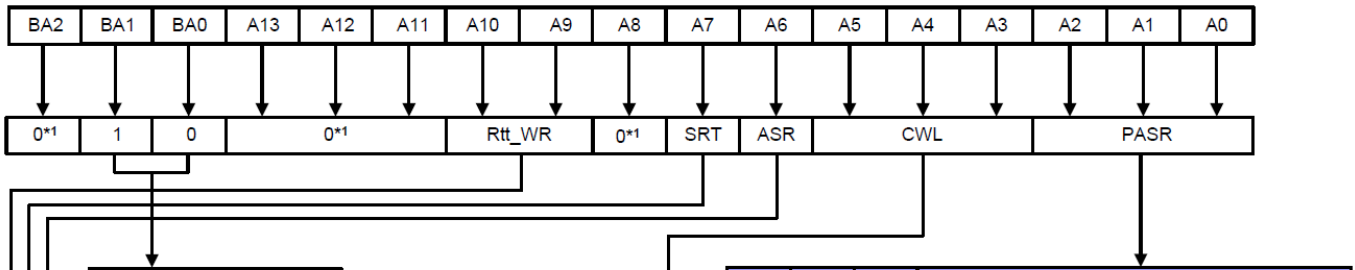
The outputs may be enabled/disabled by MR1 (bit A12). When this feature is enabled (A12 = 1), all output pins (DQs, DQS, /DQS, etc.) are disconnected from the device, thus removing any loading of the output drivers. For normal operation, A12 should be set to '0'.

TQS, /TDQS

TDQS (Termination Data Strobe) provides additional termination resistance outputs that may be useful in some system configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS & /TDQS pins that is applied to the DQS & /DQS pins. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS. The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the /TDQS pin is not used.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, including RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A6	Auto Self Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable

A7	Self Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended operating temperature range

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A2	A1	A0	Partial Array Self Refresh for 8 Banks
0	0	0	Full array
0	0	1	Half Array (BA[2:0]=000,001,010 & 011)
0	1	0	Quarter Array (BA[2:0]=000 & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100,101,110 & 111)
1	0	1	Half Array (BA[2:0]=100,101,110 & 111)
1	1	0	Quarter Array (BA[2:0]=110 & 111)
1	1	1	1/8th Array (BA[2:0]=111)

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 ($t_{CK(avg)} \geq 2.5nS$)
0	0	1	6 ($2.5nS > t_{CK(avg)} \geq 1.875nS$)
0	1	0	7 ($1.875nS > t_{CK(avg)} \geq 1.5nS$)
0	1	1	8 ($1.5nS > t_{CK(avg)} \geq 1.25nS$)
1	0	0	9 ($1.25nS > t_{CK(avg)} \geq 1.07nS$)

Note1: BA2, A8, A11 ~ A13 are RFU and must be programmed to 0 during MRS.
Note2: The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

CAS Write Latency (CWL)

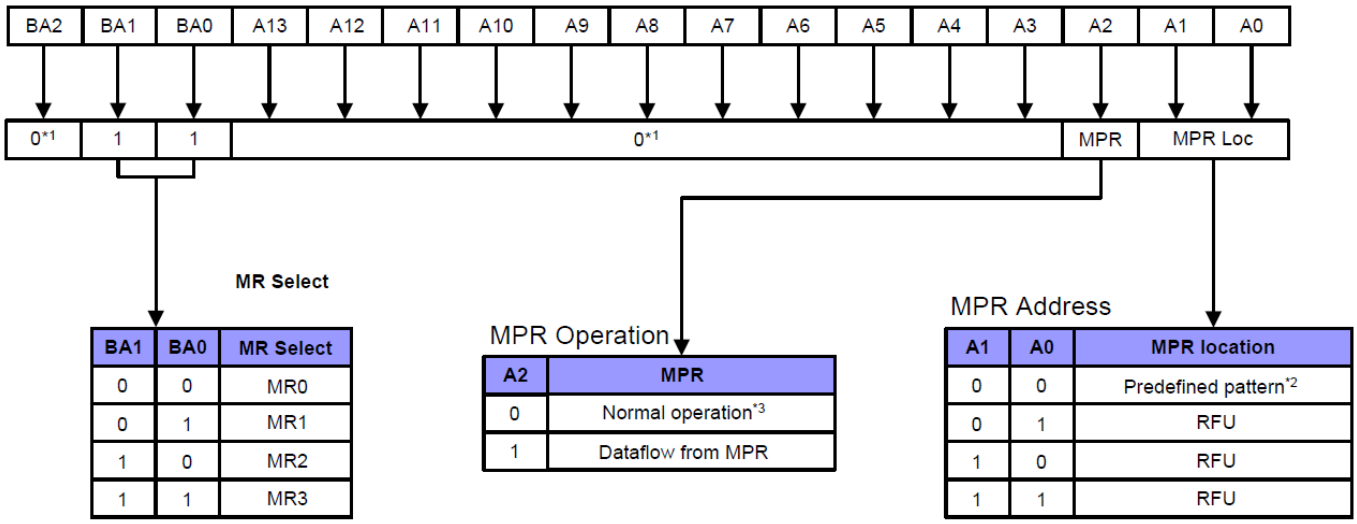
The CAS Write Latency is defined by ***MR2*** (bits A3-A5). CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. ***MR2*** Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available.

Mode Register MR3

The Mode Register ***MR3*** controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

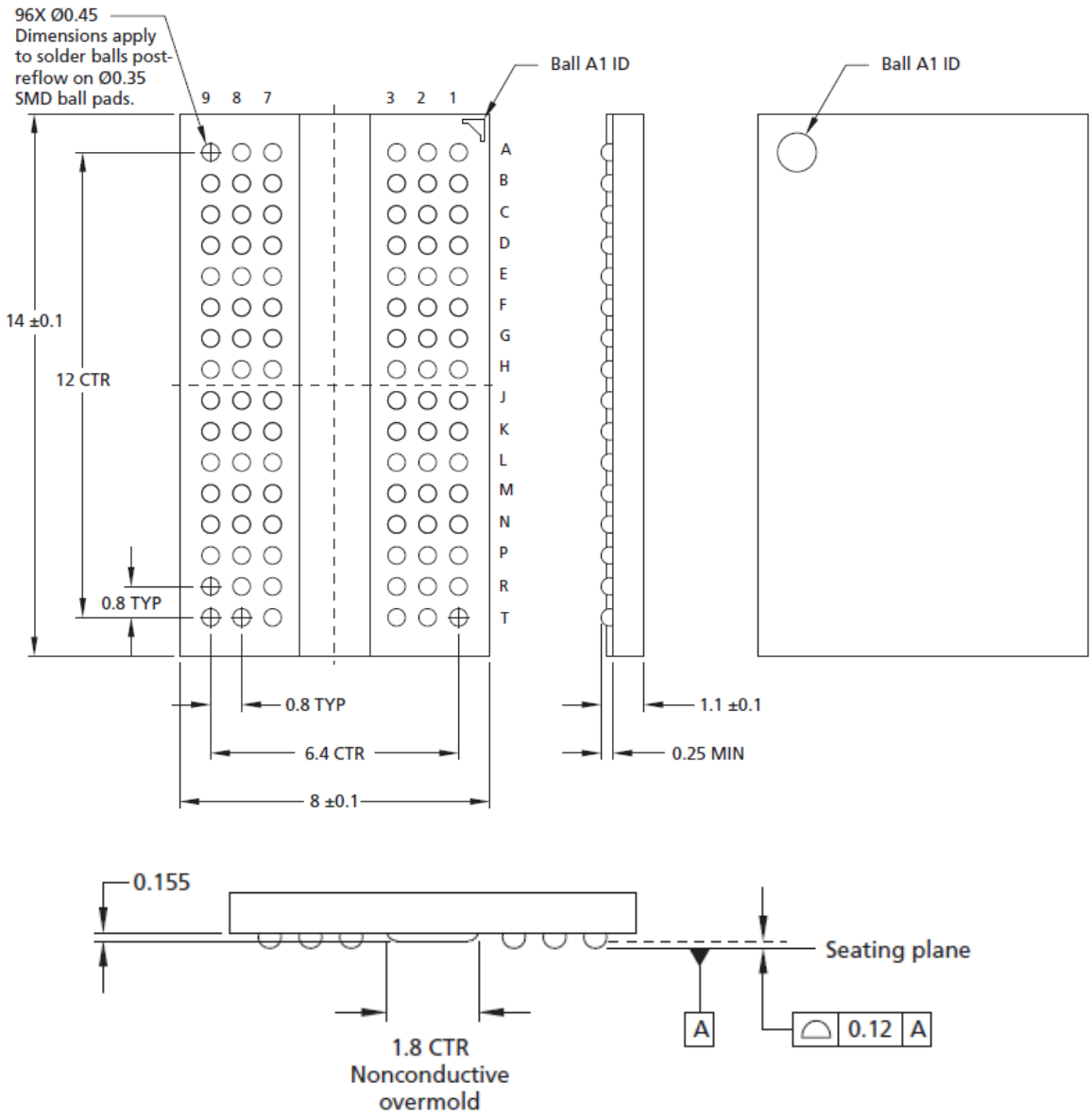
Note1: BA2, A3 - A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.
Note2: The predefined pattern will be used for read synchronization.
Note3: When MPR control is set for normal operation, ***MR3*** A[2] = 0, ***MR3*** A[1:0] will be ignored

Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to ***MR3*** Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (***MR3*** bit A2 = 0). Power-down mode, self-refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Package Description: 96Ball-FBGA 8x14mm pitch: 0.8mm, ø= 0.45mm

Solder ball: Lead free (Sn-Ag-Cu)



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Jul. 2017	Maven Hsu	N/A
1.0	First SPEC. release.	Jul. 2017	Maven Hsu	N/A