

1G-Bit 1.8V NAND FLASH MEMORY

Descriptions

The H7A11G64B9CN (1G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 1.7V to 1.95V power supply with active current consumption as low as 25mA and 10uA for CMOS standby current.

The memory array totals 138,412,032 bytes, and organized into 1,024 erasable blocks of 135,168 bytes. Each block consists of 64 programmable pages of 2,112-bytes each. Each page consists of 2,048-bytes for the main data storage area and 64-bytes for the spare data area (The spare area is typically used for error management functions). The H7A11G64B9CN supports the standard NAND flash memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions.

The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

Features

• Basic Features

- Density : 1Gbit (Single chip solution)
- Vcc : 1.7V to 1.95V
- Bus width : x8
- Operating temperature
Commercial: 0°C to 70°C

• Single-Level Cell (SLC) technology.

• Organization

- Density: 1G-bit/128M-byte
- Page size
2,112 bytes (2048 + 64 bytes)
- Block size
64 pages (128K + 4K bytes)

• Highest Performance

- Read performance (Max.)
 - Random read: 25us
 - Sequential read cycle: 35ns
- Write Erase performance
 - Page program time: 300us(typ.)
 - Block erase time: 2ms(typ.)
- Endurance 100,000 Erase/Program Cycles
- 10-years data retention

• Command set

- Standard NAND command set
- Additional command support
 - Sequential / Random Cache Read
 - Cache Program
 - Copy Back
- OTP feature
- Block Lock feature

• Lowest power consumption

- Read: 10mA(typ.3V)
- Program/Erase: 10mA(typ.)
- CMOS standby: 10uA(typ.)

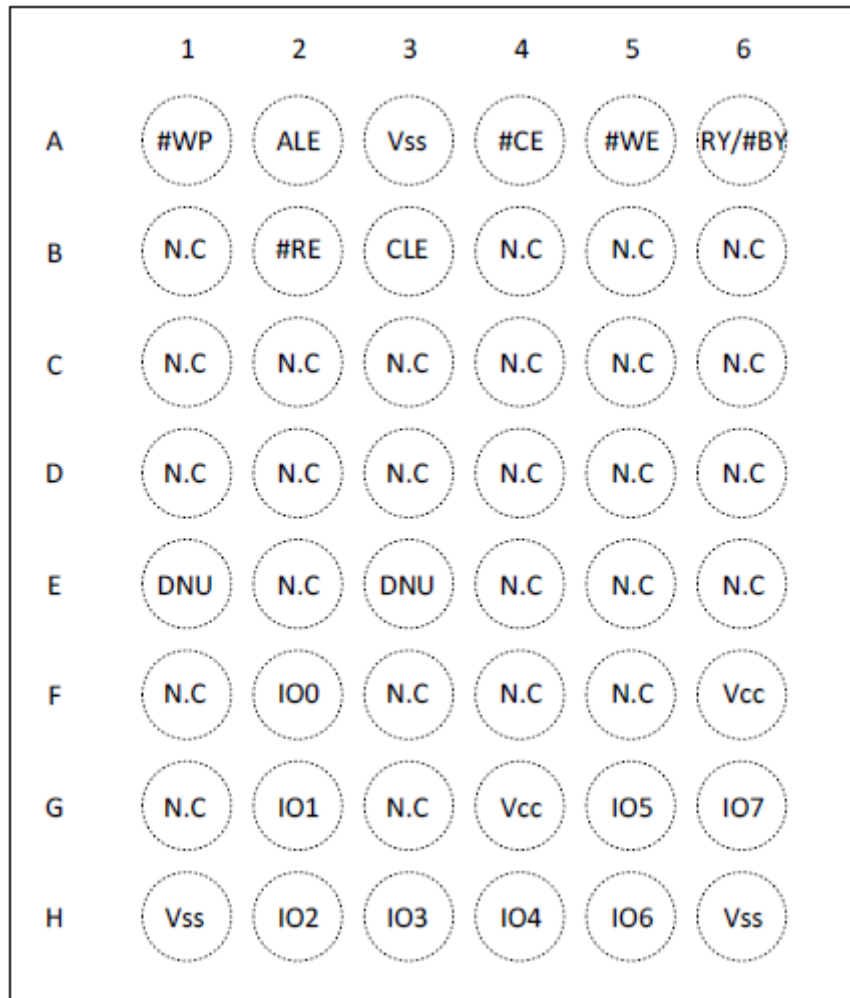
• Space Efficient Packaging

- 48-ball VFBGA

Ordering Information

Part No	Density	Organization	Package	Grade
H7A11G64B9CN	1G-bit/128M-byte	X8	48-ball VFBGA 6.5x8mm	Commercial

Pin Assignment



48-ball VFBGA TOP VIEW

Pin Description (Simplified)

48-ball VFBGA,6.5x8mm		
Pin Name	I/O	Function
#WP	Input	Write Protect
ALE	Input	Address Latch Enable
#CE	Input	Chip Enable
#WE	Input	Write Enable
RY#BY	Output	Ready/Busy
#RE	Input	Read Enable
CLE	Input	Command Latch Enable
I/O[0-7]	Input / Output	Data Input / Output (x8)
V _{cc}	Supply	Power Supply
V _{ss}	Supply	Ground
DNU	-	Do Not Use:
N.C	-	Not Connect

Note1: Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.

Absolute Maximum Rating(1.8V)

Item	Symbol	Conditions	Rating	Unit
Supply Voltage	V _{cc}		-0.6 ~ 2.4	V
Voltage Applied to Any Pin	V _{in}	Relative to Ground	-0.6 ~ 2.4	V
Storage Temperature	T _{STG}		-65 ~ 150	°C
Short circuit output current	I _{os}		5	mA

Note 1: Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.

Note 2: Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

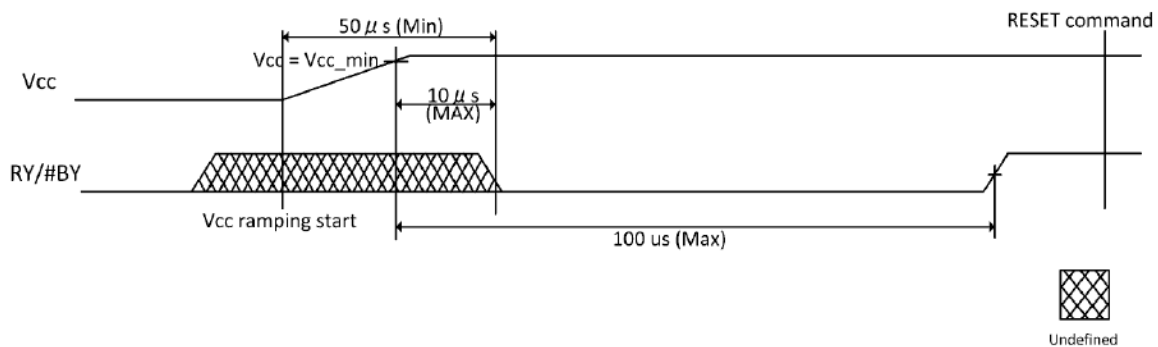
Note 3: This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

Operating Ranges(3.3V)

Parameter	Symbol	Conditions	Spec.		Unit
			Min.	Max.	
Supply Voltage	Vcc		1.7	1.95	V
Ambient Temperature, Operating	Ta	Commercial	0	70	°C

Device Power-up Timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, the system has to wait until the ready state. #WP is recommended to VIL for preventing unexpected Program and Erase operations during power-transition until Vcc is stable. The RY/#BY will become valid after 50µs from the Vcc ramp start, and at least 10µs after Vcc reaches minimum Vcc level. The first command has to be a RESET command after the device is powered on. Before issuing RESET command, the system has to wait until the RY/#BY goes HIGH, or wait at least 100µs after Vcc reaches minimum Vcc. After issuing the RESET command, the busy time is 1ms maximum. RY/#BY polling or READ STATUS command can monitor the reset busy period. After completing this procedure, the device is initialized and ready for the operation (See Below Figure).



Power ON/OFF sequence

DC Characteristics(1.8V)

Parameters	Symbol	Conditions	Spec.			Unit
			MIN	TYP	Max	
Sequential Read current	Icc1	tRC= tRC MIN #CE=VIL IOUT=0mA	-	10	25	mA
Program current	Icc2	-	-	10	25	mA
Erase current	Icc3	-	-	10	25	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc - 0.2V #WP=0V/Vcc	-	10	50	uA
Input leakage current	ILI	VIN= 0 V to Vcc	-	-	+/-10	uA
Output leakage current	ILO	VOUT=0V to Vcc	-	-	+/-10	uA
Input high voltage	VIH	I/O7~0, #CE,#WE,#RE, #WP,CLE,ALE,	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	VOH	IOH=-100µA	Vcc-0.1	-	-	V
Output low voltage(1)	VOL	IOL=100uA	-	-	0.1	V
Output low current	IOL(RY/#BY)	VOL=0.2V	3	4	-	mA

Note 1: VOH and VOL may need to be relaxed if I/O drive strength is not set to full.

Note 2: IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full.

AC Measurement Conditions(1.8V)

Parameter	Symbol	Spec.		Unit
		MIN	Max	
Input Capacitance(1), (2)	CIN	-	10	pF
Input/Output Capacitance(1), (2)	CIO	-	10	pF
Input Rise and Fall Times	TR/TF	-	5	ns
Input Pulse Voltages	-	0 to VCC		V
Input/Output timing Voltage	-	Vcc/2		V
Output load (1)	CL	1TTL GATE and CL=30pF		-

Note 1: Verified on device characterization , not 100% tested

Note 2: Test conditions TA=25°C, f=1MHz, VIN=0V

AC timing characteristics for Command, Address and Data Input(1.8V)

Parameter	Symbol	Spec.		Unit
		MIN	MAX	
ALE to Data Loading Time	tADL	100	-	ns
ALE Hold Time	tALH	10	-	ns
ALE setup Time	tALS	15	-	ns
#CE Hold Time	tCH	10	-	ns
CLE Hold Time	tCLH	5	-	ns
CLE setup Time	tCLS	15	-	ns
#CE setup Time	tCS	25	-	ns
Data Hold Time	tDH	5	-	ns
Data setup Time	tDS	15	-	ns
Write Cycle Time	tWC	35	-	ns
#WE High Hold Time	tWH	15	-	ns
#WE Pulse Width	tWP	17	-	ns
#WP setup Time	tWW	100	-	ns

Note: 1. tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.

AC timing characteristics for Operation(1.8V)

Parameter	Symbol	Spec.		Unit
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	30	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	45	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Cache Busy in Cache Read mode	tRCBSY	3	tR	us
Output High-Z to #RE LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	us
READ Cycle Time	tRC	35	-	ns
#RE Access Time	tREA	-	25	ns
#RE HIGH Hold Time	tREH	15	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	100	ns
#RE LOW to output hold	tRLOH	5	-	ns
#RE Pulse Width	tRP	17	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	us
#WE HIGH to Busy(1)	tWB	-	100	ns
#WE HIGH to #RE LOW	WHR	80	-	ns

Note 1: Transition is measured $\pm 200\text{mV}$ from steady-state voltage with load. This parameter is sampled and not 100 % tested and do not issue new command during tWB, even if RY/#BY is ready.

Note 2: The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5 μs .

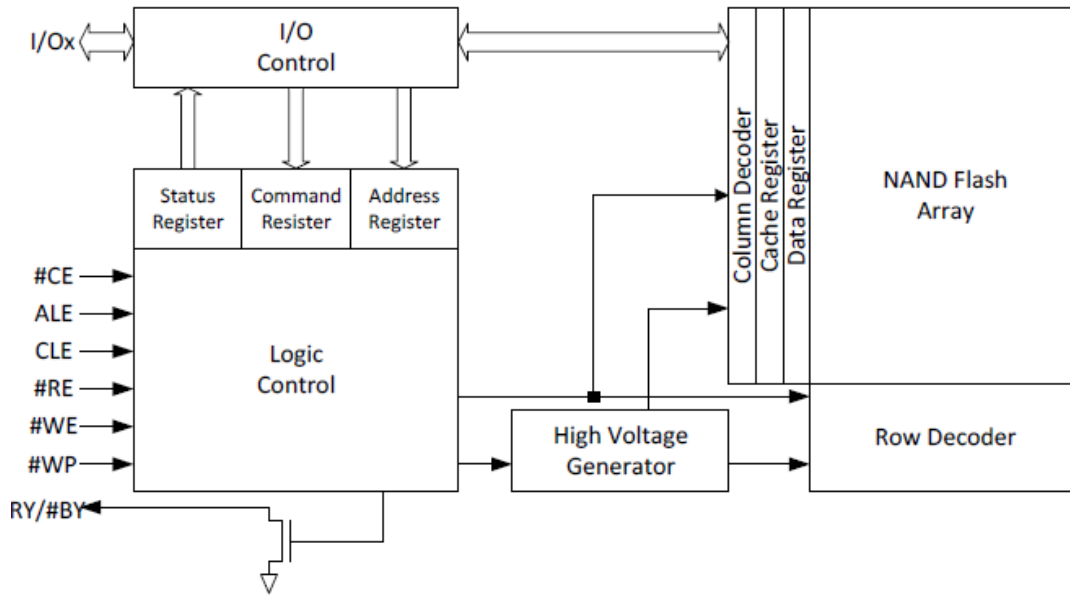
Program and Erase Characteristics

Parameter	Symbol	Spec.		Unit
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	300	700	us
Busy Time for Cache program (1)	tCBSY	3	700	us
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	us
Busy Time for program/erase at locked block	tLBSY	-	3	us
Busy Time for OTP program when OTP is protected	tOBSY	-	30	us
Block Erase Time	tBERS	2	10	ms
Last Page Program time (2)	tLPROG	-	-	-

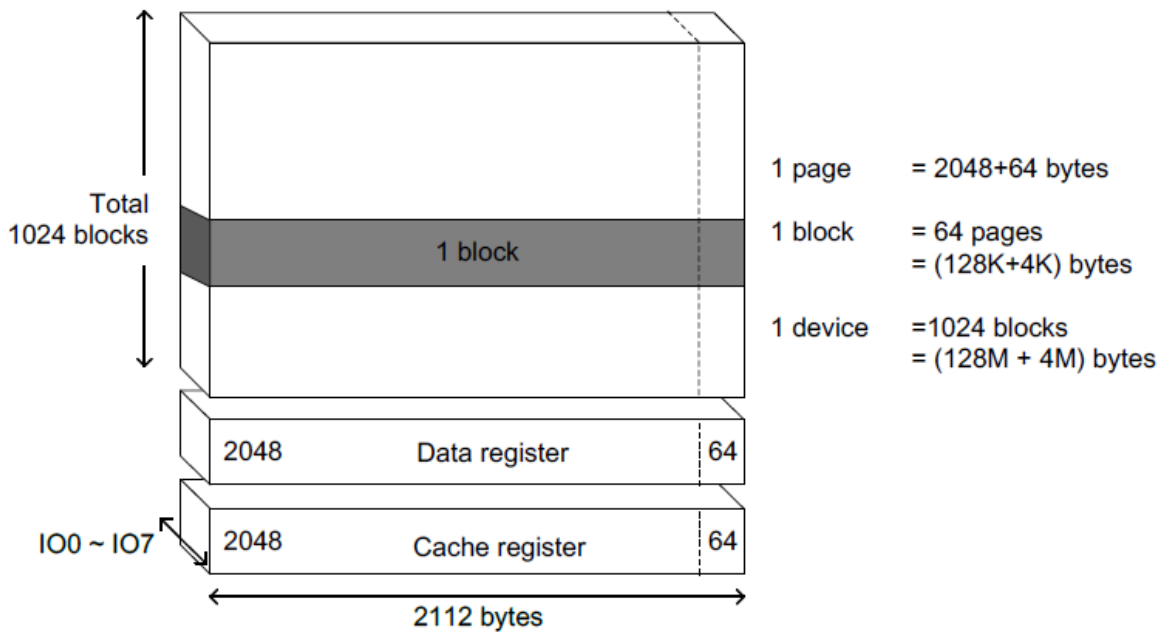
Note: 1. tCBSY maximum time depends on timing between internal program complete and data-in.

Note: 2. tLPROG = Last tPROG + Last -1 tPROG – Last page Address, Command and Data load time.

Block Diagram



Memory Array Organization









	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1 st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2 nd cycle	L	L	L	L	A11	A10	A9	A8
3 rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4 th cycle	A27	A26	A25	A24	A23	A22	A21	A20

Note: 1. "L" indicates a low condition, which must be held during the address cycle to insure correct processing.

Note: 2. A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A27 during the 3rd to 4th cycles are row addresses.

Note: 3. The device ignores any additional address inputs that exceed the device's requirement.

Mode Selection Table

Mode		CLE	ALE	#CE	#WE	#RE	#WP
Read Mode	Command input	H	L	L		H	X
	Address input	L	H	L		H	X
Write Mode	Command input	H	L	L		H	H
	Address input	L	H	L		H	H
Data input		L	L	L		H	H
Sequential Read and Data output		L	L	L	H		X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/ Vcc

Note 1: “H” indicates a HIGH input level, “L” indicates a LOW input level, and “X” indicates a Don’t Care Level.

Note 2: #WP should be biased to CMOS HIGH or LOW for standby.

Command Table

Command	1 st Cycle	2 nd Cycle	3 rd Cycle	4 th Cycle	Acceptable during busy
PAGE READ	00h	30h			
READ for COPY BACK	00h	35h			
SEQUENTIAL CACHE READ	31h				
RANDOM CACHE READ	00h	31h			
LAST ADDRESS CACHE READ	3Fh				
READ ID	90h				
READ STATUS	70h				Yes
RESET	FFh				Yes
PAGE PROGRAM	80h	10h			
PROGRAM for COPY BACK	85h	10h			
CACHE PROGRAM	80h	15h			
BLOCK ERASE	60h	D0h			
RANDOM DATA INPUT(1)	85h				
RANDOM DATA OUTPUT(1)	05h	E0h			
READ PARAMETER PAGE	ECh				
READ UNIQUE ID	EDh				
GET FEATURES	EEh				
SET FEATURES	EFh				
OTP DATA PROTECT	A5h	10h			
OTP DATA PROGRAM	A0h	10h			
OTP DATA READ	AFh	30h			

Note 1: RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.

Note 2: Any commands that are not in the above table are considered as undefined and are prohibited as inputs.

Invalid Block Management

The H7A11G64B9CN may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks(see below table). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

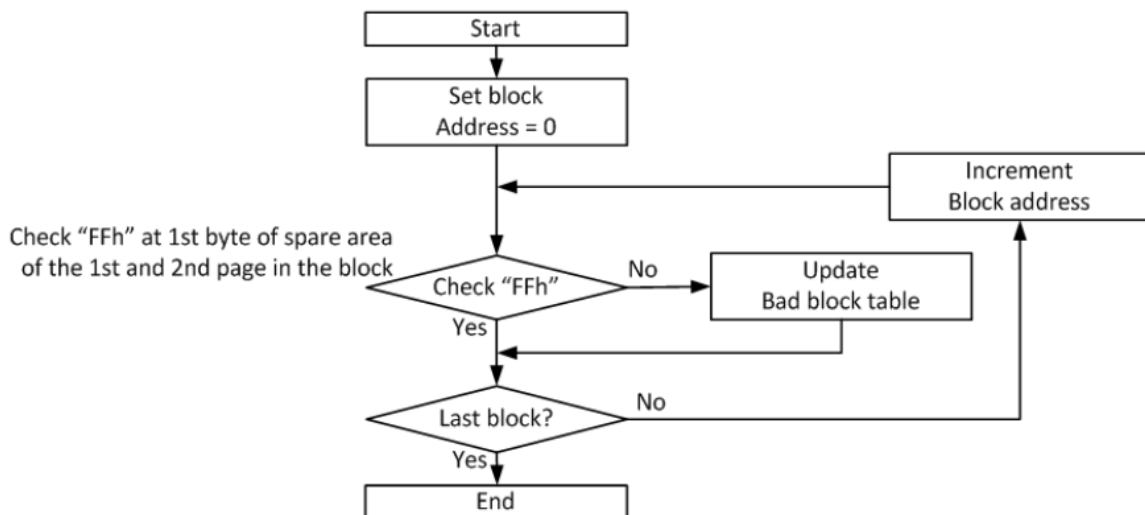
Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	1004	1024	blocks

Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The H7A11G64B9CN has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart.



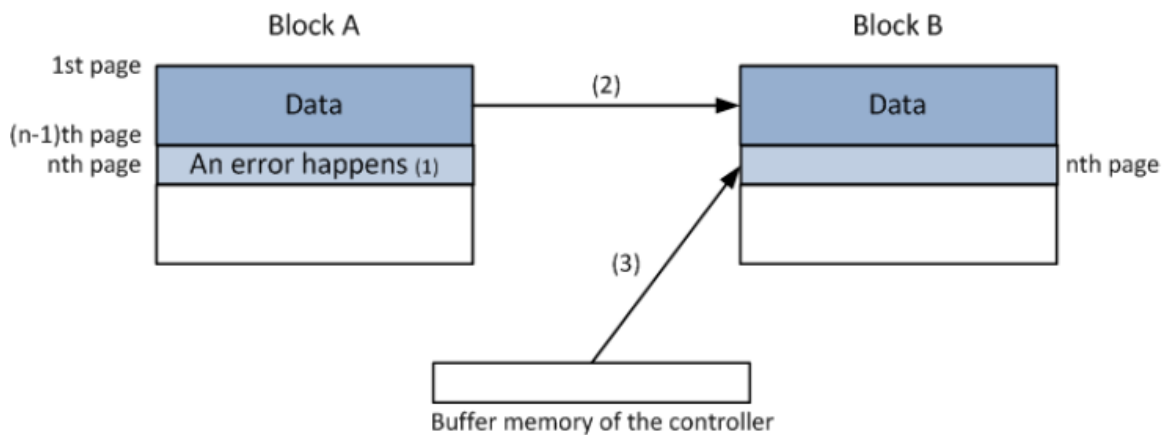
flow chart of create initial invalid block table

Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction



Bad block Replacement

Note 1: An error happens in the nth page of block A during program or erase operation.

Note 2: Copy the data in block A to the same location of block B which is valid block.

Note 3: Copy the nth page data of block A in the buffer memory to the nth page of block B

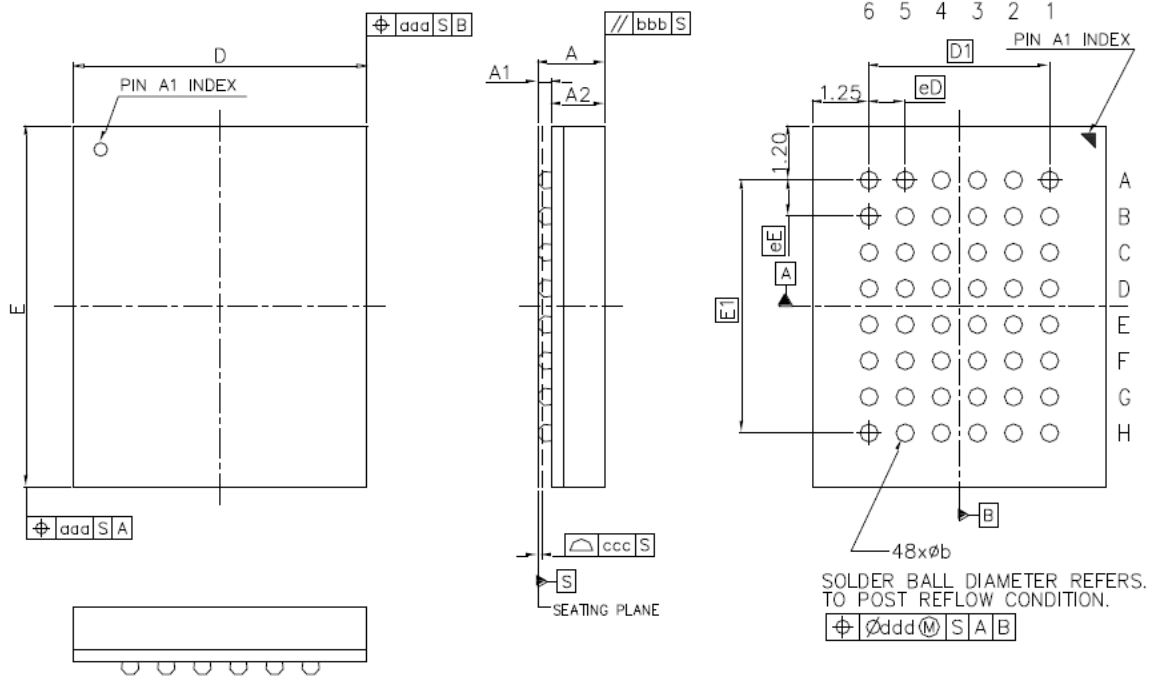
Note 4: Creating or updating bad block table for preventing further program or erase to block A

Addressing in program operation

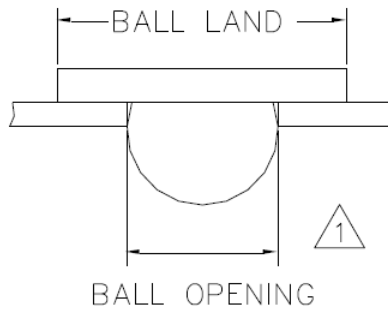
The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

Package Description

VFBGA 48-ball 6.5x8mm



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.25	0.30	0.35
A2	0.55	0.60	0.65
b	0.35	0.40	0.45
D	6.40	6.50	6.60
E	7.90	8.00	8.10
D1	4.00 BSC		
E1	5.60 BSC		
eD	0.80 BSC		
eE	0.80 BSC		
aaa	0.14		
bbb	--	--	0.1
ccc	--	--	0.10
ddd	--	--	0.15



Note:

1. Ball land:0.45mm. Ball opening:0.35mm.
PCB ball land suggested ≤ 0.35 mm

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Sep. 2017	Maven Hsu	N/A
1.0	First SPEC. Release.	Sep. 2017	Maven Hsu	N/A