1Gb (8Mx8Banksx16) DDR2 SDRAM

Descriptions

The H2A301G1656B is a high speed Double Date Rate 2 (DDR2) Synchronous DRAM fabricated with ultra high performance CMOS process containing 1,073,741,824 bits which organized as 8Mbits x 8 banks by 16 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 800Mb/sec/pin (DDR2-1066) for general applications. The chip is designed to comply with the following key DDR2 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) Off-Chip Driver (OCD) impedance adjustment and On Die Termination (4) normal and weak strength data output driver. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style. The 1Gb DDR2 device operates with a single power supply: 1.8V ± 0.1V VDD and VDDQ. Available package: TFBGA-84Ball (with 0.8mm x 0.8mm ball pitch)

Features

- JEDEC Standard VDD/VDDQ = 1.8V±0.1V.
- All inputs and outputs are compatible with SSTL_18 interface.
- Fully differential clock inputs (CK, /CK) operation.
- Eight Banks
- Posted CAS
- Bust length: 4 and 8.
- Programmable CAS Latency (CL): 5,6 and 7
- Programmable Additive Latency (AL): 0, 1, 2, 3, 4, 5 & 6.
- Write Latency (WL) =Read Latency (RL) -1.
- Read Latency (RL) = Programmable Additive Latency (AL) + CAS Latency (CL)
- Bi-directional Differential Data Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available.
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination (ODT)
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- Average Refresh Period 7.8us at lower than Tcase 85 °C, 3.9us at 85°C < Tcase ≦ 95°C
- RoHS Compliance
- Partial Array Self-Refresh (PASR)
- High Temperature Self-Refresh rate enable

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A301G1656BA6C	64M X 16	DDR2-667MHz 5-5-5	84Ball BGA, 8x12.5mm	Commercial
H2A301G1656BB6C	64M X 16	DDR2-800MHz 6-6-6	84Ball BGA, 8x12.5mm	Commercial
H2A301G1656BC6C	64M X 16	DDR2-1066MHz 7-7-7	84Ball BGA, 8x12.5mm	Commercial

Note: Speed (tck*) is in order of CL-T_{RCD}-T_{RP}

Ball Assignments and Descriptions

84-Ball FBGA – x16 (Top View)

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	/UDQS	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	/LDQS	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	/WE	K	/RAS	/CK	ODT
BA2	BA0	BA1	L	/CAS	/CS	
	A10/AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

Note: VDDL and VSSDL are power and ground for the DLL.

78-Ball FBGA - x8 Ball Descriptions

Pin	Symbol	Description
J8,K7	CK, /CK	**(System Clock)** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK . Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
L8	/CS	**(Chip Select)** All commands are masked when /CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
K2	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self- Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE are disabled during Self-Refresh.
M8,M3,M7,N2, N8,N3,N7,P2, P8,P3,M2,P7, R2	A0~A12	**(Address)** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
L2,L3,L1	BA0, BA1,BA2	**(Bank Address)** BA0 – BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
K9	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.

K7, L7, K3	/RAS, /CAS, /WE	**(Command Inputs)** /RAS, /CAS and /WE (along with /CS) define the command being entered.
B7,A8,F7,E8	UDQS,/UDQS LDQS,/LDQS	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobes LDQS and UDQS may be used in single ended mode or paired with optional complementary signals /LDQS and /UDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to A10 = 0 of EMRS(1) using LDQS/LDQS and UDQS/UDQS. "single-ended DQS signals" refers to A10 = 1 of EMRS(1) using LDQS and UDQS.
B3,F3	UDM,LDM	**(Input Data Mask)** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
G8,G2,H7,H3, H1,H9,F1,F9, C8,C2,D7,D3, D1, D9,B1,B9	DQ0~15	**(Data Input/Output)** Data inputs and outputs are on the same pin.
A1,E1,J9,M9, R1/ A3,E3,J3, N1,P9	VDD/VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
A9,C1,C3,C7, C9,E9,G1,G3, G7,G9/A7,B2, B8,D2,D8,E7, F2,F8,H2,H8	VDDQ/VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
J1/J7	VDDL/VSSDL	**(DLL Power Supply/DLL Ground)** VDDL and VSSDL are power supply for DLL circuits
J2	VREF	**(Reference Voltage)** SSTL_1.8 reference voltage
A2,E2,R3, R7, R8	NC	**(No Connection)** No internal electrical connection is present.

Note: Input balls only BA0~BA2, A0~A15, /RAS, /CAS, /WE, /CS, CKE, ODT and /RESET do not supply termination.

Absolute Maximum Ratings

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ +2.3		V
V_{DD}	Power Supply Voltage	-1.0 ~ +2.3		V
V_{DDQ}	Power Supply Voltage	-0.5 ~ +2.3		V
V_{DDL}	DLL Power Supply Voltage	-0.5 ~ +2.3		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +70	°C
T_{STG}	Storage Temperature Range	-55 ~ +100		°C
P_D	Power Dissipation	1		W

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Input/ Output Capacitance (V_{CC}=1.8V± 0.1V, f=1MHz, T_A=25°C)

Symbol	Parameters	Min.	Typ	Max.	Unit
C_{CK}	Input Capacitance of CK,/CK	1.0	-	2.0	pF
CD_{CK}	Input Capacitance delta of CK, /CK	-	-	0.25	pF
C_I	Input Capacitance for others: CKE, Address, /CS, /RAS, /CAS, /WE	1.0	-	1.75	pF
CD_I	Input Capacitance delta for others	-	-	0.25	pF
C_{IO}	Input/Output Capacitance DQ, DM, DQS, DQS, RDQS, RDQS	2.5	-	3.5	pF
CD_{IO}	Input/Output Capacitance delta	-	-	0.5	pF

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	Power Supply Voltage	1.7	1.8	1.9	V
VDDL	Power Supply for DLL Voltage	1.7	1.8	1.9	V
VDDQ	Power Supply for I/O Voltage	1.7	1.8	1.9	V
VREF	I/O Reference Voltage	0.49 VDDQ	0.50VDDQ	0.51 VDDQ	V
VTT	I/O Termination Voltage	VREF-0.04	VREF	VREF+0.04	V

Recommended DC Operating Conditions

(V_{DD}=1.8V±0.2V, T_A=0°C ~ 70°C)

Symbol	Parameter & Test Conditions		1066MHz	800MHz	667MHz	Units
			Max			
I_{DD0}	**Operation Current – One Bank Active-Precharge** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD) CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING; Databus input are SWITCHING.		75	70	65	mA
I_{DD1}	**Operating Current - One Bank Active-Read-Precharge** IOUT = 0 mA;BL = 4, CL = CL(IDD), AL = 0;tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD (IDD);CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING;Data bus inputs are SWITCHING.		90	85	80	mA
I_{DD2P}	**Precharge Power-Down Current** All banks idle;tCK = tCK(IDD); CKE is LOW;Other control and address inputs are STABLE; Data Bus inputs are FLOATING. (TCASE ≤ 85°C)		8	8	8	mA
I_{DD2N}	**Precharge Standby Current** All banks idle;tCK = tCK(IDD);CKE is HIGH, /CS is HIGH;Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		45	40	35	mA
I_{DD2Q}	**Precharge Quiet Standby Current** All banks idle;tCK = tCK(IDD);CKE is HIGH, /CS is HIGH; Other control and address inputs are STABLE; Data bus inputs are FLOATING.		40	35	30	mA
I_{DD3PF}	**Active Power Down Current** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address inputs are STABLE; Data bus inputs are FLOATING. (TCASE≤85°C)	Fast PDN Exit MRS(12) = 0	25	25	25	mA
I_{DD3PS}		Slow PDN Exit MRS(12) = 1	25	25	25	mA
I_{DD3N}	**Active Standby Current in Non-power Down Mode** All banks open tCK = tCK(IDD), tRAS = tRASmax(IDD) tRP = tRP(IDD), CKE is HIGH CS is HIGH between valid commands Other control and address bus inputs are SWITCHING Data bus inputs are SWITCHING		55	50	45	mA

I_{DD4R}	**Operating Burst Read Current** All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD),tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	145	120	105	mA
I_{DD4W}		155	130	110	mA
I_{DD5B}	**Burst Refresh Current** tCK = tCK(IDD);Refresh command every tRFC(IDD) interval;CKE is HIGH, /CS is HIGH between valid commands;Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING	145	130	120	mA
I_{DD6}	**Self Refresh Current** CKE ≤ 0.2 V, external clock off, CLK and /CLK at 0 V;Other control and address inputs are FLOATING; Data bus inputs are FLOATING. (TCASE ≤ 85°C)	8	8	8	mA
I_{DD7}	**Operating Bank Interleave Read Current** All bank interleaving reads, IOU T = 0mA;BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD);tCK = tCK(IDD),tRC = tRC(IDD), tRRD =tRRD(IDD), tFAW= tFAW(IDD), tRCD = tRCD(IDD);CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are STABLE during deselects;Data Bus inputs are SWITCHING.	190	185	160	mA

Note 1: I_{DD1} depends on output loading and cycle rates. (CL=CLmin, AL=0)

Note 2: I_{DD4} depends on output loading and cycle rates. Input signals SWITCHING

Note 3: Min. of t_{RFC} (Auto refresh Row Cycle Times) is shown at AC Characteristics.

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH}	High Level Output Voltage	*Note5	VTT+0.603		V
V_{OL}	Low Level Output Voltage	*Note5		VTT-0.603	V
I_{LI}	Input Leakage Current	-	-	2	µA
I_{LO}	Output Leakage Current	-	-	5	µA
I_{OH}	Output Minimum Source Current	*Note2, 4, 5	-13.4		mA
I_{OL}	Output Minimum Sink Current	*Note3, 4, 5		+13.4	mA

Note1: The VDDQ of the device under test is referenced

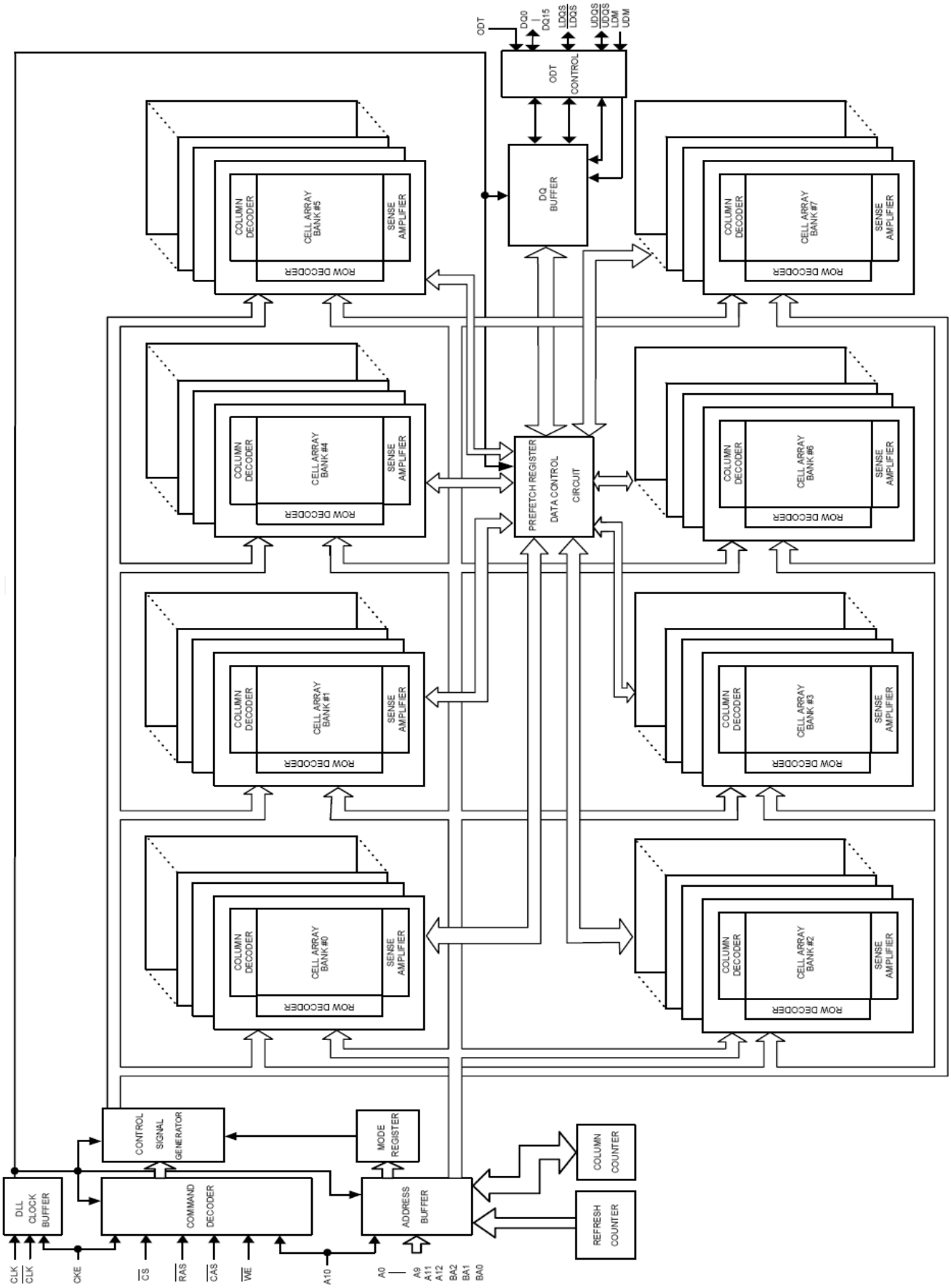
Note2: VDDQ=1.7V, VOUT=1.42V

Note3: VDDQ=1.7V, VOUT=0.28V

Note4: The DC value of VREF applied to the receiving device is expected to be set to VTT

Note5: After OCD calibration to 18Ω at TC=25℃, VDD=VDDQ=1.8V

Block Diagram



OCD Default Setting Table

Parameter	Min.	Typ.	Max.	Units
Output Impedance	12.6	18	23.4	Ω
Pull-up / Pull-down mismatch	0	-	4	Ω
Output Slew Rate	1.5	-	5.0	V/ns

AC Operating Test Conditions

(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

Parameter	Min.	Typ.	Max.
VSWING (max.)	Input Signal Maximum Peak to Peak Swing	1.0	V
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns
VREF	Input Reference Level	0.5*VDDQ	V

AC Operating Test Conditions

Parameter	Min.	Typ.	Max.	Units
V_{ID}	AC Differential Input Voltage	0.5	VDDQ+0.6	V
V_{IX}	AC Differential Cross Point Input Voltage	0.5*VDDQ-0.175	0.5*VDDQ+0.175	V
V_{OX}	AC Differential Cross Point Output Voltage	0.5*VDDQ-0.125	0.5*VDDQ+0.125	V
V_{IH}	Input Logic High Voltage (DDR2-533)	VREF+0.25	VDDQ+Vpeak	V
V_{IH}	Input Logic High Voltage (DDR2-667/800)	VREF+0.25	VDDQ+Vpeak	V
V_{IL}	Input Logic High Voltage (DDR2-533)	VSSQ-Vpeak	VREF-0.25	V
V_{IL}	Input Logic High Voltage (DDR2-667/800)	VSSQ-Vpeak	VREF-0.25	V

AC Operating Test Characteristics

(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

Symbol	Parameter	(DDR2-1066)		(DDR2-800)		(DDR2-667)		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	DQ output access from CLK,/CLK	-0.35	0.35	-0.40	0.40	-0.45	0.45	ns
t_{DQSCK}	DQS output access from CLK,/CLK	-0.32	0.32	-0.35	0.35	-0.40	0.40	ns
t_{CL},t_{CH}	CL low/high level width	0.48	0.52	0.48	0.52	0.48	0.52	tCK
t_{CK}	Clock Cycle Time CL=5, Speed= -25/-3	1.875	7.5	2.5	7.5	3	7.5	ns
t_{DS}	DQ and DM setup time	0.02		0.05	-	0.10	-	ns
t_{DH}	DQ and DM hold time	0.02		0.125	-	0.175	-	ns
t_{DIPW}	DQ and DM input pulse width for each input	0.35		0.35	-	0.35	-	ns
t_{HZ}	Data out high impedance time from CLK,/CLK	-	tAC (max)	-	tAC (max)	-	tAC (max)	ns
t_{LZ} (DQ)	DQ low impedance time from CLK,/CLK	2*tAC (min)	tAC (max)	2*tAC (min)	tAC (max)	2*tAC (min)	tAC (max)	ns
t_{LZ} (DQS)	DQS,/DQS low impedance time from CLK,/CLK	tAC (min)	tAC (max)	tAC (min)	tAC (max)	tAC (min)	tAC (max)	ns
t_{DQSQ}	DQS-DQ skew for associated DQ signal	-	0.175	-	0.20	-	0.24	ns
t_{QHS}	Data hold skew factor	-0.25	-	-	0.30	-	0.34	ns
t_{DQSS}	Write command to first latching DQS transition	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK
t_{DQSL},t_{DQSH}	DQS Low/High input pulse width	0.35	-	0.35	-	0.35	-	tCK
t_{DSL},t_{DSH}	DQS input valid window	0.20	-	0.20	-	0.20	-	tCK
t_{MRD}	Mode Register Set command cycle time	2	-	2	-	2	-	tCK
t_{WPRES}	Write Preamble setup time	0	-	0	-	0	-	ns
t_{WPRE}	Write Preamble	0.35	-	0.35	-	0.35	-	tCK
t_{WPST}	Write Postamble	0.4	0.6	0.4	0.6	0.4	0.6	tCK
t_{IS}	Address/control input setup time (fast slew rate)	0125		0.175	-	0.20	-	ns
t_{IH}	Address/control input hold time (fast slew rate)	0.2		0.25	-	0.275	-	ns
t_{RPRE}	Read Preamble	0.9	1.1	0.9	1.1	0.9	1.1	tCK

AC Operating Test Characteristics

(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

Symbol	Parameter	(DDR2-1066)		(DDR2-800)		(DDR2-667)		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RPST}	Read Postamble	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{RAS}	Active to Precharge command period	45	70k	45	70k	45	70k	ns
t_{RC}	Active to Active command period	57.5	-	57.5	-	60	-	ns
t_{RFC}	Auto Refresh Row Cycle Time	127.5	-	127.5	-	127.5	-	ns
t_{RCD}	Active to Read or Write delay	11.25		12.5	-	15	-	ns
t_{RP}	Precharge command period	11.25		12.5	-	15	-	ns
t_{RRD}	Active bank A to B command period	10		10	-	10	-	ns
t_{CCD}	Column address to column address delay	2		2	-	2	-	t_{CK}
t_{WR}	Write recover time	15		15	-	15	-	ns
t_{DAL}	Auto precharge write recovery + precharge time	$t_{RP}+t_{WR}$		$t_{RP}+t_{WR}$	-	$t_{RP}+t_{WR}$	-	ns
t_{XARD}	Exit active power-down mode to read command (fast exit)	2		2	-	2	-	t_{CK}
t_{XARDS}	Exit active power-down mode to read command (slow exit)	10-AL		8-AL	-	7-AL	-	t_{CK}
t_{XP}	Exit precharge power-down to any non-read command	2	-	2	-	2	-	t_{CK}
t_{WTR}	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns
t_{RTP}	Internal read to precharge delay	7.5	-	7.5	-	7.5	-	ns
t_{XSNR}	Exit self Refresh to non-read command	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	ns
t_{XSRD}	Exit self Refresh to read command	200	-	200	-	200	-	t_{CK}
t_{REFI}	Average periodic refresh interval	-	7.8	-	7.8	-	7.8	us
t_{CKE}	CKE minimum pulse width	3	-	3	-	3	-	t_{CK}
t_{FAW}	Four active to Row active delay (same bank)	45		45		50		ns
t_{OIT}	OCD drive mode output delay	0	12	0	12	0	12	ns

AC Operating Test Characteristics

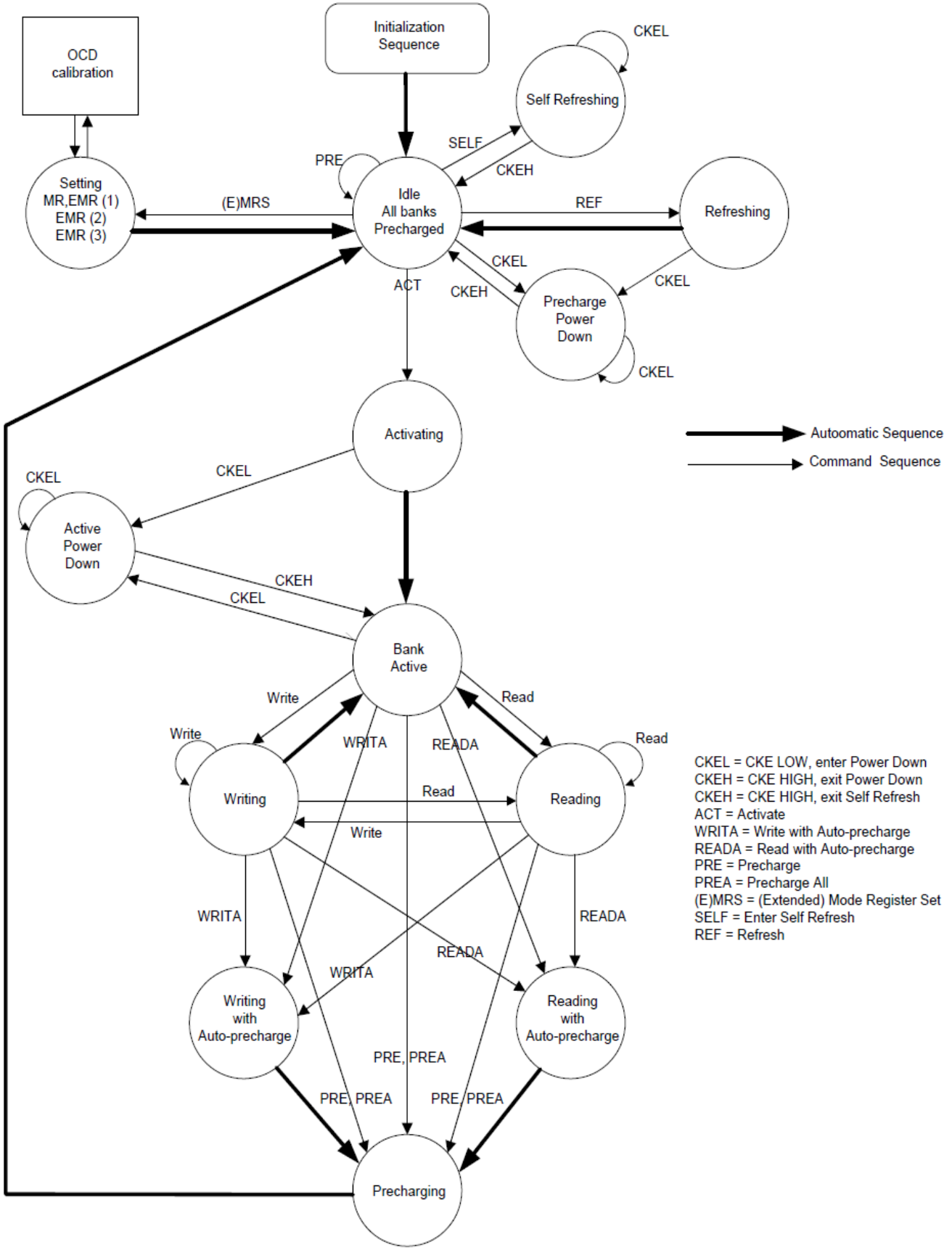
(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

Symbol	Parameter	(DDR2-1066)		(DDR2-667/ 800)		Units
		Min.	Max.	Min.	Max.	
t_{AOND}	ODT turn-on delay	2	2	2	2	t_{CK}
t_{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	t_{CK}
t_{AON}	ODT turn-on ***(Note1)***	tAC(min.)	tAC(max) +2.575	tAC(min.)	tAC(max) +0.7	ns
t_{AOF}	ODT turn-off***(Note2)***	tAC(min.)	tAC(max) +0.6	tAC(min.)	tAC(max) +0.6	ns
t_{AONPD}	ODT turn-on in power-down mode	tAC(min.) +2	$3*t_{CK}+t_{AC}$(max) +1	tAC(min.) +2	$2*t_{CK}+t_{AC}$(max) +1	ns
t_{AOFPD}	ODT turn-off in power-down mode	tAC(min.) +2	$2.5*t_{CK}+t_{AC}$(max)+1	tAC(min.) +2	$2.5*t_{CK}+t_{AC}$(max)+1	t_{CK}
t_{ANPD}	ODT to power-down mode entry latency	4	-	3	-	t_{CK}
t_{AXPD}	ODT power-down exit latency	11	-	8	-	t_{CK}

Note 1: ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.

Note 2: ODT turn off time min is when the device starts to turn off ODT resistance ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

Simplified State Diagram



Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0~BA2	A10	A12, A10~A0
		n-1	N							
Device Deselect	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Read	READ	H	H	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	H	L	H	L	H	V	H	V
Write	WRIT	H	H	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	H	L	H	L	L	V	H	V
Bank Activate	ACT	H	H	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	H	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	H	L	L	H	L	X	H	X
(Ext.) Mode Register Set	EMRS	H	H	L	L	L	L	V*	V	V
Auto Refresh	REF	H	H	L	L	L	H	X	X	X
Self refresh entry	SELF	H	L	L	L	L	H	X	X	X
Power Down Entry	PDEN	H	L	H	X	X	X	X	X	X
		H	L	L	H	H	H	X	X	X
Power Down Exit	PDEX	L	H	H	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

* Please refers to the MRS, EMRS(1) & EMRS(2) setting

CKE Truth Table

Current State	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Any state	***Note1***	-	H	H	V	V	V	V	V
All Bank Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit	NOP	L	H	L	H	H	H	X
		DESL	L	H	H	X	X	X	X
All Bank Idle	Active or Precharge Power Down Entry	DESL	H	L	H	X	X	X	X
		NOP	H	L	L	H	H	H	X
Power Down	Power Down Exit	DESL	L	H	H	X	X	X	X
		NOP	L	H	L	H	H	H	X
Power Down	Maintain power down	-	L	L	X	X	X	X	X
Self Refresh	Maintain self refresh	-	L	L	X	X	X	X	X

H = High level, L = Low level, X = High or Low level (Don't care)

Note1: Must be legal commands as defined in the command truth table. And any state other than list above.

Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	Bank active,Latch RA
	L	L	H	L	BA, A10	PRE/PREA	NOP***(Note 3)***
	L	L	L	H	X	REF/SELF	Auto/Self refresh***(Note 4)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	Mode register
Bank Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	L	H	BA/CA/A10	READ/READA	Begin read,Latch CA, Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write,Latch CA, Determine auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	Precharge/Precharge all
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***
Read	H	X	X	X	X	DESL	Row Active(Continue burst to end)
	L	H	H	H	X	NOP	Row Active(Continue burst to end)
	L	H	L	H	BA/CA/A10	READ/READA	Burst Interrupt
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***
Write	H	X	X	X	X	DESL	Write recovering (Continue burst to end)
	L	H	H	H	X	NOP	Write recovering (Continue burst to end)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Burst Interrupt
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code,	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***

Operative Command Table (Contined)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	Precharging (Continue burst to end)
	L	H	H	H	X	NOP	Precharging (Continue burst to end)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/A10	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***
Write with AP	H	X	X	X	X	DESL	Write recover with auto precharge (Continue burst to end)
	L	H	H	H	X	NOP	Write recover with auto precharge (Continue burst to end)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***
Pre-Charging	H	X	X	X	X	DESL	NOP(idle after tRP)
	L	H	H	H	X	NOP	NOP(idle after tRP)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after tRP) ***(Note 3)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***
Raw Activating	H	X	X	X	X	DESL	NOP(Row active after tRCD)
	L	H	H	H	X	NOP	NOP(Row active after tRCD)
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Operative Command Table (Contined)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP (enter bank active after tWR)
	L	H	H	H	X	NOP	NOP (enter bank active after tWR)
	L	H	L	H	BA/CA/A10	READ	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***
Refreshing	H	X	X	X	X	DESL	NOP(idle after t_{RFC})
	L	H	H	H	X	NOP	NOP(idle after t_{RFC})
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REF/SELF	ILLEGAL ***(Note 1)***
	L	L	L	L	Op-Code, Mode-Add	MRS/EMRS(1)(2)	ILLEGAL ***(Note 1)***

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 1: ILLEGAL to bank in specified states;

Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 2: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 3: NOP to bank precharging or in idle state.May precharge bank indicated by BA.

Note 4: ILLEGAL of any bank is not idle.

Command Truth Table forCKE

Current State	CK	CKE	/CS	/R	/C	/W	Addr.	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Self-Refresh
	L	H	L	H	H	H	X	Exist Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
Both bank precharge power down	L	L	X	X	X	X	X	NOP(Maintain self refresh)
	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Power down
	L	H	L	H	H	H	X	Exist Power down
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
All Banks Idle	L	L	X	X	X	X	X	NOP(Maintain Power down)
	H	H	X	X	X	X	X	Refer to function true table
	H	L	H	X	X	X	X	Enter power down mode***(Note 3)***
	H	L	L	H	H	H	X	Enter power down mode***(Note 3)***
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row active/Bank active
	H	L	L	L	L	H	X	Enter self-refresh***(Note 3)***
	H	L	L	L	L	L	Op-Code	Mode register access
	H	L	L	L	L	L	Op-Code	Special mode register access
Any state other than listed above	L	X	X	X	X	X	X	Refer to current state

H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1: After CKE's low to high transition to exist self refresh mode.And a time of tRC(min) has to be Elapse after CKE's low to high transition to issue a new command.

Notes 2: CKE low to high transition is asynchronous as if restarts internal clock.

Notes 3: Power down and self refresh can be entered only from the idle state of all banks.

Bank Selection Signal Table

Bank\Signal	BA0	BA1	BA2
Bank0	L	L	L
Bank1	H	L	L
Bank2	L	H	L
Bank3	H	H	L
Bank4	L	L	H
Bank5	H	L	H
Bank6	L	H	H

Note: H:VIH, L:VIL

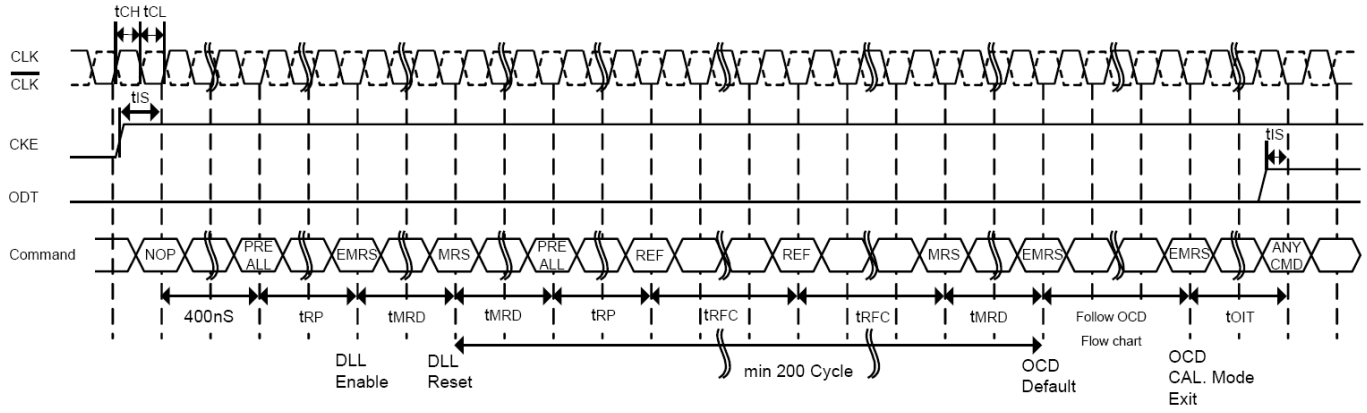
Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.
The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power and attempt to maintain CKE below 0.2 * VDDQ and ODT at a low state (all other inputs may be undefined). To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.
   A. The V_{DD} voltage ramp time must be no greater than 200 mS from when V_{DD} ramps from 300mV to V_{DD} min; and during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3$ volts.
   - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output
   - V_{TT} is limited to 0.95V max
   - V_{REF*2} tracks $V_{DDQ}/2$
   - $V_{DDQ} \geq V_{REF}$ must be met at all times

   B. Voltage levels at I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete.
   - Apply V_{DD}/V_{DDL*3} before or at the same time as V_{DDQ}
   - Apply V_{DDQ*4} before or at the same time as V_{TT}
   - V_{REF*2} tracks $V_{DDQ}/2$
   - $V_{DDQ} \geq V_{REF}$ must be met at all times.
   - Apply V_{TT}
   - The V_{TT} voltage ramp time from when V_{DDQ} min is achieved on V_{DDQ} to when V_{TT} min is achieved on V_{TT} must be no greater than 500 mS
2. Start clock (CK, /CK) and maintain stable power and clock condition for a minimum of 200 µs(min.).
3. After stable power and clock (CLK,CLK),apply NOP or Deselect commands & take CKE high.
4. Wait minimum of 400ns, then issue a Precharge-all command.
5. Issue Reserved command EMRS(2),(To issue EMRS command to EMR (2),BA0=0, BA1=1,BA2=0.)
6. Issue Reserved command EMRS(3), (To issue EMRS command to EMR (3), BA0=1, BA1=1, BA2=0.)
7. Issue EMRS(1) command to enable DLL. (A0=0,BA0=1, BA1=0,BA2=0 and A9=A8=A7=0)
8. Issue MRS Command (Mode Register Set) for "DLL reset". (A8=1 and BA0=BA1=0)
9. Issue Precharge-All command.
10. Issue 2 or more Auto-Refresh commands.
11. Issue a MRS command with low on A8 to initialize device operation. (Without resetting the DLL)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8=A7=1) followed by EMRS(1) OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other parameters of EMRS(1).
13. The DDR2 SDRAM is now initialized and ready for normal operation.

Initialization Sequence after Power Up



Mode Register Definition

Mode Register Set(MRS)

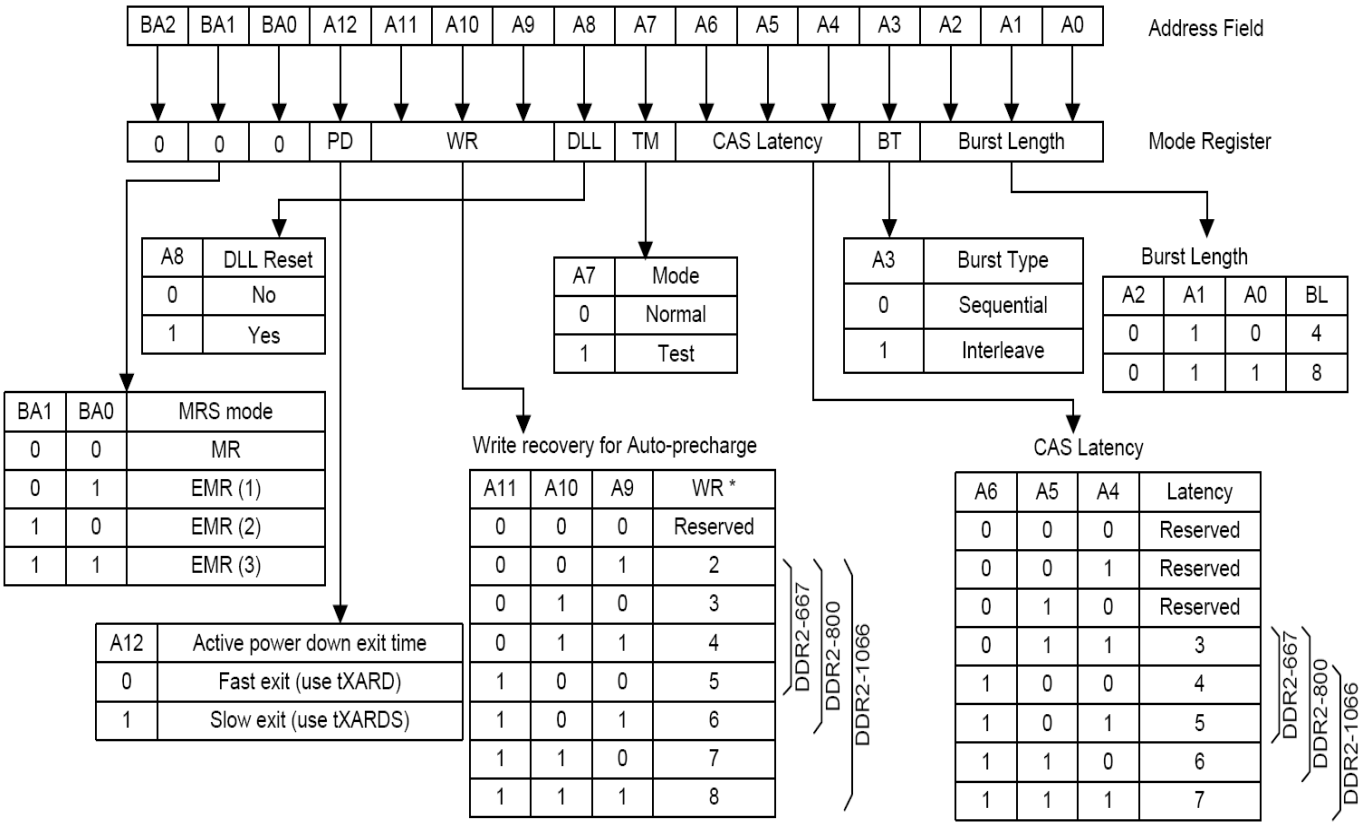
The mode register stores the data for controlling the various operating modes of DDR2 SDRAM which contains burst sequence, burst length, /CAS latency, WR (write recovery), test mode, DLL reset and various vendor's specific opinions.

The defaults value of the register is not defined, so the mode register must be written after power up for proper DDR2 SDRAM operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0/1. The state of the address pins A0-A12 in the same cycle as /CS, /RAS, /CAS, /WE and BA0/1 going low is written in the mode register.

Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operating as long as all banks are in the idle state.

The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, Burst address sequence used by A3, /CAS latency (read latency from column address) uses A4-A6. A7 is used for test mode. A8 is used for DLL reset. A9 ~ A11 are used for write recovery time (WR), A7 must be set to low for normal MRS operation. With address bit A12 two Power-Down modes can be selected, a "standard mode" and a "low-power" Power-Down mode.

Address input for Mode Register Set (MRS)



Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	X	0	0	0123TTTT	0123TTTT
	X	0	1	1230TTTT	1032TTTT
	X	1	0	2301TTTT	2301TTTT
	X	1	1	3012TTTT	3210TTTT
8	0	0	0	01234567	01234567
	0	0	1	12305674	10325476
	0	1	0	23016745	23016745
	0	1	1	30127456	32107654
	1	0	0	45670123	45670123
	1	0	1	56741230	54761032
	1	1	0	67452301	67452301
	1	1	1	74563012	76543210

*Page length is a function of I/O organization and column addressing

Write Recovery

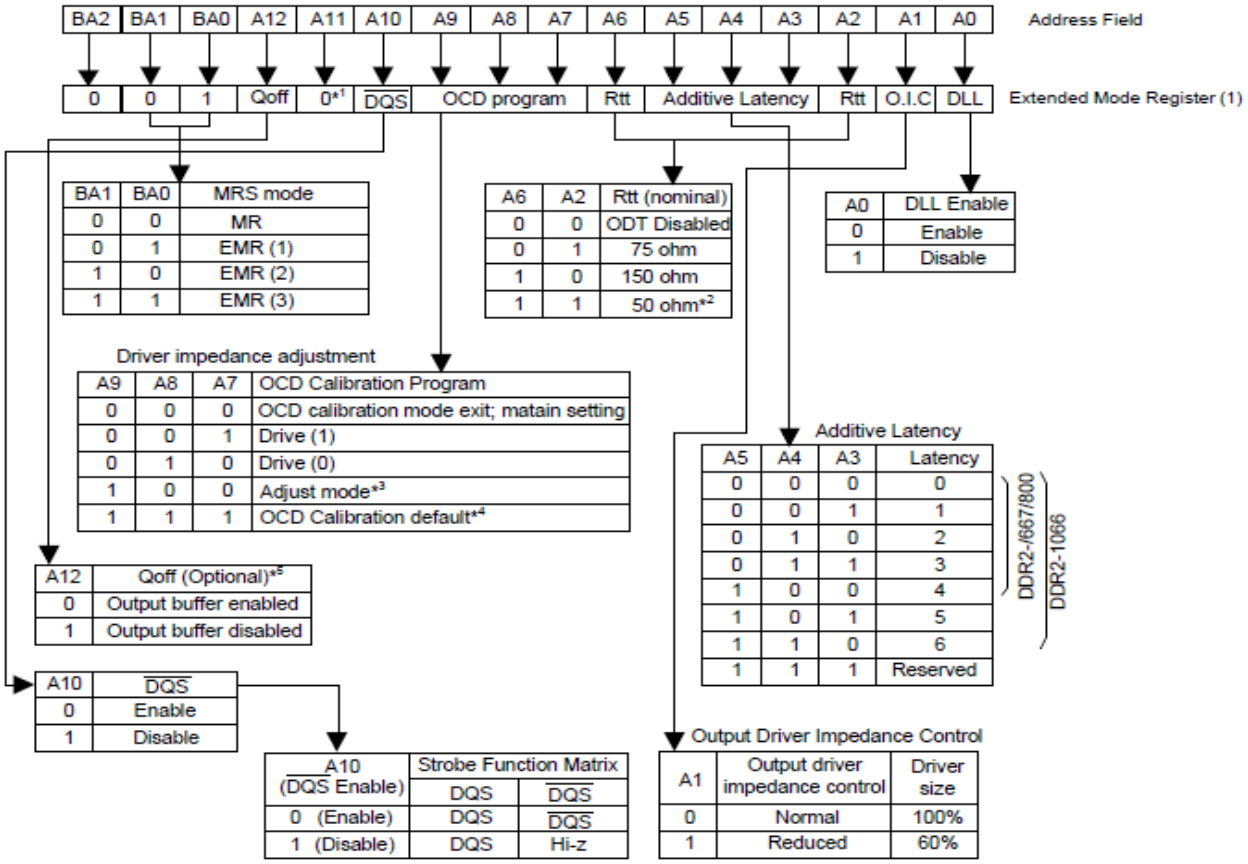
WR (Write Recovery) is for Writes with Auto-Precharge only and defines the time when the device starts pre-charge internally. WR must be programmed to match the minimum requirement for the analogue tWR timing.

Power-Down Mode

Active power-down (PD) mode is defined by bit A12. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit A12 does not apply to precharge power-down mode. When bit A12 = 0, standard Active Power-down mode or ‘fast-exit’ active power-down mode is enabled. The tXARD parameter is used for ‘fast-exit’ active power-down exit timing. The DLL is expected to be enabled and running during this mode. When bit M12 = 1, a lower power active power-down mode or ‘slow-exit’ active power-down mode is enabled. The tXARDS parameter is used for ‘slow-exit’ active power-down exit timing. The DLL can be enabled, but ‘frozen’ during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD ‘normal’ and PD ‘low-power’ mode is defined in the IDD table.

Extended Mode Register Set EMRS(1)

The EMRS (1) is written by asserting low on /CS, /RAS, /CAS, /WE,BA1,BA2 and high on BA0 (The DDR2 should be in all bank pre-charge with CKE already prior to writing into the extended mode register.) The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, OCD program, ODT, DQS and output buffers disable, RQDS and RDQS enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMRS(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation when all banks are in pre-charge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver.A3-A5 determines the additive latency,A7-A9 are used for OCD control, A10 is used for DQS disable. A2 and A6 are used for ODT setting.



Output Drive Strength

The output drive strength is defined by bit A1. Normal drive strength outputs are specified to be SSTL_18.

Programming bit A1 = 0 selects normal (100 %) drive strength for all outputs.

Programming bit A1 = 1 will reduce all outputs to approximately 60 % of the SSTL_18 drive strength.

This option is intended for the support of the lighter load and/or point-to-point environments.

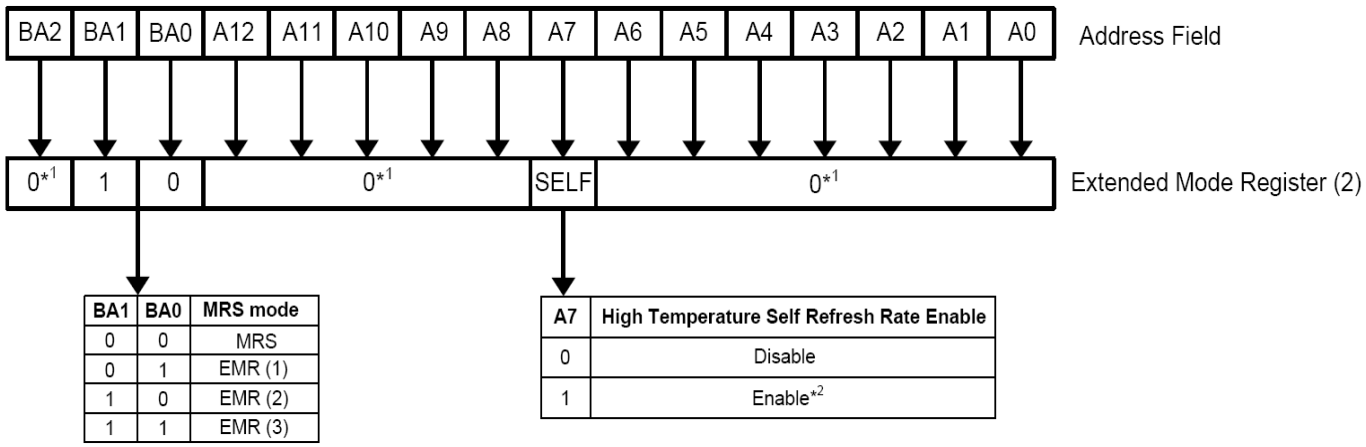
Single-ended and Differential Data Strobe Signals

EMRS		Strobe Function Matrix				Signals
A11 (/RDQS Enable)	A10 (/DQS Enable)	RDQS DM	/RDQS	DQS	/DQS	
0 (Disable)	0 (Enable)	DM	Hi-Z	DQS	/DQS	Differential DQS signal
0 (Disable)	1 (Disable)	DM	Hi-Z	DQS	Hi-Z	Single-ended DQS signal
1 (Enable)	0 (Enable)	RDQS	/RDQS	DQS	/DQS	Differential DQS signal
1 (Enable)	1 (Disable)	RDQS	Hi-Z	DQS	Hi-Z	Single-ended DQS signal

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data Qoff bit in the EMRS(1) is set to (0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current.

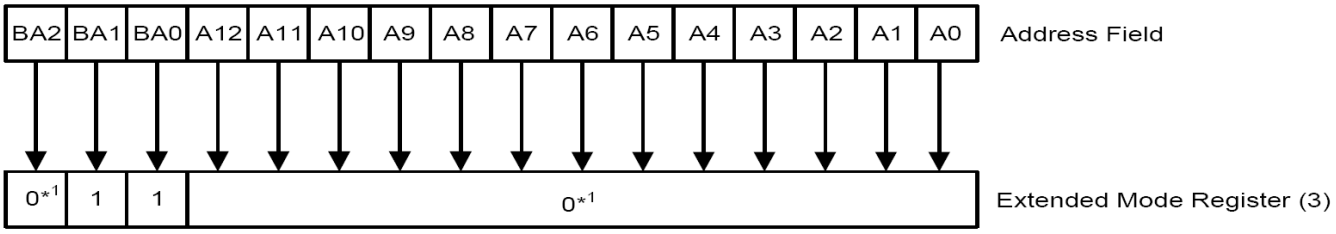
Address input for Extended Mode Register Set EMRS(2)



BA1	BA0	MRS mode
0	0	MRS
0	1	EMR (1)
1	0	EMR (2)
1	1	EMR (3)

A7	High Temperature Self Refresh Rate Enable
0	Disable
1	Enable*2

EMRS (3) Programming: Reserved

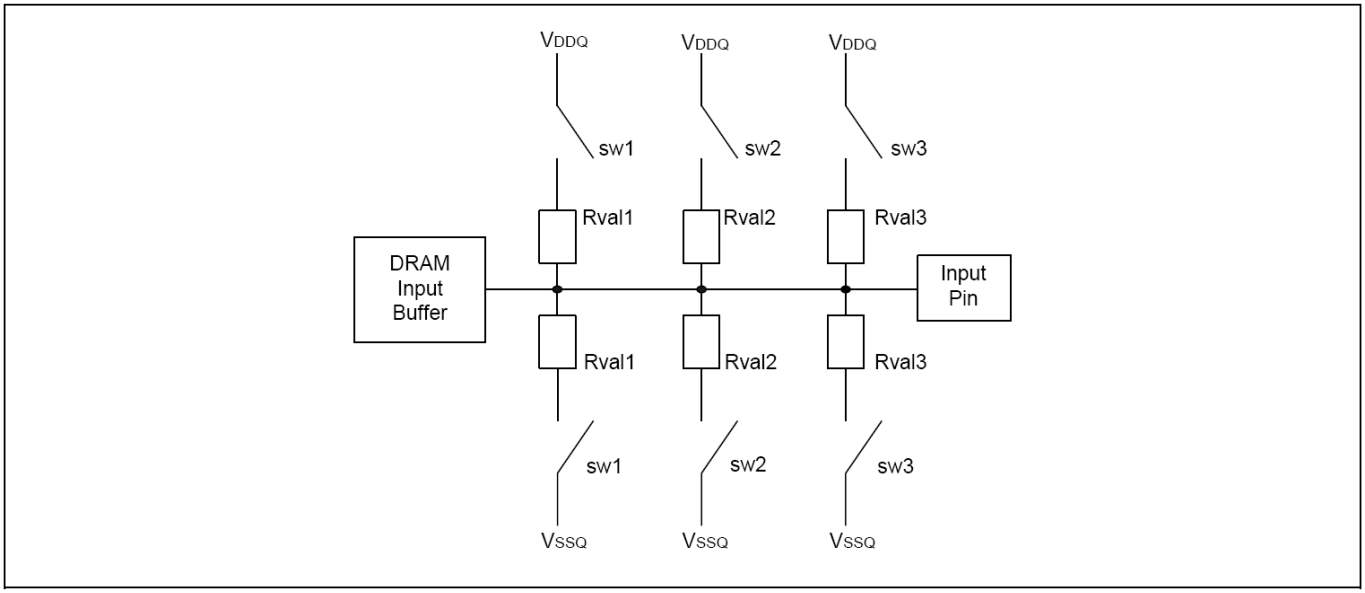


On-Die Termination (ODT)

ODT (On-Die Termination) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, UDQS,/UDQS, LDQS,/LDQS, UDM and LDM signal via the ODT control pin for x16 configuration, where /UDQS and /LDQS are terminated only when enabled in the EMRS(1) by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self- Refresh mode.

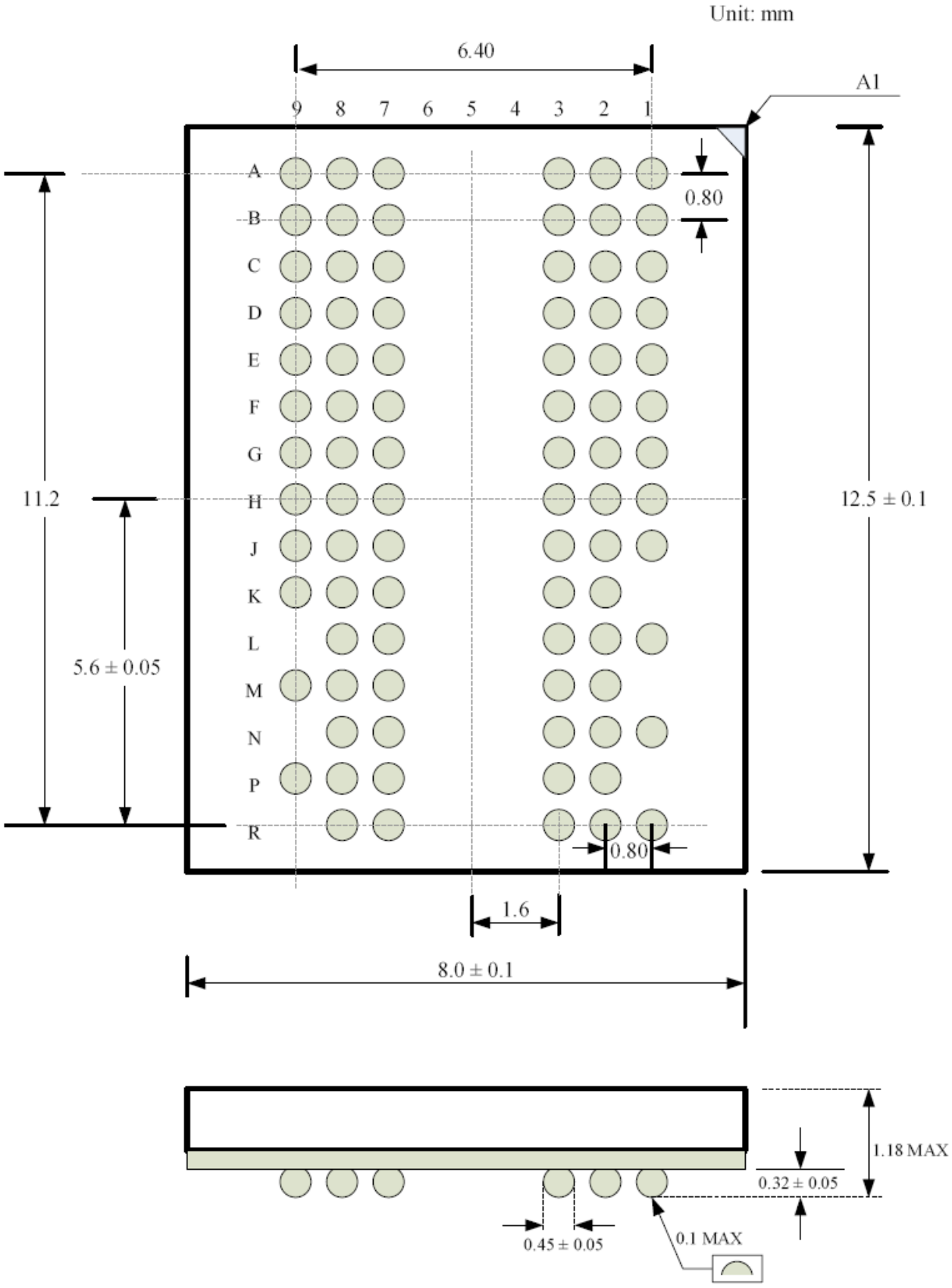
ODT Function



Switch (sw1,sw2,sw3) is enabled by the ODT pin. Selection between sw1, sw2 and sw3 is determined by “Rtt (nominal)” in EMRS(1) address bits A6 & A2. Target Rtt = 0.5 * Rval1 or 0.5 * Rval2.
The ODT pin will be ignored if the EMRS(1) is programmed to disable ODT.

Package Description: 78Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Jul. 2014	Jon Hsu	N/A
1.0	First SPEC. release.	Jul. 2014	Jon Hsu	N/A
1.1	Revise EMRS	May. 2016	Maven Hsu	N/A