

## 1Gb (16M×8Bank×8) DDR 3 SDRAM

### Description

The H2A401G0866B is a 1G bits DDR3 SDRAM, organized as 16,777,216 words × 8 banks × 8 bits. This device achieves high speed transfer rates up to 1600 Mb/sec/pin (DDR3-1600) for various applications.

The H2A401G0866B is designed to comply with the following key DDR3 SDRAM features such as posted /CAS, programmable /CAS Write Latency (CWL), ZQ calibration, on die termination and asynchronous reset. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a differential DQS-DQS# pair in a source synchronous fashion.

### Features

- JEDEC Standard VDD/VDDQ = 1.5V±0.075V.
- Double Data Rate architecture: two data transfers per clock cycle
- Eight internal banks for concurrent operation
- 8 bit prefetch architecture
- CAS Latency: 6, 7, 8, 9, 10 and 11
- Burst length 8 (BL8) and burst chop 4 (BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or nibble sequential
- Bi-directional, differential data strobes (DQS and /DQS) are transmitted / received with data
- Edge-aligned with read data and center-aligned with write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CK and /CK)
- Commands entered on each positive CK edge, data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- Posted CAS with programmable additive latency (AL = 0, CL - 1 and CL - 2) for improved command, address and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Auto-precharge operation for read and write bursts
- Refresh, Self-Refresh, Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Precharged Power Down and Active Power Down
- Data masks (DM) for write data
- Programmable CAS Write Latency (CWL) per operating frequency
- Write Latency WL = AL + CWL
- Interface: SSTL\_15
- Packaged in WBGA 78 Ball (8x10.5 mm<sup>2</sup>), using lead free materials with RoHS compliant

**Ordering Information**

Part No	Organization	Max. Freq	Package	Grade
H2A401G0866BD3C	128M X 8	DDR3-1333MHz 9-9-9	78Ball BGA, 8x10.5mm	Commercial
H2A401G0866BF3C	128M X 8	DDR3-1600MHz 11-11-11	78Ball BGA, 8x10.5mm	Commercial

**Ball Assignments and Descriptions**

78-Ball FBGA – x8 (Top View)

1	2	3		7	8	9
VSS	VDD	NC	A	NU/ /TDQS	VSS	VDD
VSS	VSSQ	DQ0	B	DM/TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS	C	DQ1	DQ3	VSSQ
VSSQ	DQ6	/DQS	D	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	E	DQ7	DQ5	VDDQ
NC	VSS	/RAS	F	CK	VSS	NC
ODT	VDD	/CAS	G	/CK	VDD	CKE
NC	/CS	/WE	H	A10/ /AP	ZQ	NC
VSS	BA0	BA2	J	NC	VREFCA	VSS
VDD	A3	A0	K	A12/ /BC	BA1	VDD
VSS	A5	A2	L	A1	A4	VSS
VDD	A7	A9	M	A11	A6	VDD
VSS	/RESET	A13	N	NC	A8	VSS

**78-Ball FBGA – x8 Ball Descriptions**

Pin	Symbol	Description
F7, G7	CK, /CK	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK.
G9	CKE	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and self-Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power down. Input buffers, excluding CKE, are disabled during self-refresh.
H2	/CS	Chip Select: All commands are masked when CS# is registered HIGH. /CS provides for external Rank selection on systems with multiple ranks. /CS is considered part of the command code.
G1	ODT	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, /DQS and DM/TDQS, NU/ /TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal. The ODT signal will be ignored if Mode Registers MR1 and MR2 are programmed to disable ODT and during self refresh.
F3, G3, H3	/RAS, /CAS, /WE	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
B7	DM	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. The function of DM or TDQS/ /TDQS is enabled by Mode Register A11 setting in MR1.
J2, K8, J3	BA0-BA2	Bank Address Inputs: BA0-BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
K3, L7, L3, K2, L8, L2, M8, M2, N8, M3, H7, M7, K7, N3	A0-A13	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ /BC have additional functions; see below). The address inputs also provide the op-code during Mode Register Set command. Row address: A0-A13. Column address: A0-A9.

Pin	Symbol	Description
H7	A10/AP	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation.(HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
K7	A12/ /BC	Burst Chop: A12/BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped).
N2	/RESET	Active Low Asynchronous Reset: Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rai to rail signal with DC high and low at 80% and 20% of VDD, RESET# active is destructive to data contents.
B3, C7,C2, C8, E3,E8, D2, E7	DQ0–DQ7	Data Input/Output: Bi-directional data bus.
C3, D3	DQS,/ DQS	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. DQS is paired with /DQS to provide differential pair signaling to the system during read and write data transfer. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
B7, A7	TDQS, /TDQS	Termination Data Strobe: When TDQS enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ /TDQS that is applied to DQS/ /DQS. When TDQS disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and /TDQS is not used.
A2, A9, D7, G2, G8, K1, K9, M1, M9	VDD	Power Supply: 1.5V ± 0.075V.
A1, A8, B1, D8, F2,F8, J1, J9, L1, L9, N1, N9	VSS	Ground.
B9, C1, E2, E9	VDDQ	DQ Power Supply: 1.5V ± 0.075V.
B2, B8, C9, D1, D9	VSSQ	DQ Ground.
E1	VREFDQ	Reference voltage for DQ.
J8	VREFCA	Reference voltage for Control, Command and Address inputs.
H8	ZQ	External reference ball for output drive and On-Die Termination Impedance calibration: This ball needs an external 240Ω ± 1% external resistor (RZQ), connected from this ball to ground to perform ZQ calibration.
A3, F1, F9, H1, H9,J7, N7	NC	No Connect: No internal electrical connection is present.

Note: Input only balls (BA0-BA2, A0-A13, /RAS, /CAS, /WE, /CS, CKE, ODT and RESET#) do not supply termination.

## Absolute Maximum Ratings

Symbol	Item	Rating	Unit	Notes
VDD	Voltage on VDD pin relative to VSS	-0.4 ~ 1.975	V	1, 3
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4 ~ 1.975	V	1, 3
VIN, VOUT	Voltage on any pin relative to VSS	-0.4 ~ 1.975	V	1
TSTG	Storage Temperature	-55 ~ 150	°C	1, 2

Note 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Note 3. VDD and VDDQ must be within 300 mV of each other at all times. VREFDQ and VREFCA must not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500 mV, VREFDQ and VREFCA may be equal to or less than 300 mV.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDD	Supply Voltage	1.425	1.5	1.575	V	1, 2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1, 2
RZQ	External Calibration Resistor connected from ZQ ball to ground	237.6	240.0	242.4	Ω	3

Note 1. Under all conditions VDDQ must be less than or equal to VDD.

Note 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Note 3. The external calibration resistor RZQ can be time-shared among DRAMs in special applications.

## Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1333, DDR3-1600		Unit	Notes
		Min.	Max.		
VIH.CA(DC100)	DC input logic high	VREF + 0.100	VDD	V	1, 5
VIL.CA(DC100)	DC input logic low	VSS	VREF - 0.100	V	1, 6
VIH.CA(AC175)	AC input logic high	VREF + 0.175	Note 2	V	1, 2, 7
VIL.CA(AC175)	AC input logic low	Note 2	VREF - 0.175	V	1, 2, 8
VIH.CA(AC150)	AC input logic high	VREF + 0.150	Note 2	V	1, 2, 7
VIL.CA(AC150)	AC input logic low	Note 2	VREF - 0.150	V	1, 2, 8
VIH.CA(AC135)	AC input logic high	-	-	V	1, 2, 7
VIL.CA(AC135)	AC input logic low	-	-	V	1, 2, 8
VIH.CA(AC125)	AC input logic high	-	-	V	1, 2, 7
VIL.CA(AC125)	AC input logic low	-	-	V	1, 2, 8
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 x VDD	0.51 x VDD	V	3, 4

Note 1. For input only pins except RESET#. VREF = VREFCA(DC).

Note 2. See “Overshoot and Undershoot Specifications”.

Note 3. The AC peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than  $\pm 1\%$  VDD (for reference: approx.  $\pm 15$  mV).

Note 4. For reference: approx.  $VDD/2 \pm 15$  mV.

Note 5. VIH(DC) is used as a simplified symbol for VIH.CA(DC100).

Note 6. VIL(DC) is used as a simplified symbol for VIL.CA(DC100).

Note 7. VIH(AC) is used as a simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135), and VIH.CA(AC125); VIH.CA(AC175) value is used when  $VREF + 0.175V$  is referenced, VIH.CA(AC150) value is used when  $VREF + 0.150V$  is referenced, VIH.CA(AC135) value is used when  $VREF + 0.135V$  is referenced, and VIH.CA(AC125) value is used when  $VREF + 0.125V$  is referenced.

Note 8. VIL(AC) is used as a simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC125); VIL.CA(AC175) value is used when  $VREF - 0.175V$  is referenced, VIL.CA(AC150) value is used when  $VREF - 0.150V$  is referenced, VIL.CA(AC135) value is used when  $VREF - 0.135V$  is referenced, and VIL.CA(AC125) value is used when  $VREF - 0.125V$  is referenced.

### Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1333, DDR3-1600		Unit	Notes
		Min.	Max.		
VIH.DQ(DC100)	DC input logic high	$VREF + 0.100$	VDD	V	1, 5
VIL.DQ(DC100)	DC input logic low	VSS	$VREF - 0.100$	V	1, 6
VIH.DQ(AC150)	AC input logic high	$VREF + 0.150$	Note 2	V	1, 2, 7
VIL.DQ(AC150)	AC input logic low	Note 2	$VREF - 0.150$	V	1, 2, 8
VIH.DQ(AC135)	AC input logic high	$VREF + 0.135$	Note 2	V	1, 2, 7
VIL.DQ(AC135)	AC input logic low	Note 2	$VREF - 0.135$	V	1, 2, 8
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	$0.49 \times VDD$	$0.51 \times VDD$	V	3, 4

Note 1. VREF = VREFDQ(DC).

Note 2. See “Overshoot and Undershoot Specifications”.

Note 3. The AC peak noise on VREF may not allow VREF to deviate from VREFDQ(DC) by more than  $\pm 1\%$  VDD (for reference: approx.  $\pm 15$  mV).

Note 4. For reference: approx.  $VDD/2 \pm 15$  mV.

Note 5. VIH(DC) is used as a simplified symbol for VIH.DQ(DC100).

Note 6. VIL(DC) is used as a simplified symbol for VIL.DQ(DC100).

Note 7. VIH(AC) is used as a simplified symbol for VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC150) value is used when  $VREF + 0.150V$  is referenced, and VIH.DQ(AC135) value is used when  $VREF + 0.135V$  is referenced.

Note 8. VIL(AC) is used as a simplified symbol for VIL.DQ(AC150), and VIL.DQ(AC135); VIL.DQ(AC150) value is used when  $VREF - 0.150V$  is referenced, and VIL.DQ(AC135) value is used when  $VREF - 0.135V$  is referenced.

**Input/ Output Capacitance**

Symbol	Parameter	1333 MHz		1600 MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
CIO	Input/output capacitance (DQ,DM,DQS,/DQS, TDQS, /TDQS)	1.4	2.5	1.4	2.3	pF	1, 2, 3
CCK	Input capacitance (CK and /CK)	0.8	1.4	0.8	1.4	pF	2, 3
CDCK	Delta of input capacitance (CK and /CK)	0	0.15	0	0.15	pF	2, 3, 4
CDDQS	Delta of Input/Output capacitance (DQS and /DQS)	0	0.15	0	0.15	pF	2, 3, 5
CI	Input capacitance (CTRL, ADD, CMD input-only pins)	0.75	1.3	0.75	1.3	pF	2, 3, 6
CDI_CTRL	Delta of input capacitance (All CTRL input-only pins)	-0.4	0.2	-0.4	0.2	pF	2, 3, 7, 8
CDI_ADD_CMD	Delta of input capacitance (All ADD/CMD input-only pins)	-0.4	0.4	-0.4	0.4	pF	2, 3, 9, 10
CDIO	Delta of Input/output capacitance (DQ,DM,DQS,/DQS, TDQS, /TDQS)	-0.5	0.3	-0.5	0.3	pF	2, 3, 11
CZQ	Input/output capacitance of ZQ signal	-	3	-	3	pF	2, 3, 12

Note 1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.

Note 2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the ball under test, CKE, /RESET and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.

Note 3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

Note 4. Absolute value of CCK-/CCK.

Note 5. Absolute value of CIO(DQS)-CIO(/DQS).

Note 6. CI applies to ODT, /CS, CKE, A0-A13, BA0-BA2, /RAS,/ CAS, /WE.

Note 7. CDI\_CTRL applies to ODT, /CS and CKE.

Note 8.  $CDI\_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI(/CLK))$ .

Note 9. CDI\_ADD\_CMD applies to A0-A13, BA0-BA2, /RAS, /CAS and /WE.

Note 10.  $CDI\_ADD\_CMD=CI(ADD\_CMD) - 0.5*(CI(CLK)+CI(/CLK))$ .

Note 11.  $CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO(/DQS))$ .

Note 12. Maximum external load capacitance on ZQ signal: 5 pF.

## AC and DC Logic Input Levels for Differential Signals

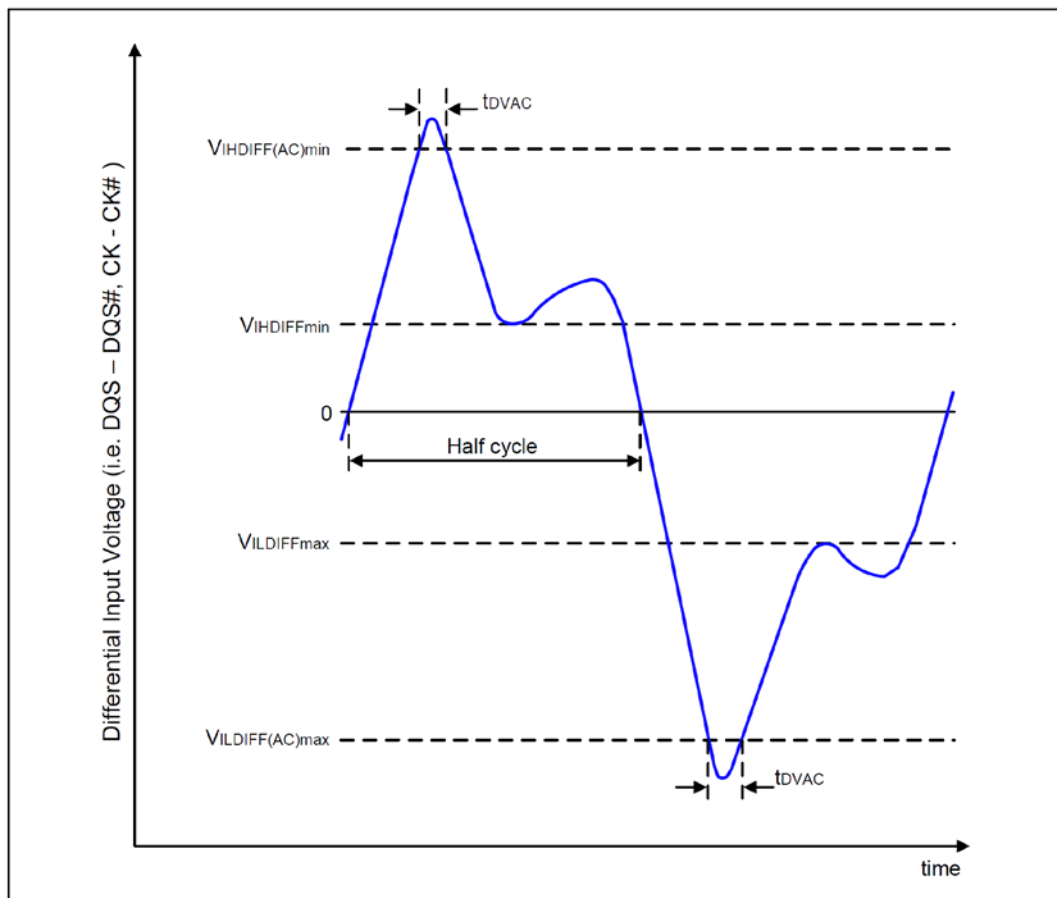
### Differential AC and DC Input Levels

Symbol	Parameter	Min.	Max.	Unit	Notes
VIH.DIFF	Differential input high	+0.200	Note 3	V	1
VIL.DIFF	Differential input low	Note 3	-0.200	V	1
VIH.DIFF(AC)	Differential input high AC	$2 \times (VIH(AC) - VREF)$	Note 3	V	2
VIL.DIFF(AC)	Differential input low AC	Note 3	$2 \times (VIL(AC) - VREF)$	V	2

Note 1. Used to define a differential signal slew-rate.

Note 2. For CK - /CK use VIH.CA(AC)/VIL.CA(AC) of ADD/CMD and VREFCA; for DQS, /DQS use VIH.DQ(AC)/VIL.DQ(AC) of DQs and VREFDQ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.

Note 3. These values are not defined; however, the single-ended signals CK, /CK, DQS, /DQS need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.



Definition of differential ac-swing and “time above AC-level” tDVAC

## Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

### Allowed time before ringback (tDVAC) for CK - /CK and DQS - /DQS

Slew Rate [V/ns]	tDVAC [ps] @  VIH/Ldiff(ac)  = 350mV		tDVAC [ps] @  VIH/Ldiff(ac)  = 300mV	
	Min	Max	Min	Max
-	Min	Max	Min	Max
>4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	119	-
1.8	34	-	102	-
1.6	29	-	81	-
1.4	Note	-	54	-
1.2	Note	-	19	-
1.0	Note	-	Note	-
<1.0	Note	-	Note	-

Note. Rising input differential signal shall become equal to or greater than VIHDIFF(AC) level and Falling input differential signal shall become equal to or less than VILDIFF(AC) level.

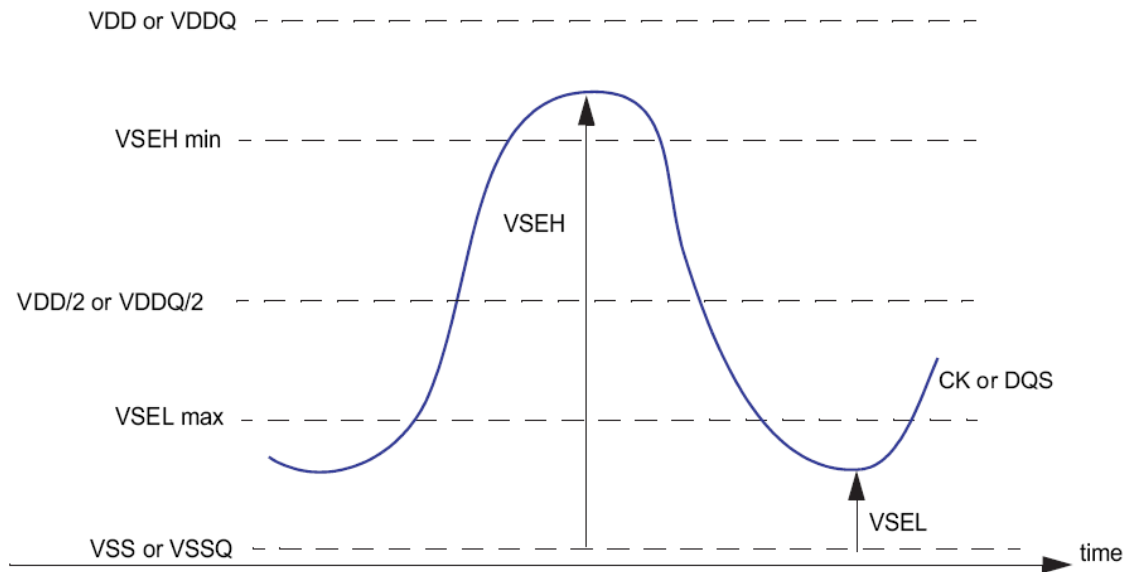
### Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, /CK, /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEHmin / VSELmax (approximately equal to the AC-levels (VIH.CA(AC) / VIL.CA(AC) ) for ADD/CMD signals) in every half-cycle.

DQS, /DQS have to reach VSEHmin / VSELmax (approximately the AC-levels (VIH.DQ(AC) / VIL.DQ(AC) ) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK and /CK.



Single-ended requirement for differential signals

Note that, while ADD/CMD and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

### Single-ended levels for CK, DQS, /CK, /DQS

Symbol	Parameter	Min.	Max.	Unit	Notes
$V_{SEH}$	Single-ended high-level for strobes	$(VDD/2)+0.175$	Note 3	V	1,2
	Single-ended high-level for CK, /CK	$(VDD/2)+0.175$	Note 3	V	1,2
$V_{SEL}$	Single-ended low-level for strobes	Note 3	$(VDD/2)-0.175$	V	1,2
	Single-ended low-level for CK, /CK	Note 3	$(VDD/2)-0.175$	V	1,2

Note 1. For CK, /CK use VIH.CA(AC) / VIL..CA(AC) of ADD/CMD; for strobes (DQS, /DQS) use VIH.DQ(AC) / VIL.DQ(AC) of DQs.

Note 2. VIH.DQ(AC) / VIL.DQ(AC) for DQs is based on VREFDQ; VIH.CA(AC) / VIL.CA(AC) for ADD/CMD is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.

Note 3. These values are not defined; however, the single-ended signals CK, /CK, DQS, DQS# need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

**AC and DC Output Measurement Levels**

Symbol	Parameter	Specification	Units	Notes
V <sub>OH</sub> (DC)	DC output high measurement level (for IV curve linearity)	0.8*VDDQ	V	
V <sub>OM</sub> (DC)	DC output middle measurement level (for IV curve linearity)	0.5*VDDQ	V	
V <sub>OL</sub> (DC)	DC output low measurement level (for IV curve linearity)	0.2*VDDQ	V	
V <sub>OH</sub> (AC)	AC output high measurement level (for output slew rate)	VTT+0.1*VDDQ	V	1
V <sub>OL</sub> (AC)	AC output low measurement level (for output slew rate)	VTT-0.1*VDDQ	V	1

Note. The swing of  $\pm 0.1 \times VDDQ$  is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34  $\Omega$  and an effective test load of 25  $\Omega$  to VTT = VDDQ/2.

**Recommended DC Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	1..425	1.5	1.575	V	1,2
RZQ	External Calibration Resistor connected from ZQ ball to ground	237.6	240	242.4	$\Omega$	1,2,3

## Recommended DC Operating Conditions

VDD/VDDQ = 1.5V±0.075V

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current: CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 39; BL: 8; AL: 0; /CS: High between ACT and PRE; Command, Address; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD1	Operating One Bank Active-Read-Precharge Current: CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 39; BL: 8; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD2N	Precharge Standby Current: CKE: High; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD2NT	Precharge Standby ODT Current: CKE: High; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers.
IDDQ2NT	Precharge Standby ODT IDDQ Current: Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current.
IDD2P0	Precharge Power-Down Current Slow Exit: CKE: Low; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit.
IDD2P1	Precharge Power-Down Current Fast Exit: CKE: Low; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit.
IDD2Q	Precharge Quiet Standby Current: CKE: High; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD3N	Active Standby Current: CKE: High; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 43; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD3P	Active Power-Down Current: CKE: Low; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.

Symbol	Description
IDD4R	Operating Burst Read Current: CKE: High; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: High between RD; Command, Address; Data IO: seamless read data burst with different data; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDDQ4R	Operating Burst Read IDDQ Current: Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	Operating Burst Write Current: CKE: High; External clock: On; tCK, CL: see Table 39; BL: 8; AL: 0; /CS: High between WR; Command, Address; Data IO: seamless write data burst with different data; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH.
IDD5B	Burst Refresh Current: CKE: High; External clock: On; tCK, CL: BL: 8; AL: 0; /CS: High between REF; Command, Address; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD6	Self Refresh Current: Normal Temperature Range: TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see Table 39; BL: 8; AL: 0; /CS, Command, Address, Bank Address, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: MID-LEVEL.
IDD6ET	Self-Refresh Current: Extended Temperature Range: TCASE: 0 - 95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and /CK: LOW; BL: 8; AL: 0; /CS, Command, Address, Bank Address, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: MID-LEVEL.
IDD7	Operating Bank Interleave Read Current: CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 39; BL:8; AL: CL-1; /CS: High between ACT and RDA; Command, Address; Data IO: read data bursts with different data; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0.
IDD8	RESET# Low Current /RESET: Low; External clock: Off; CK and /CK: Low; CKE: FLOATING; /CS, Command, Address, Bank Address, Data IO: FLOATING; ODT Signal: FLOATING /RESET Low current reading is valid once power is stable and RESET has been Low for at least 1mS

Note 1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00b.

Note 2. Output Buffer Enable: set MR1 A[12] = 0b; set MR1 A[5,1] = 01b; Rtt\_Nom enable: set MR1 A[9,6,2] = 011b;  
Rtt\_WR enable: set MR2 A[10,9] = 10b.

Note 3. Pecharge Power Down Mode: set MR0 A12=0b for Slow Exit or MR0 A12=1b for Fast Exit.

Note 4. Auto Self-Refresh (ASR): set MR2 A6 = 0b to disable or 1b to enable feature.

Note 5. Self-Refresh Temperature Range (SRT): set MR2 A7=0b for normal or 1b for extended temperature range.

Note 6. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0b.



**AC Operating Test Characteristics**
**DDR3-1333 & DDR3-1600 Speed Bins**

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Grade	1600MHz		1333MHz		Unit	Notes
	Parameter	Mlin.	Max.	Mlin.	Max.		
Common Notes							1, 2, 3, 4
Clock Input Timing							
tCK(DLL-off)	Minimum clock cycle time (DLL-off mode)	8	–	8	–	nS	45
tCK(avg)	Average Clock Period					pS	
tCH(avg)	Average CK/CK# high pulse width	0.47	0.53	0.47	0.53	tCK(avg)	
tCL(avg)	Average CK/CK# low pulse width	0.47	0.53	0.47	0.53	tCK(avg)	
tCK(abs)	Absolute Clock Period	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				pS	37
tCH(abs)	Absolute CK/CK# high pulse width	0.43	–	0.43	–	tCK(avg)	38
tCL(abs)	Absolute CK/CK# low pulse width	0.43	–	0.43	–	tCK(avg)	39
tJIT(per)	Clock Period Jitter	-70	70	-80	80	pS	
tJIT(per,lck)	Clock Period Jitter during DLL locking period	-60	60	-70	70	pS	
tJIT(cc)	Cycle to Cycle Period Jitter	–	140	–	160	pS	
tJIT(cc,lck)	Cycle to Cycle Period Jitter during DLL locking period	–	120	–	140	pS	
tJIT(duty)	Clock Duty Cycle Jitter	Already included in tCH(abs) and tCL(abs)				pS	
tERR(2per)	Cumulative error across 2 cycles	-103	103	-118	118	pS	
tERR(3per)	Cumulative error across 3 cycles	-122	122	-140	140	pS	
tERR(4per)	Cumulative error across 4 cycles	-136	136	-155	155	pS	
tERR(5per)	Cumulative error across 5 cycles	-147	147	-168	168	pS	
tERR(6per)	Cumulative error across 6 cycles	-155	155	-177	177	pS	
tERR(7per)	Cumulative error across 7 cycles	-163	163	-186	186	pS	
tERR(8per)	Cumulative error across 8 cycles	-169	169	-193	193	pS	
tERR(9per)	Cumulative error across 9 cycles	-175	175	-200	200	pS	
tERR(10per)	Cumulative error across 10 cycles	-180	180	-205	205	pS	
tERR(11per)	Cumulative error across 11 cycles	-184	184	-210	210	pS	
tERR(12per)	Cumulative error across 12 cycles	-188	188	-215	215	pS	
tERR(nper)	Cumulative error across n = 13, 14...49, 50 cycles	Min.: tJIT(per)min * (1 + 0.68 * ln(n)) Max.: tJIT(per)max * (1 + 0.68 * ln(n))				pS	7

Symbol	Speed Grade		1600MHz		1333MHz		Unit	Notes
	Parameter		Mlin.	Max.	Mlin.	Max.		
<b>Data Timing</b>								
tDQSQ	DQS, /QS to DQ skew, per group, per access		-	100	-	125	pS	23
tQH	DQ output hold time from DQS, /DQS		0.38	-	0.38	-	tCK(avg)	18, 23
tLZ(DQ)	DQ low impedance time from CK, /CK		-450	225	-500	250	pS	17, 23, 24
tHZ(DQ)	DQ high impedance time from CK, /CK		-	225	-	250	pS	17, 23, 24
tDS(AC150)	Data setup time to DQS, /DQS	Base specification	10		30		pS	11, 40
		VREF @ 1 V/nS	160		180			11, 40, 42
tDH(DC100)	Data hold time from DQS, /DQS	Base specification	45		65		pS	11, 40
		VREF @ 1 V/nS	145		165			11, 40, 42
tDIPW	DQ and DM input pulse width for each input		360	-	400	-	pS	10
<b>Data Strobe Timing</b>								
tRPRE	DQS,/DQS differential READ Preamble		0.9	Note 21	0.9	Note 21	tCK(avg)	18, 21, 23
tRPST	DQS,/DQS differential READ Postamble		0.3	Note 22	0.3	Note 22	tCK(avg)	18, 22, 23
tQSH	DQS,/DQS differential output high time		0.4	-	0.4	-	tCK(avg)	18, 23
tQSL	DQS,/DQS differential output low time		0.4	-	0.4	-	tCK(avg)	18, 23
tWPRE	DQS,/DQS differential WRITE Preamble		0.9	-	0.9	-	tCK(avg)	46
tWPST	DQS,/DQS differential WRITE Postamble		0.3	-	0.3	-	tCK(avg)	46
tDQSK	DQS,/DQS rising edge output access time from rising CK, /CK		-225	225	-255	255	pS	17, 23
tLZ(DQS)	DQS and /DQS low-impedance time from CK, /CK (Referenced from RL - 1)		-450	225	-500	250	pS	17, 23, 24
tHZ(DQS)	DQS and /DQS high-impedance time from CK, /CK (Referenced from RL + BL/2)		-	225	-	250	pS	17, 23, 24
tDQSL	DQS,/DQS differential input low pulse width		0.45	0.55	0.45	0.55	tCK(avg)	12, 14
tDQSH	DQS,/DQS differential input high pulse width		0.45	0.55	0.45	0.55	tCK(avg)	13, 14
tDQSS	DQS,/DQS rising edge to CK,/CK rising edge		-0.27	0.27	-0.25	0.25	tCK(avg)	16
tDSS	DQS,/DQS falling edge setup time to CK,/CK rising edge		0.18	-	0.2	-	tCK(avg)	15, 16
tDSH	DQS,/DQS falling edge hold time from CK,/CK rising edge		0.18	-	0.2	-	tCK(avg)	15, 16
<b>Command and Address Timing</b>								
tAA	Internal read command to first data		See "Speed Bin"				nS	8
tRCD	ACT to internal read or write delay time						nS	8
tRP	PRE command period						nS	8
tRC	ACT to ACT or REF command period						nS	8
tRAS	ACT to PRE command period						nS	8
tDLLK	DLL locking time		512	-	512	-	nCK	
tRTP	Internal READ Command to PRECHARGE Command delay		max(4nCK, 7.5nS)	-	max(4nCK, 7.5nS)	-		8
tWTR	Delay from start of internal write transaction to internal read command		max(4nCK, 7.5nS)	-	max(4nCK, 7.5nS)	-		8, 26

Symbol	Speed Grade		1600MHz		1333MHz		Unit	Notes
	Parameter		Mlin.	Max.	Mlin.	Max.		
<b>Command and Address Timing</b>								
tWR	WRITE recovery time		15	-	15	-	nS	8, 26
tMRD	Mode Register Set command cycle time		4	-	4	-	nCK	
tMOD	Mode Register Set command update delay		max(12nCK, 15nS)	-	max(12nCK, 15nS)	-		
tCCD	/CAS to /CAS command delay		4	-	4	-	nCK	
tDAL(min)	Auto precharge write recovery + precharge time		WR + roundup(tRP(min)/ tCK(avg))				nCK	6
tMPRR	Multi-Purpose Register Recovery Time		1	-	1	-	nCK	29
tRRD	ACTIVE to ACTIVE command period for 1KB page size		max(4nCK, 6nS)	-	max(4nCK, 6nS)	-		8
tFAW	Four activate window for 1KB page size		30	-	30	-	nS	8
tIS(AC175)	Command and Address setup time to CK, /CK	Base specification	-□		-□		pS	9, 41
		VREF @ 1 V/nS	220		240		pS	9, 41, 42
tIS(AC150)	Command and Address setup time to CK, /CK	Base specification	170		190		pS	9, 41
		VREF @ 1 V/nS	320		340		pS	9, 41, 42
tIH(DC100)	Command and Address hold time from CK, /CK	Base specification	120		140		pS	9, 41
		VREF @ 1 V/nS	220		240		pS	9, 41, 42
tIPW	Control, address and control input pulse width for each input		560	-	620	-	pS	10
<b>Calibration Timing</b>								
tZQinit	Power-up and RESET calibration time		max(512nCK, 640nS)	-	max(512nCK, 640nS)	-		
tZQoper	Normal operation Full calibration time		max(256nCK, 320nS)	-	max(256nCK, 320nS)	-		
tZQCS	Normal operation Short calibration time		max(64nCK, 80nS)	-	max(64nCK, 80nS)	-		33
<b>Reset Timing</b>								
taper	Exit Reset from CKE HIGH to a valid command		max(5nCK, 120nS)	-	max(5nCK, 120nS)	-		
<b>Self Refresh Timing</b>								
tXS	Exit Self Refresh to commands not requiring a locked DLL		max(5nCK, 120nS)	-	max(5nCK, 120nS)	-		34
tXSDLL	Exit Self Refresh to commands requiring a locked DLL		tDLLK(min)	-	tDLLK(min)	-	nCK	35
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing		tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-		
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE)		max(5 nCK, 10nS)	-	max(5 nCK, 10nS)	-		
tCKSRX	Valid Clock Requirement before Self Refresh		max(5 nCK, 10nS)	-	max(5 nCK, 10nS)	-		
<b>Refresh Timing</b>								
tRFC	REF command to ACT or REF command time		110		110		nS	36
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*	-	7.8	-	7.8	μS	
		0°C < TCASE ≤ 85°C	-	7.8	-	7.8	μS	
		85°C ≤ TCASE ≤ 95°C	-	3.9	-	3.9	μS	
		95°C < TCASE ≤ 105°C*	-	3.9	-	3.9	μS	

Symbol	Speed Grade	1600MHz		1333MHz		Unit	Notes
		Min.	Max.	Min.	Max.		
<b>Power Down Timing</b>							
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6nS)	-	max(3nCK, 6nS)	-		34
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24nS)	-	max(10nCK, 24nS)	-		35
tCKE	CKE minimum pulse width	max(3nCK, 5nS)	-	max(3nCK, 5.625nS)	-		
tCPDED	Command pass disable delay	1	-	1	-	nCK	
tPD	Power Down Entry to Exit Timing	tCKE(min)	9 * tREFI	tCKE(min)	9 * tREFI		25
tACTPDEN	Timing of ACT command to Power Down entry	1	-	1	-	nCK	27
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	1	-	nCK	27
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	Min.: WL + 4 + roundup (tWR(min)/ tCK(avg))				nCK	20
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	Min.: WL + 4 + WR + 1				nCK	19
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	Min.: WL + 2 + roundup (tWR(min)/ tCK(avg))				nCK	20
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	Min.: WL + 2 + WR + 1				nCK	19
tREFPDEN	Timing of REF command to Power Down entry	1	-	1	-	nCK	27, 28
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	tMOD(min)	-		
<b>ODT Timing</b>							
ODTH4	ODT high time without write command or with write command and burst chop 4	4	-	4	-	nCK	30
ODTH8	ODT high time with Write command and burst length 8	6	-	6	-	nCK	31
tAONPD	Asynchronous RTT turn-on delay (Power Down with DLL frozen)	2	8.5	2	8.5	nS	32
tAOFPD	Asynchronous RTT turn-off delay (Power Down with DLL frozen)	2	8.5	2	8.5	nS	32
tAON	RTT turn-on	-225	225	-250	250	pS	17, 43
tAOF	Rtt_Nom and Rtt_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tCK(avg)	17, 44
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	tCK(avg)	17
<b>Write Leveling Timing</b>							
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	40	-	nCK	5
tWLDQSEN	DQS/ /DQS delay after write leveling mode is programmed	25	-	25	-	nCK	5
tWLS	Write leveling setup time from (CK, /CK) zero crossing to rising (DQS, /DQS) zero crossing	165	-	195	-	pS	
tWLH	Write leveling hold time from rising (DQS, /DQS)	165	-	195	-	pS	
tWLO	Write leveling output delay	0	7.5	0	9	nS	
tWLOE	Write leveling output error	0	2	0	2	nS	

- Note 1. Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.  
For example, tMRD = 4 [nCK] means; if one Mode Register Set command is registered at T<sub>m</sub>, another Mode Register Set command may be registered at T<sub>m</sub>+4, even if (T<sub>m</sub>+4 - T<sub>m</sub>) is 4 x tCK(avg) + tERR(4per),min (which is smaller than 4 x tCK(avg)).
- Note 2. Timing that is not specified is illegal and after such an event, in order to provide proper operation, the DRAM must be resetted or powered down and then restarted through the specified initialization sequence before normal operation can continue.
- Note 3. The CK/ /CK input reference level (for timing reference to CK / /CK) is the point at which CK and /CK cross. The DQS/ /DQS input reference level is the point at which DQS and /DQS cross;  
The input reference level for signals other than CK/ /CK, DQS//DQS and /RESET is VREFCA and VREFDQ respectively.
- Note 4. Inputs are not recognized as valid until VREFCA stabilizes within specified limits.
- Note 5. The max values are system dependent.
- Note 6. tCK(avg) refers to the actual application clock period. WR refers to the WR parameter stored in mode register MR0.
- Note 7. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
- Note 8. For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [nS] / tCK(avg) [nS] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.  
For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-1333 (9-9-9), of which tRP = 13.5nS, the device will support tnRP = RU{tRP / tCK(avg)} = 9, as long as the input clock jitter specifications are met, i.e. Precharge command at T<sub>m</sub> and Active command at T<sub>m</sub>+9 is valid even if (T<sub>m</sub>+9 - T<sub>m</sub>) is less than 13.5nS due to input clock jitter.
- Note 9. These parameters are measured from a command/address signal (CKE, CS#, /RAS, /CAS, /WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK//CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- Note 10. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
- Note 11. These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
- Note 12. tDQSL describes the instantaneous differential input low pulse width on DQS - /DQS, as measured from one falling edge to the next consecutive rising edge.
- Note 13. tDQSH describes the instantaneous differential input high pulse width on DQS - /DQS, as measured from one rising edge to the next consecutive falling edge.
- Note 14. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
- Note 15. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
- Note 16. These parameters are measured from a data strobe signal (DQS, /DQS) crossing to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters

should be met whether clock jitter is present or not.

Note 17. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{ERR}(mper)$ , act of the input clock, where  $2 \leq m \leq 12$ . (output deratings are relative to the actual SDRAM input clock.)

For example, if the measured jitter into a DDR3-1333 SDRAM has  $t_{ERR}(mper),act,min} = -138$  pS and  $t_{ERR}(mper),act,max} = +155$  pS, then  $t_{DQCK,min}(derated) = t_{DQCK,min} - t_{ERR}(mper),act,max} = -255$  pS - 155 pS = -410 pS and  $t_{DQCK,max}(derated) = t_{DQCK,max} - t_{ERR}(mper),act,min} = 255$  pS + 138 pS = +393 pS.

Similarly,  $t_{LZ}(DQ)$  for DDR3-1333 derates to  $t_{LZ}(DQ),min(derated) = -500$  pS - 155 pS = -655 pS and  $t_{LZ}(DQ),max(derated) = 250$  pS + 138 pS = +388 pS. (Caution on the min/max usage!)

Note that  $t_{ERR}(mper),act,min}$  is the minimum measured value of  $t_{ERR}(nper)$  where  $2 \leq n \leq 12$ , and  $t_{ERR}(mper),act,max}$  is the maximum measured value of  $t_{ERR}(nper)$  where  $2 \leq n \leq 12$ .

Note 18. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT}(per)$ , act of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-1333 SDRAM has  $t_{CK}(avg),act} = 1500$  pS,  $t_{JIT}(per),act,min} = -58$  pS and  $t_{JIT}(per),act,max} = +74$  pS, then  $t_{RPRE,min}(derated) = t_{RPRE,min} + t_{JIT}(per),act,min} = 0.9 \times t_{CK}(avg),act} + t_{JIT}(per),act,min} = 0.9 \times 1500$  pS - 58 pS = +1292 pS.

Similarly,  $t_{QH,min}(derated) = t_{QH,min} + t_{JIT}(per),act,min} = 0.38 \times t_{CK}(avg),act} + t_{JIT}(per),act,min} = 0.38 \times 1500$  pS - 58 pS = +512 pS. (Caution on the min/max usage!).

Note 19. WR in clock cycles as programmed in mode register MR0.

Note 20.  $t_{WR}(min)$  is defined in nS, for calculation of  $t_{WRPDEN}$  it is necessary to round up  $t_{WR}(min)/t_{CK}(avg)$  to the next integer value.

Note 21. The maximum read preamble is bound by  $t_{LZ}(DQS)min$  on the left side and  $t_{DQCK}(max)$  on the right side.

Note 22. The maximum read postamble is bound by  $t_{DQCK}(min)$  plus  $t_{QSH}(min)$  on the left side and  $t_{HZ}(DQS)max$  on the right side.

Note 23. Value is only valid for RON34.

Note 24. Single ended signal parameter.

Note 25.  $t_{REFI}$  depends on TOPER.

Note 26. Start of internal write transaction is defined as follows:

For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.

For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.

For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

Note 27.  $t_{CKE}$  is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power down  $I_{DD}$  spec will not be applied until finishing those operations.

Note 28. Although  $t_{CKE}$  is allowed to be registered LOW after a REFRESH command once  $t_{REFPDEN}(min)$  is satisfied, there are cases where additional time such as  $t_{XPDLL}(min)$  is also required.

Note 29. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

Note 30.  $t_{ODTH4}$  is measured from ODT first registered high (without a Write command) to ODT first registered low, or from ODT registered high together with a Write command with burst length 4 to ODT registered low.

Note 31.  $t_{ODTH8}$  is measured from ODT registered high together with a Write command with burst length 8 to ODT registered low.

Note 32. This parameter applies upon entry and during precharge power down mode with DLL frozen.

Note 33. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity'

tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature ( $T_{driftrate}$ ) and voltage ( $V_{driftrate}$ ) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQ Correction}}{(TSens \times T_{driftrate}) + (VSens \times V_{driftrate})}$$

where  $TSens = \max(dRTTdT, dRONdTM)$  and  $VSens = \max(dRTTdV, dRONdVM)$  define the SDRAM temperature and voltage sensitivities.

Note 34. Commands not requiring a locked DLL are all commands except Read, Read with Auto-Precharge and Synchronous ODT.

Note 35. Commands requiring a locked DLL are Read, Read with Auto-Precharge and Synchronous ODT.

Note 36. A maximum of one regular plus eight posted refresh commands can be issued to any given DDR3 SDRAM device meaning that the maximum absolute interval between any refresh command and the next refresh command is  $9 \times tREFI$ .

Note 37. Parameter  $tCK(avg)$  is specified per its average value. However, it is understood that the relationship between the average timing  $tCK(avg)$  and the respective absolute instantaneous timing  $tCK(abs)$  holds all times.

Note 38.  $tCH(abs)$  is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

Note 39.  $tCL(abs)$  is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Note 40.  $tDS(base)$  and  $tDH(base)$  values are for a single-ended  $1V/nS$  slew rate DQs (DQs are at  $2V/nS$  for DDR3-1866) and  $2V/nS$  DQS, /DQS differential slew rate. Note for DQ and DM signals,  $VREF(DC) = VREFDQ(DC)$ . For input only pins except /RESET,  $VREF(DC) = VREFCA(DC)$ .

Note 41.  $tIS(base)$  and  $tIH(base)$  values are for  $1V/nS$  CMD/ADD single-ended slew rate and  $2V/nS$  CK, /CK differential slew rate. Note for DQ and DM signals,  $VREF(DC) = VREFDQ(DC)$ . For input only pins except /RESET,  $VREF(DC) = VREFCA(DC)$ .

Note 42. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is  $1 V/nS$  (DQs are at  $2V/nS$  for DDR3-1866). These values, with a slew rate of  $1 V/nS$  (DQs are at  $2V/nS$  for DDR3-1866), are for reference only.

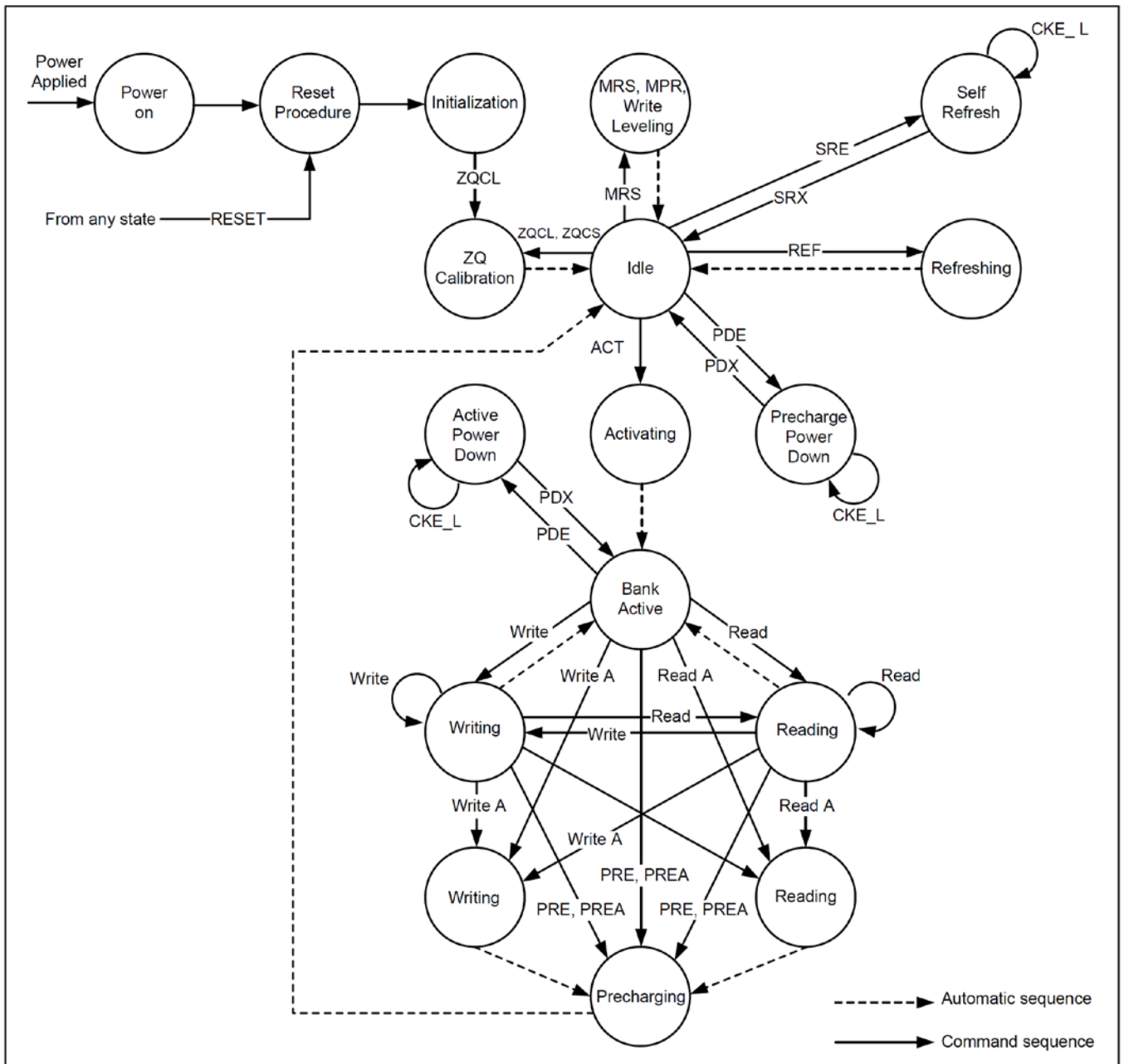
Note 43. For definition of RTT turn-on time  $tAON$  See "Timing Parameters".

Note 44. For definition of RTT turn-off time  $tAOF$  See "Timing Parameters".

Note 45. There is no maximum cycle time limit besides the need to satisfy the refresh interval,  $tREFI$ .

Note 46. Actual value dependant upon measurement level.

**Simplified State Diagram**



**Command Truth Table**

Symbol	Command	CKE		/CS	/RAS	/CAS	/WE	BA0-BA2	A13	A12/ /BC	A10/ AP	A0~ A9, A11	Notes
		Previous Cycle	Current Cycle										
MRS	Mode Register Set	H	H	L	L	L	L	BA	OP Code				
REF	Refresh	H	H	L	L	L	H	V	V	V	V	V	
SRE	Self Refresh Entry	H	L	L	L	L	H	V	V	V	V	V	7,9,12
SRX	Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
PRE	Single Bank Precharge	H	H	L	L	H	L	BA	V	V	L	V	
PREA	Precharge all Banks	H	H	L	L	H	L	V	V	V	H	V	
ACT	Bank Activate	H	H	L	L	H	H	BA	Row Address (RA)				
WR	Write (Fixed BL8 or BC4)	H	H	L	H	L	L	BA	RFU	V	L	CA	5
WRS4	Write (BC4, on the Fly)	H	H	L	H	L	L	BA	RFU	L	L	CA	5
WRS8	Write (BL8, on the Fly)	H	H	L	H	L	L	BA	RFU	H	L	CA	5
WRA	Write with Auto Precharge (Fixed BL8 or BC4)	H	H	L	H	L	L	BA	RFU	V	H	CA	5
WRAS4	Write with Auto Precharge (BC4, on the Fly)	H	H	L	H	L	L	BA	RFU	L	H	CA	5
WRAS8	Write with Auto Precharge (BL8, on the Fly)	H	H	L	H	L	L	BA	RFU	H	H	CA	5
RD	Read (Fixed BL8 or BC4)	H	H	L	H	L	H	BA	RFU	V	L	CA	5
RDS4	Read (BC4, on the Fly)	H	H	L	H	L	H	BA	RFU	L	L	CA	5
RDS8	Read (BL8, on the Fly)	H	H	L	H	L	H	BA	RFU	H	L	CA	5
RDA	Read with Auto Precharge (Fixed BL8 or BC4)	H	H	L	H	L	H	BA	RFU	V	H	CA	5
RDAS4	Read with Auto Precharge (BC4, on the Fly)	H	H	L	H	L	H	BA	RFU	L	H	CA	5
RDAS8	Read with Auto Precharge (BL8, on the Fly)	H	H	L	H	L	H	BA	RFU	H	H	CA	5
NOP	No Operation	H	H	L	H	H	H	V	V	V	V	V	10
DES	Device Deselected	H	H	H	X	X	X	X	X	X	X	X	11
PDE	Power Down Entry	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
PDX	Power Down Exit	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQCL	ZQ Calibration Long	H	H	L	H	H	L	X	X	X	H	X	
ZQCS	ZQ Calibration Short	H	H	L	H	H	L	X	X	X	L	X	

Note 1. All DDR3 SDRAM commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

Note 2. /RESET is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

Note 3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Note 4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

Note 5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-fly BL will be defined by MRS.

Note 6. The Power Down Mode does not perform any refresh operation.

Note 7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note 8. Self Refresh Exit is asynchronous.

Note 9. VREF (Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VREFDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note 10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Note 11. The Deselect command performs the same function as No Operation command.

Note 12. Refer to the CKE Truth Table for more detail with CKE transition.

## CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18
For more details with all signals, see "Command Truth Table"					10

- Note1. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
- Note2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.
- Note3. Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.
- Note4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- Note5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
- Note6. During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
- Note7. DESELECT and NOP are defined in the "Command Truth Table".
- Note8. On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
- Note9. Self-Refresh mode can only be entered from the All Banks Idle state.
- Note10. Must be a legal command as defined in the "Command Truth Table".
- Note11. Valid commands for power-down entry and exit are NOP and DESELECT only.
- Note12. Valid commands for self-refresh exit are NOP and DESELECT only.
- Note13. Self-Refresh can not be entered during Read or Write operations.
- Note14. The Power-Down does not perform any refresh operations.
- Note15. "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
- Note16. VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.
- Note17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
- Note18. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

## Initialization

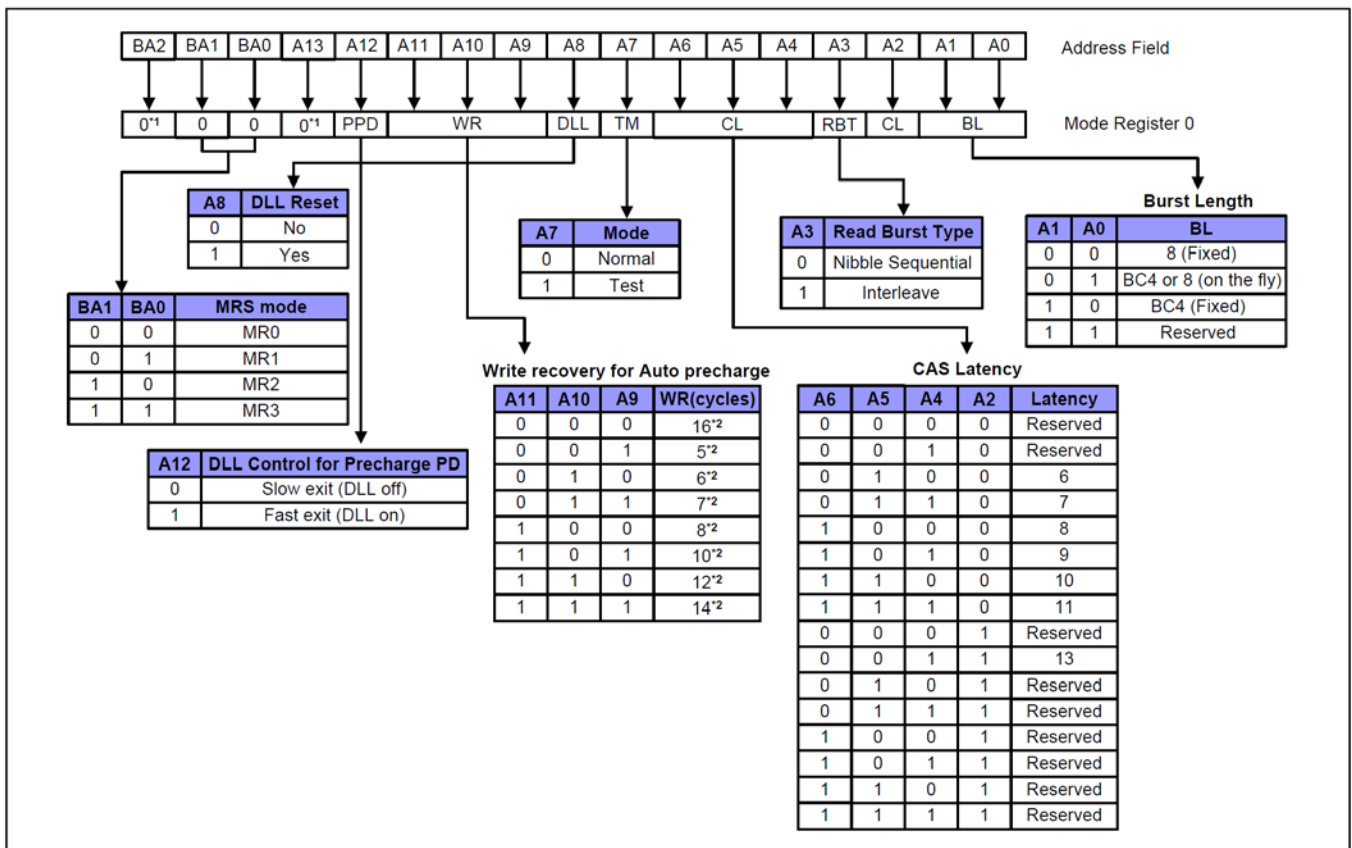
The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below  $0.2 \times VDD$ ; all other inputs may be undefined). /RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp,  $VDD > VDDQ$  and  $(VDD - VDDQ) < 0.3$  volts.
  - VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
  - Vref tracks VDDQ/2. OR
  - Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT\_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ( $tXPR = \max(tXS ; 5 \times tCK)$ )
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

## Mode Register Definition

### Mode Register MR0

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



Note 1. BA2 and A13 are reserved for future use and must be programmed to 0 during MRS.

Note 2. WR (write recovery for Auto precharge)min in clock cycles is calculated by dividing tWR (in nS) by tCK (in nS) and rounding up to the next integer:  $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{nS}] / tCK(\text{avg})[\text{nS}])$ .

The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Note 3. The table only shows the encodings for a given Cas Latency.

Note 4. The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

**Burst Type (A3)**

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0 1 2 3 T T T T	0 1 2 3 T T T T
	R	0	0	1	1 2 3 0 T T T T	1 0 3 2 T T T T
	R	0	1	0	2 3 0 1 T T T T	2 3 0 1 T T T T
	R	0	1	1	3 0 1 2 T T T T	3 2 1 0 T T T T
	R	1	0	0	4 5 6 7 T T T T	4 5 6 7 T T T T
	R	1	0	1	5 6 7 4 T T T T	5 4 7 6 T T T T
	R	1	1	0	6 7 4 5 T T T T	6 7 4 5 T T T T
	R	1	1	1	7 4 5 6 T T T T	7 6 5 4 T T T T
	W	0	V	V	0 1 2 3 X X X X	0 1 2 3 X X X X
	W	1	V	V	4 5 6 7 X X X X	4 5 6 7 X X X X
8	R	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	R	0	0	1	1 2 3 0 5 6 7 4	1 0 3 2 5 4 7 6
	R	0	1	0	2 3 0 1 6 7 4 5	2 3 0 1 6 7 4 5
	R	0	1	1	3 0 1 2 7 4 5 6	3 2 1 0 7 6 5 4
	R	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	R	1	0	1	5 6 7 4 1 2 3 0	5 4 7 6 1 0 3 2
	R	1	1	0	6 7 4 5 2 3 0 1	6 7 4 5 2 3 0 1
	R	1	1	1	7 4 5 6 3 0 1 2	7 6 5 4 3 2 1 0
	W	V	V	V	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7

Note1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12 (/BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Note2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

Note3. T: Output driver for data and strobes are in high impedance.

Note4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

Note5. X: Don't Care.

### **CAS Latency**

The CAS Latency is defined by MR0 (bits A2, A4, A5 and A6) as shown in Figure 5. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL);  $RL = AL + CL$ .

### **Test Mode**

The normal operating mode is selected by MR0 (bit A7 = 0) and rest bits set to the desired values. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM factory and should NOT be used. No operations or functionality is specified if A7 = 1.

### **DLL Reset**

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

### **Write Recovery**

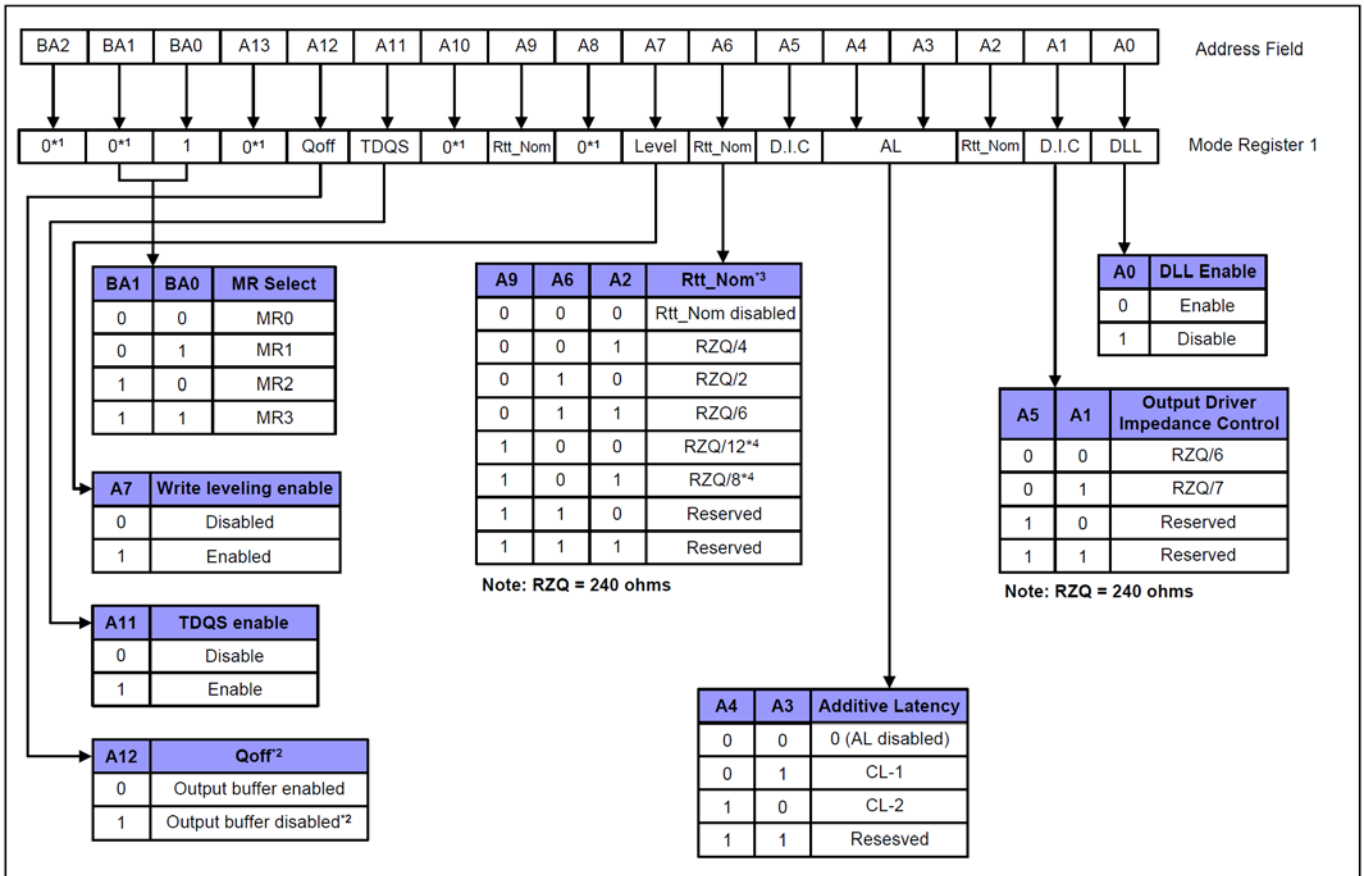
The programmed WR value MR0 (bits A9, A10 and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in nS) by tCK(avg) (in nS) and rounding up to the next integer:  $WR_{min}[cycles] = \text{Round up}(tWR[nS]/tCK(avg)[nS])$ . The WR must be programmed to be equal to or larger than tWR(min).

### **Precharge PD DLL**

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

### Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt\_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.



Note 1. BA2, A8, A10 and A13 are reserved for future use and must be programmed to 0 during MRS.

Note 2. Outputs disabled - DQs, DQSs, /DQSs.

Note 3. In Write leveling Mode (MR1 A[7] = 1) with MR1 A[12]=1, all Rtt\_Nom settings are allowed; in Write Leveling Mode (MR1 A[7]= 1) with MR1 A[12]=0, only Rtt\_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

Note 4. If Rtt\_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

### ***DLL Enable***

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled upon exit of Self Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when Rtt\_WR is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the Rtt\_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt\_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

### ***ODT Rtt Values***

DDR3 SDRAM is capable of providing two different termination values (Rtt\_Nom and Rtt\_WR). The nominal termination value Rtt\_Nom is programmed in MR1. A separate value (Rtt\_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled.

### ***Additive Latency***

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, It allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings.

### ***Write Leveling***

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

### ***Output Disable***

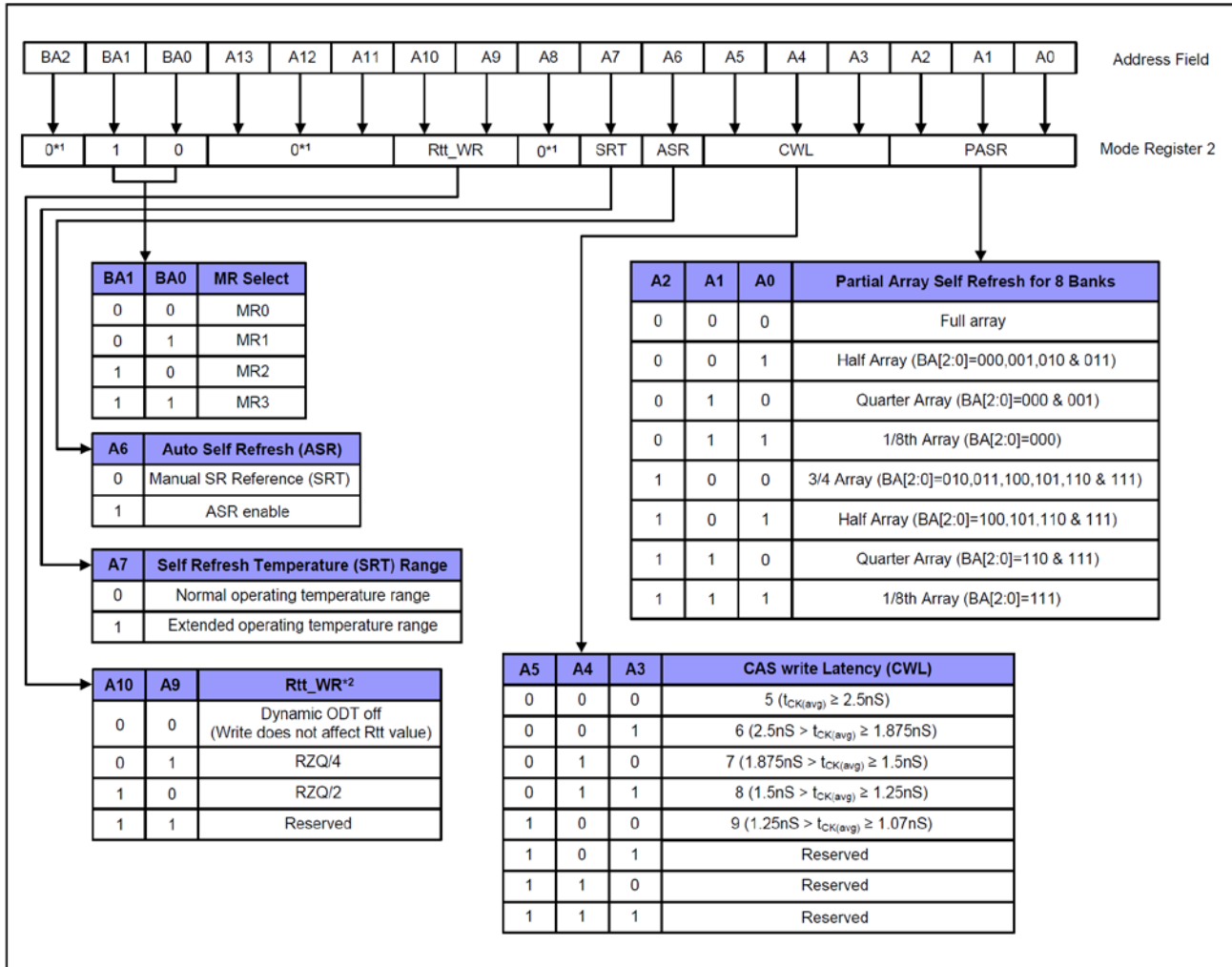
The outputs may be enabled/disabled by MR1 (bit A12). When this feature is enabled (A12 = 1), all output pins (DQs, DQS, /DQS, etc.) are disconnected from the device, thus removing any loading of the output drivers. For normal operation, A12 should be set to '0'.

### ***TQS, /TDQS***

TDQS (Termination Data Strobe) provides additional termination resistance outputs that may be useful in some system configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS & /TDQS pins that is applied to the DQS & /DQS pins. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS. The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the /TDQS pin is not used.

## Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, including RTT\_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.



Note 1. BA2, A8, A11~A13 are reserved for future use and must be programmed to 0 during MRS.

Note 2. The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled. During write leveling, Dynamic ODT is not available.

### ***CAS Write Latency (CWL)***

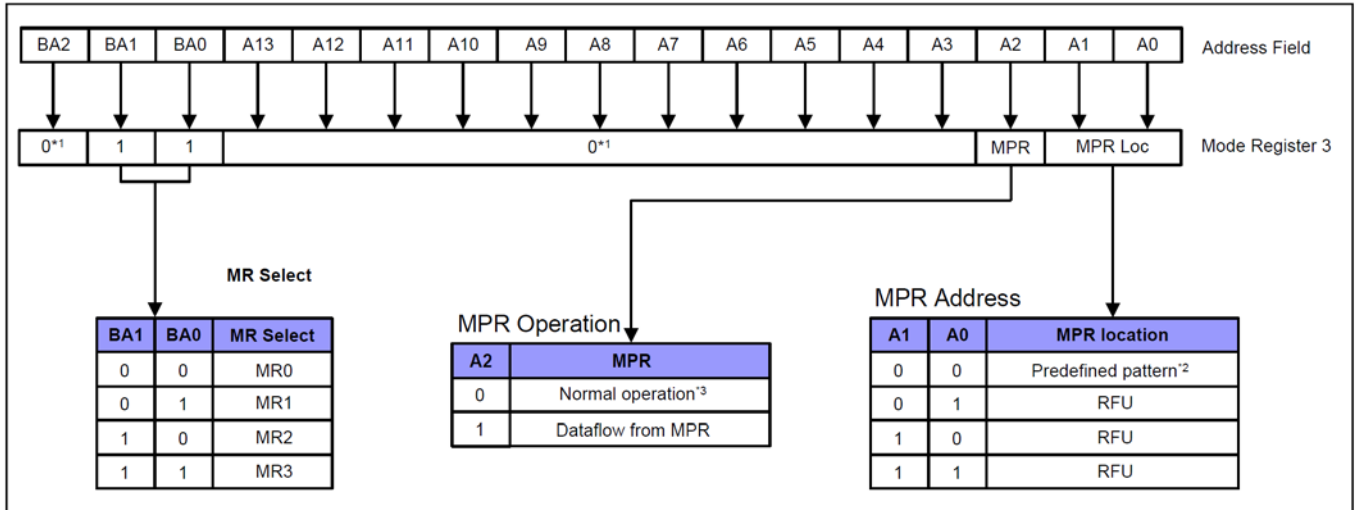
The CAS Write Latency is defined by MR2 (bits A3-A5). CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL);  $WL = AL + CWL$ .

### ***Dynamic ODT (Rtt<sub>WR</sub>)***

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only Rtt<sub>Nom</sub> is available.

### Mode Register MR3

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



Note 1. BA2, A3~A13 are reserved for future use and must be programmed to 0 during MRS.

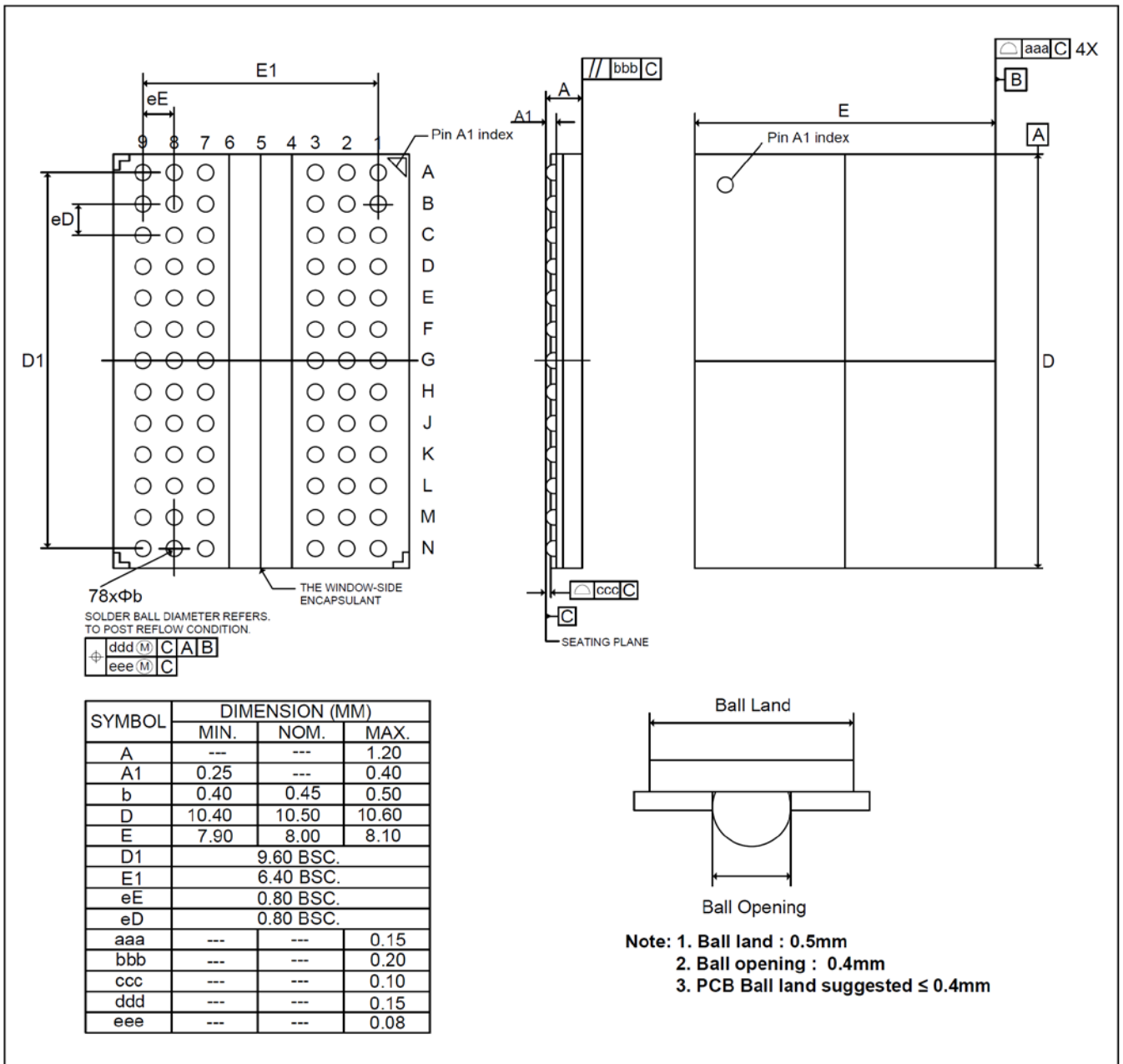
Note 2. The predefined pattern will be used for read synchronization.

Note 3. When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

### Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-down mode, self-refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

## Package Description: 78Ball-WBGA



**Revision History**

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Sep. 2014	Hermon Chen	N/A
1.0	First SPEC. release.	Sep. 2014	Hermon Chen	N/A