1Gb (16Mx4Banksx8) DDR2 SDRAM

Descriptions

The H2A35120856B is a 512M bits DDR2 SDRAM, organized as 16,777,216 words x 4 banks x 8 bits. This device achieves high speed transfer rates up to 800Mb/sec/pin (DDR2-800) for general applications. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and /CLK falling). All I/Os are synchronized with a single ended DQS or differential DQS- /DQS pair in a source synchronous fashion.

Features

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, 5 and 6
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS an/DQS) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and /CLK)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted /CAS programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18
- Packaged in WBGA 60 Ball (8X12.5 mm^2), using Lead free materials with RoHS compliant

Ordering Information

Part No	Organization	Max. Freq	Package	Grade
H2A35120856BB6C	64M X 8	DDR2-800MHz 6-6-6	60Ball BGA, 8x12.5mm	Commercial
H2A35120856BA6C	64M X 8	DDR2-667MHz 5-5-5	60Ball BGA, 8x12.5mm	Commercial

Ball Assignments and Descriptions

60-Ball FBGA – x8 (Top View)

1	2	3	5	7	8	9
VDD	NU/ /RDQS	VSS	A	VSSQ	/DQS	VDDQ
DQ6	VSSQ	DM/RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CLK	VDD
	CKE	/WE	F	/RAS	/CLK	ODT
NC	BA0	BA1	G	/CAS	/CS	
	A10/AP	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

60-Ball FBGA – x8 Ball Descriptions

Pin	Name	Function
H8,H3,H7,J2,J8,J3, J7,K2,K8,K3,H2,K7, L2,L8	A0−A13	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0−A13. Column address: A0−A9. (A10 is used for Auto-precharge)
G2,G3	BA0−BA1	BA0−BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or one of the extended mode registers is to be accessed during a MRS or EMRS command cycle.
C8,C2,D7,D3,D1,D9, B1,B9	DQ0−DQ7	Bi-directional data bus.
F9	ODT	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
B7,A8	DQS, /DQS	Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. /DQS is only used when differential data strobe mode is enabled via the control bit at EMR (1) [A10] = 0.
G8	CS	All commands are masked when /CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
F7,G7,F3	/RAS , /CAS, /WE	/RAS , /CAS and /WE (along with /CS) define the command being entered.
B3	DM/RDQS	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is input only, the DM loading matches the DQ and DQS loading. When RDQS is enabled, RDQS is output with read data only and is ignored during write data. RDQS is enabled by EMR (1) [A11] = 1. If RDQS is enabled, the DM function is disabled.
A2	NU/ /RDQS	/RDQS is only used when RDQS is enabled and differential data strobe mode is enabled. If differential data strobe mode is disabled via the control bit at EMR (1) [A10] = 1, then ball A2 and A8 are not used.
E8,F8	CLK, /CLK	CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK . Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
F2	CKE	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
E2	VREF	VREF is reference voltage for inputs.
A1,E9,H9,L1	VDD	Power Supply: 1.8V ± 0.1V.
A3,E3,J1,K9	VSS	Ground

A9,C1,C3,C7,C9	VDDQ	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8	VSSQ	DQ Ground. Isolated on the device for improved noise immunity.
G1,L3,L7	NC	No connection.
E1	VDDL	DLL Power Supply: 1.8V ± 0.1V.
E7	VSSDL	DLL Ground.

Absolute Maximum Ratings

Symbol	Item	Rating	Unit	Notes
VDD	Voltage on VDD pin relative to VSS	-1.0 ~ 2.3	V	1, 2
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5 ~ 2.3	V	1, 2
VDDL	Voltage on VDDL pin relative to VSS	-0.5 ~ 2.3	V	1, 2
VIN, VOUT	Voltage on any pin relative to VSS	-0.5 ~ 2.3	V	1, 2
TSTG	Storage Temperature	-55 ~ 100	℃	1, 2, 3

Note 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2. When VDD and VDDQ and VDDL are less than 500mV; VREF may be equal to or less than 300mV.

Note 3. Storage temperature is the case surface temperature on the center/top side of the DRAM.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	2, 3
VTT	Termination Voltage (System)	VREF - 0.04	VREF	VREF + 0.04	V	4

Note 1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must than or equal to VDD.

Note 2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

Note 3. Peak to peak AC noise on VREF may not exceed ±2 % VREF(dc).

Note 4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and device must track VREF of receiving device.

Note 5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	Min.	Max.	Unit
V_{IH}(DC)	DC input logic high	VREF+0.125	VDDQ+0.3	V
V_{IL}(DC)	DC input logic low	-0.3	VREF-0.125	V
V_{IH}(AC)	AC input logic high	VREF+0.200	-	V
V_{IL}(AC)	AC input logic low	-	VREF-0.200	V

Note . Refer to the page 67 sections 9.14.1 and 9.14.2 AC Overshoot/Undershoot specification table for VPEAK value: maximum peak amplitude allowed for Overshoot/Undershoot.

Input/ Output Capacitance

Symbol	Parameter	Min.	Max.	Unit
CCK	Input Capacitance , CLK and /CLK	1.0	2.0	pF
CDCK	Input Capacitance delta , CLK and /CLK	-	0.25	pF
CI	Input Capacitance, all other input-only pins	1.0	2.0	pF
CDI	Input Capacitance delta, all other input-only pins	-	0.25	pF
CIO	Input/output Capacitance, DQ, DM, DQS,/DQS ,RDQS, /RDQS	2.5	3.5	pF
CDIO	Input/output Capacitance delta, DQ, DM, DQS,/DQS ,RDQS, /RDQS	-	0.5	pF

AC and DC Logic Input Levels for Differential Signals

Differential Input/Output AC Logic Levels

Symbol	Parameter	Min.	Max.	Unit	Notes
VID (ac)	AC differential input voltage	0.5	VDDQ + 0.6	V	1
VIX (ac)	AC differential cross point	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2
VOX (ac)	AC differential cross point	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	3

Note 1. VID (ac) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CLK, DQS) and VCP is the complementary input signal (such as CLK , DQS). The minimum value is equal to VIH (ac) -VIL (ac).

Note 2. The typical value of VIX (ac) is expected to be about 0.5 x VDDQ of the transmitting device and VIX (ac) is expected to track variations in VDDQ. VIX (ac) indicates the voltage at which differential input signals must cross.

Note 3. The typical value of VOX (ac) is expected to be about 0.5 x VDDQ of the transmitting device and VOX (ac) is expected to track variations in VDDQ. VOX (ac) indicates the voltage at which differential output signals must cross.

Recommended DC Operating Conditions

VDD/VDDQ = 1.8V±0.1V

Symbol	Parameter & Test Conditions		800MHz Max.	667MHz Max.	Unit	Notes
IDD0	**Operating Current - One Bank Active-Precharge** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING; Databus inputs are SWITCHING.		55	55	mA	1,2,3,4,5,6
IDD1	**Operating Current - One Bank Active-Read-Precharge** IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD= tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.		62	60	mA	1,2,3,4,5,6
IDD2P	**Precharge Power-Down Current** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING. (TCASE ≤ 85°C)		6	6	mA	1,2,3,4,5,6,7
IDD2N	**Precharge Standby Current** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		35	35	mA	1,2,3,4,5,6
IDD2Q	**Precharge Quiet Standby Current** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address inputs are STABLE; Data bus inputs are FLOATING.		30	30	mA	1,2,3,4,5,6
IDD3PF	**Active Power-Down Current** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address inputs are STABLE;	Fast PDN Exit MRS(12) = 0	10	10	mA	1,2,3,4,5,6
IDD3PS		Slow PDN Exit MRS(12) = 1	10	10	mA	1,2,3,4,5,6,7
IDD3N	**Active Standby Current** All banks open; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		45	45	mA	1,2,3,4,5,6

IDD4R	**Operating Burst Read Current** All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	85	80	mA	1,2,3,4,5,6
IDD4W	**Operating Burst Write Current** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	110	115	mA	1,2,3,4,5,6
IDD5B	**Burst Refresh Current** tCK = tCK(IDD); Refresh command every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.	80	80	mA	1,2,3,4,5,6
IDD6	**Self Refresh Current** CKE ≤ 0.2 V, external clock off, CLK and /CLK at 0 V; Other control and address inputs are FLOATING; Data bus inputs are FLOATING. (TCASE ≤ 85°C)	6	6	mA	1,2,3,4,5,6,7
IDD7	**Operating Bank Interleave Read Current** All bank interleaving reads, IOUT = 0mA;BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD (IDD), tRCD =tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during deselects; Data Bus inputs are SWITCHING.	120	110	mA	1,2,3,4,5,6

Note 1. VDD = 1.8 V±0.1V; VDDQ = 1.8 V±0.1V.

Note 2. IDD specifications are tested after the device is properly initialized.

Note 3. Input slew rate is specified by AC Parametric Test Condition.

Note 4. IDD parameters are specified with ODT disabled.

Note 5. Data Bus consists of DQ, DM, DQS, /DQS , RDQS, /RDQS.

Note 6. Definitions for IDD

LOW = Vin ≤ VIL (ac) (max)

HIGH = Vin ≥ VIH (ac) (min)

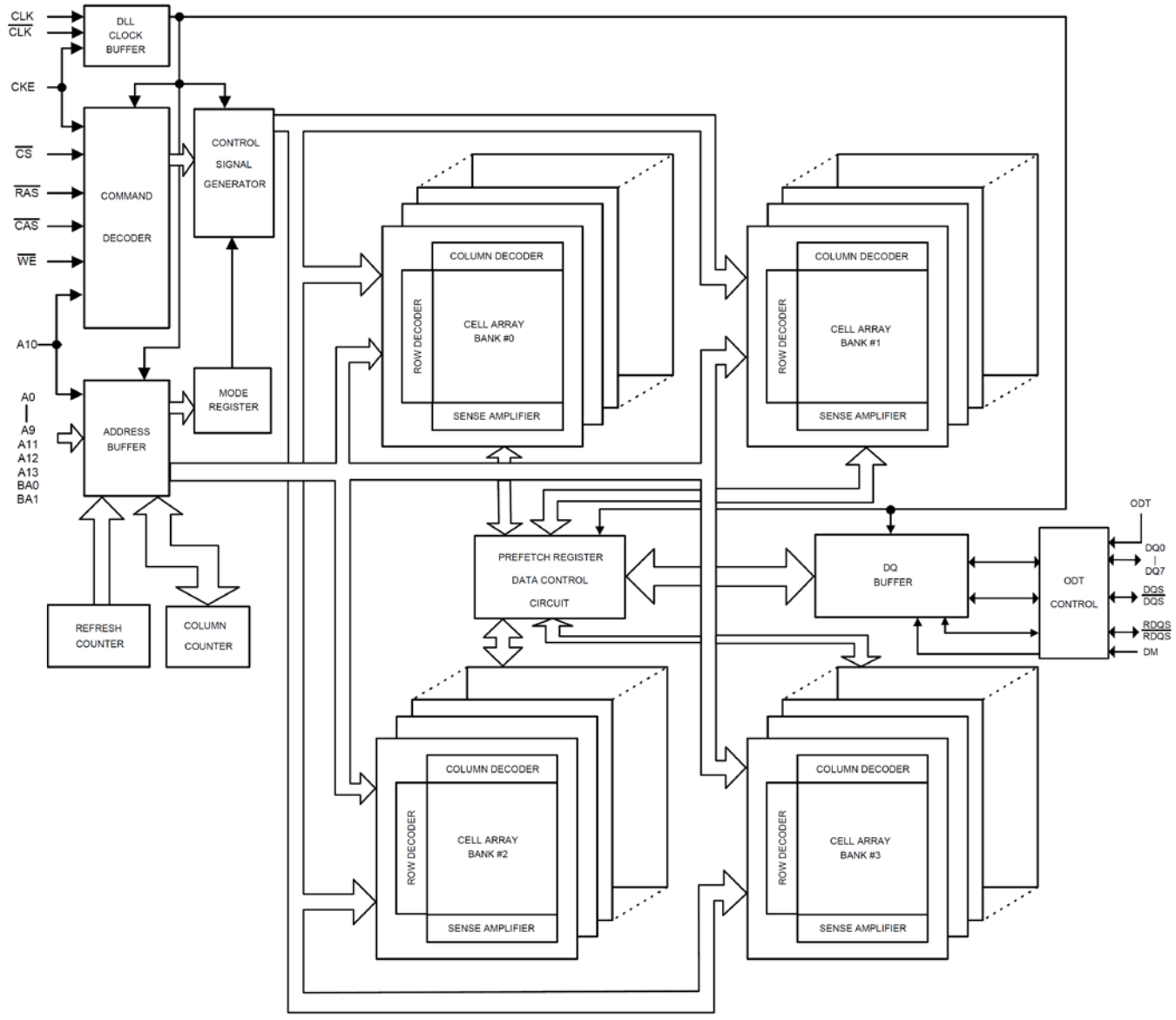
STABLE = inputs stable at a HIGH or LOW level

FLOATING = inputs at VREF = VDDQ/2

SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Note 7. The following IDD values must be derated (IDD limits increase), when TCASE ≥ 85°C IDD2P must be derated by 20 %; IDD3P(slow) must be derated by 30 % and IDD6 must be derated by 80 %. (IDD6 will increase by this amount if TCASE < 85°C and the 2X refresh option is still enabled)

Block Diagram



NOTE: The cell array configuration is 16384 * 1024 * 8

AC Operating Test Characteristics

Symbol	Speed Bin		800MHz		667MHz		Unit	Notes
	CL-nRCD-nRP		6-6-6		5-5-5			
	Parameter		Min.	Max.	Min.	Max.		
tRCD	Active to Read/Write Command Delay Time		12.5		15		nS	23
tRP	Precharge to Active Command Period		12.5		15		nS	23
tRC	Active to Ref/Active Command Period		57.5		60		nS	23
tRAS	Active to Precharge Command Period		45	70000	45	70000	nS	4,23
tRFC	Auto Refresh to Active/Auto Refresh command period		105		105		nS	5
tREFI	Average periodic refresh Interval	0℃ ≤ TCASE ≤ 85℃		7.8		7.8	μS	5
tCCD	/CAS to /CAS command delay		2		2		nCK	
tCK(avg)	Average clock period	tCK(avg) @ CL=3	5	8	5	8	nS	30,31
		tCK(avg) @ CL=4	3.75	8	3.75	8	nS	30,31
		tCK(avg) @ CL=5	2.5	8	3	8	nS	30,31
		tCK(avg) @ CL=6	2.5	8			nS	30,31
tCH(avg)	Average clock high pulse width		0.48	0.52	0.48	0.52	tCK(avg)	30,31
tCL(avg)	Average clock low pulse width		0.48	0.52	0.48	0.52	tCK(avg)	30,31
tAC	DQ output access time from CLK/ /CLK		-400	400	-450	450	pS	35
tDQSCK	DQS output access time from CLK / /CLK		-350	350	-400	400	pS	35
tDQSQ	DQS-DQ skew for DQS & associated DQ signals			200		240	pS	13
tCKE	CKE minimum high and low pulse width		3		3		nCK	7
tRRD	Active to active command period for 1KB page size		7.5		7.5		nS	8,23
tFAW	Four Activate Window for 1KB page size		35		37.5		nS	23
tWR	Write recovery time		15		15		nS	23
tDAL	Auto-precharge write recovery + precharge time		WR + tnRP		WR + tnRP		nCK	24
tWTR	Internal Write to Read command delay		7.5		7.5		nS	9,23
tRTP	Internal Read to Precharge command delay		7.5		7.5		nS	4,23
tIS (base)	Address and control input setup time		175		200		pS	10, 26, 40,42,43
tIH (base)	Address and control input hold time		250		275		pS	11, 26, 40,42,43
tIS (ref)	Address and control input setup time		375		400		pS	10,26, 40,42,43
tIH (ref)	Address and control input hold time		375		400		pS	11,26, 40,42,43
tIPW	Address and control input pulse width for each input		0.6		0.6		tCK(avg)	
tDQSS	DQS latching rising transitions to associated clock edges		-0.25	0.25	-0.25	0.25	tCK(avg)	28
tDSS	DQS falling edge to CLK setup time		0.2		0.2		tCK(avg)	28
tDSH	DQS falling edge hold time from CLK		0.2		0.2		tCK(avg)	28
tDQSH	DQS input high pulse width		0.35		0.35		tCK(avg)	
tDQSL	DQS input low pulse width		0.35		0.35		tCK(avg)	

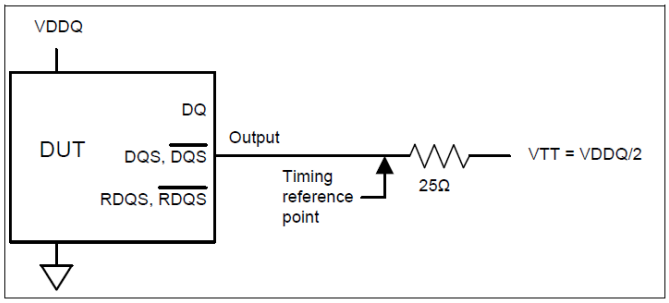
Symbol	Speed Bin	800MHz		667MHz		Unit	Notes
	CL-nRCD-nRP	6-6-6		5-5-5			
	Parameter	Min.	Max.	Min.	Max.		
tWPRE	Write preamble	0.35		0.35		tCK(avg)	
tWPST	Write postamble	0.4	0.6	0.4	0.6	tCK(avg)	12
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK(avg)	14,36
tRPST	Read postamble	0.4	0.6	0.4	0.6	tCK(avg)	14,37
tDS(base)	DQ and DM input setup time	50		100		pS	16,27,29, 41,42,44
tDH(base)	DQ and DM input hold time	125		175		pS	17,27,29, 41,42,44
tDS(ref)	DQ and DM input setup time	250		300		pS	16,27,29, 41,42,44
tDH(ref)	DQ and DM input hold time	250		300		pS	17,27,29, 41,42,44
tDIPW	DQ and DM input pulse width for each input	0.35		0.35		tCK(avg)	
tHZ	Data-out high-impedance time from CLK/ CLK		tAC,max		tAC,max	pS	15,35
tLZ(DQS)	DQS/DQS -low-impedance time from	tAC,min	tAC,max	tAC,min	tAC,max	pS	15,35
tLZ(DQ)	DQ low-impedance time from CLK/ CLK	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	pS	15,35
tHP	Clock half pulse width	Min. (tCH(abs), tCL(abs))		Min. (tCH(abs), tCL(abs))		pS	32
tQHS	Data hold skew factor		300		340	pS	33
tQH	DQ/DQS output hold time from DQS	tHP - tQHS		tHP - tQHS		pS	34
tXSNR	Exit Self Refresh to a non-Read command	tRFC + 10		tRFC + 10		nS	23
tXSRD	Exit Self Refresh to a Read command	200		200		nCK	
tXP	Exit precharge power down to any command	2		2		nCK	
tXARD	Exit active power down to Read command	2		2		nCK	18
tXARDS	Exit active power down to Read command (slow exit, lower power)	8 - AL		7 - AL		nCK	18,19
tAOND	ODT turn-on delay	2	2	2	2	nCK	20
tAON	ODT turn-on	tAC,min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	nS	20,35
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	2 tCK(avg) + tAC,max + 1	tAC,min + 2	2 tCK(avg) + tAC,max + 1	nS	
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	nCK	21,39
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	nS	21,38,39
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	nS	
tANPD	ODT to power down Entry Latency	3		3		nCK	
tAXPD	ODT Power Down Exit Latency	8		8		nCK	
tMRD	Mode Register Set command cycle time	2		2		nCK	
tMOD	MRS command to ODT update delay	0	12	0	12	nS	23
tOIT	OCD Drive mode output delay	0	12	0	12	nS	23
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK(avg)+ tIH		tIS+tCK(avg)+ tIH		nS	22

Note 1. All voltages are referenced to VSS.

Note 2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range

specified. ODT is disabled for all measurements that are not ODT-specific.

Note 3. AC timing reference load:



Note 4. This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min)have been satisfied.

Note 5. If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

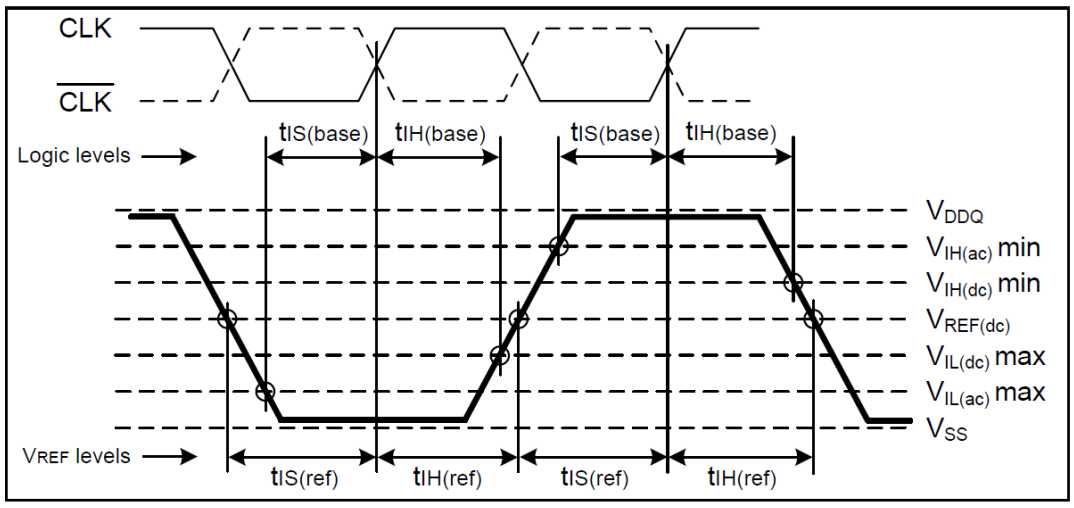
Note 6. This is an optional feature.

Note 7. tCKE min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

Note 8. A minimum of two clocks (2 * nCK) is required irrespective of operating frequency.

Note 9. tWTR is at least two clocks (2 * nCK) independent of operation frequency.

Note 10. There are two sets of values listed for Command/Address input setup time: tIS(base) and tIS(ref). The tIS(ref) value (for reference only) is equivalent to the baseline value of tIS(base) at VREF when the slew rate is 1.0 V/nS. The baseline value tIS(base) is the JEDEC defined value, referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test. If the Command/Address slew rate is not equal to 1.0 V/nS, then the baseline values must be derated by adding the values from table of tIS/tIH derating values for DDR2-667 and DDR2-800 .



Note 11. There are two sets of values listed for Command/Address input hold time: tIH(base) and tIH(ref). The tIH(ref) value (for reference only) is equivalent to the baseline value of tIH(base) at VREF when the slew rate is 1.0 V/nS. The baseline value tIH(base) is the JEDEC defined value, referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test. If the Command/Address

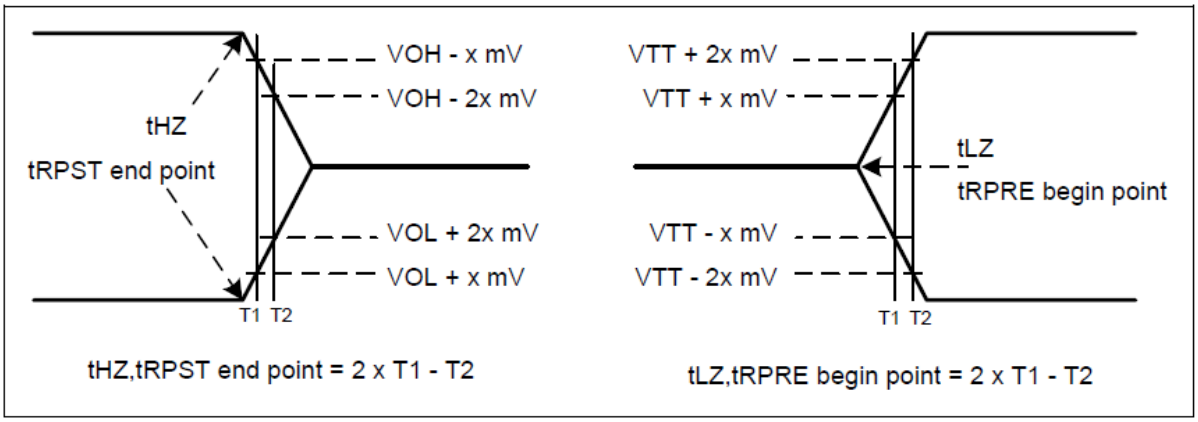
slew rate is not equal to 1.0 V/nS, then the baseline values must be derated by adding the values from table tIS/tIH derating values for DDR2-667 and DDR2-800 .

Note 12. The maximum limit for the tWPST parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrades accordingly.

Note 13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mismatch between DQS / /DQS and associated DQ in any given cycle.

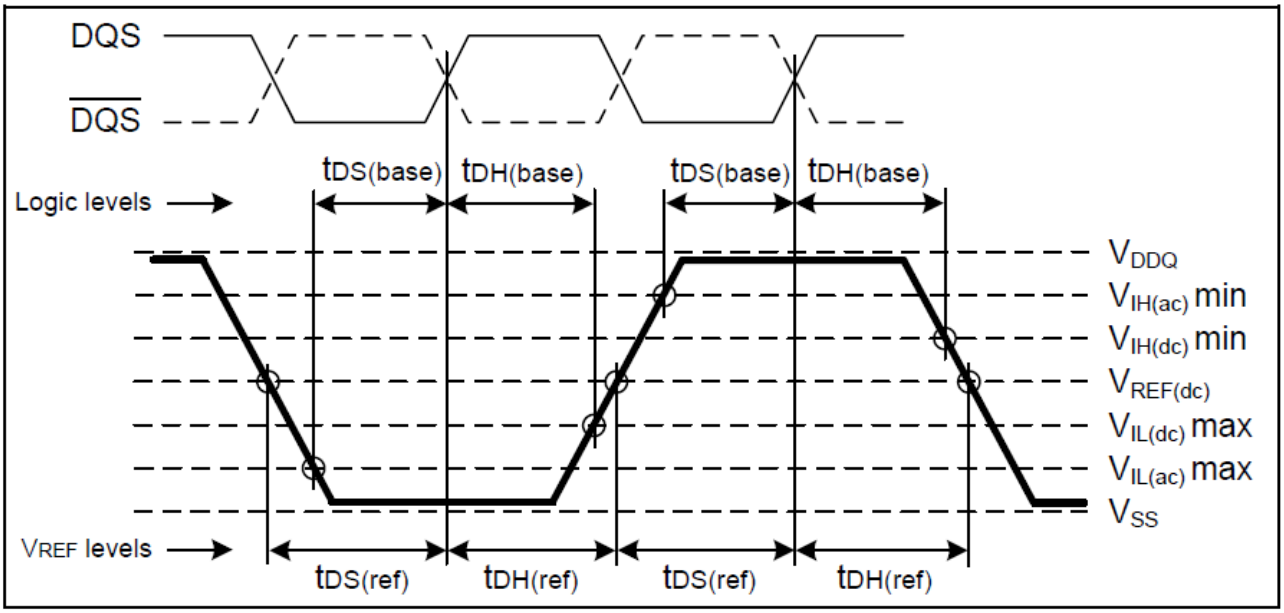
Note 14. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE).

Note 15. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ"s and tLZ(DQS) refers to tLZ of the (DQS, /DQS , RDQS, /RDQS) each treated as single-ended signal.



Note 16. Input waveform timing tDS with differential data strobe enabled MR[bit10]=0. There are two sets of values listed for DQ and DM input setup time: tDS(base) and tDS(ref). The tDS(ref) value (for reference only) is equivalent to the baseline value tDS(base) at VREF when the slew rate is 2.0 V/nS, differentially. The baseline value tDS(base) is the JEDEC defined value, referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, /DQS signals must be monotonic between VIL(dc)max and VIH(dc)min.

Note 17. Input waveform timing tDH with differential data strobe enabled MR[bit10]=0. There are two sets of values listed for DQ and DM input hold time: tDH(base) and tDH(ref). The tDH(ref) value (for reference only) is equivalent to the baseline value tDH(base) at VREF when the slew rate is 2.0 V/nS, differentially. The baseline value tDH(base) is the JEDEC defined value, referenced from the differential data strobe crosspoint to the input signal crossing at the VIH(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the VIL(dc) level for a rising signal applied to the device under test. DQS, /DQS signals must be monotonic between VIL(dc)max and VIH(dc)min.



Note 18. User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

Note 19. AL = Additive Latency.

Note 20. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from tAOND, which is interpreted differently per speed bin. For DDR2-667/800, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

Note 21. ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.
For DDR2-667/800: If tCK(avg) = 3 nS is assumed, tAOFD is 1.5 nS (= 0.5 x 3 nS) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

Note 22. The clock frequency is allowed to change during Self Refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required.

Note 23. For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
Examples:
The device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15nS, the device will support tnRP = RU{tRP / tCK(avg)} = 5,
i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15nS due to input clock jitter.

Note 24. tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [pS] / tCK(avg) [pS] }, where WR is the value programmed in the mode register set and RU stands for round up.

Note 25. New units, „tCK(avg)" and „nCK", are introduced in DDR2-667 and DDR2-800 .
Unit „tCK(avg)" represents the actual tCK(avg) of the input clock under operation.
Unit „nCK" represents one clock cycle of the input clock, counting the actual clock edges.
Examples:
For DDR2-667/800: tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be

registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

Note 26. These parameters are measured from a command/address signal (CKE, /CS , /RAS , /CAS, /WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CLK/ /CLK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Note 27. If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

Note 28. These parameters are measured from a data strobe signal (DQS, /DQS , RDQS, /RDQS) crossing to its respective clock signal (CLK/ /CLK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Note 29. These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal (DQS, /DQS , RDQS, /RDQS) crossing.

Note 30. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters'. The jitter specified is a random jitter meeting a Gaussian distribution

Symbol	Parameter	667MHz		800MHz		Unit
		Min.	Max.	Min.	Max.	
tJIT(per)	Clock period jitter	-125	125	-100	100	pS
tJIT(per,lck)	Clock period jitter during DLL locking period	-100	100	-80	80	pS
tJIT(cc)	Cycle to cycle clock period	-250	250	-200	200	pS
tJIT(cc,lck)	Cycle to cycle clock period jitter during DLL locking period	-200	200	-160	160	pS
tERR(2per)	Cumulative error across 2 cycles	-175	175	-150	150	pS
tERR(3per)	Cumulative error across 3 cycles	-225	225	-175	175	pS
tERR(4per)	Cumulative error across 4 cycles	-250	250	-200	200	pS
tERR(5per)	Cumulative error across 5 cycles	-250	250	-200	200	pS
tERR(6-10per)	Cumulative error across n cycles, n = 6 ... 10, inclusive	-350	350	-300	300	pS
tERR(11-50per)	Cumulative error across n cycles, n = 11 ... 50, inclusive	-450	450	-450	450	pS
tJIT(duty)	Duty cycle jitter	-125	125	-100	100	pS

Note 31. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Symbol	Parameter	Min.	Max.	Unit
tCK(abs)	Absolute clock period	tCK(avg),min + tJIT(per),min	tCK(avg),max+tJIT(per),max	pS
tCH(abs)	Absolute clock HIGH pulse width	tCH(avg),min x CK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	pS
tCL(abs)	Absolute clock LOW pulse width	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max +JIT(duty),max	pS

Examples: 1) For DDR2-667, tCH(abs),min = (0.48 x 3000 pS) - 125 pS = 1315 pS

Note 32. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH. The value to be used for tQH calculation is determined by the following equation;

tHP = Min (tCH(abs), tCL(abs)),

where,

tCH(abs) is the minimum of the actual instantaneous clock HIGH time;

tCL(abs) is the minimum of the actual instantaneous clock LOW time;

Note 33. tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and

2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to nchannel variation of the output drivers

Note 34. tQH = tHP – tQHS, where:

tHP is the minimum of the absolute half period of the actual input clock; and

tQHS is the specification value under the max column.

{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

Examples:

1) If the system provides tHP of 1315 pS into a DDR2-667 SDRAM, the DRAM provides tQH of 975 pS minimum.

2) If the system provides tHP of 1420 pS into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 pS minimum.

Note 35. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

Examples:

1) If the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 pS and tERR(6-10per),max = +293 pS, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 pS - 293 pS = - 693 pS and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 pS + 272 pS = + 672 pS.

Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 pS - 293 pS = - 1193 pS and tLZ(DQ),max(derated) = 450 pS + 272 pS = + 722 pS. (Caution on the min/max usage!)

Note 36. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

Examples:

1) If the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 pS and tJIT(per),max = + 93 pS, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 pS = + 2178 pS and tRPRE,max(derated) =tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 pS = + 2843 pS. (Caution on the min/max usage!)

Note 37. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

Examples:

1) If the measured jitter into a DDR2-667 SDRAM has tJIT(duty),min = - 72 pS and tJIT(duty),max = + 93 pS, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 pS = + 928 pS and tRPST,max(derated) =tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 pS = + 1592 pS. (Caution on the min/max usage!)

Note 38. When the device is operated with input clock jitter, this parameter needs to be derated by { -tJIT(duty),max – t ERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are

relative to the SDRAM input clock.)

Examples:

1) If the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 pS, tERR(6-10per),max = + 293 pS, tJIT(duty),min = - 106 pS and tJIT(duty),max = + 94 pS, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max- tERR(6-10per),max } = - 450 pS + { - 94 pS - 293 pS} = - 837 pS and tAOF,max(derated) = tAOF,max + { -tJIT(duty),min - tERR(6-10per),min } = 1050 pS + { 106 pS + 272 pS } = + 1428 pS. (Caution on the min/max usage!)

Note 39. For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5.

Example:

If an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)

tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)

or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))

tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))

where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However

tAC values used in the equations shown above are from the timing parameter table and are not derated.

Thus the final derated values for tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }

tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }

Note 40. Timings are specified with command/address input slew rate of 1.0 V/nS.

Note 41. Timings are specified with DQs and DM input slew rate of 1.0V/nS.

Note 42. Timings are specified with CLK/ /CLK differential slew rate of 2.0 V/nS. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/nS in differential strobe mode.

Note 43. tIS and tIH (input setup and hold) derating.

Command/ Address Slew Rate (V/nS)	ΔtIS and ΔtIH Derating Values for DDR2-667 and DDR2-800						
	CLK/ /CLK Differential Slew Rate						
	2.0		1.5		1.0		Unit
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+150	+94	+180	+124	+210	+154	pS
3.5	+143	+89	+173	+119	+203	+149	pS
3.0	+133	+83	+163	+113	+193	+143	pS
2.5	+120	+75	+150	+105	+180	+135	pS
2.0	+100	+45	+130	+75	+160	+105	pS
1.5	+67	+21	+97	+51	+127	+81	pS
1.0	0	0	+30	+30	+60	+60	pS
0.9	-5	-14	+25	+16	+55	+46	pS
0.8	-13	-31	+17	-1	+47	+29	pS
0.7	-22	-54	+8	-24	+38	+6	pS
0.6	-34	-83	-4	-53	+26	-23	pS
0.5	-60	-125	-30	-95	0	-65	pS
0.4	-100	-188	-70	-158	-40	-128	pS
0.3	-168	-292	-138	-262	-108	-232	pS
0.2	-200	-375	-170	-345	-140	-315	pS
0.2	-325	-500	-295	-470	-265	-440	pS
0.15	-517	-708	-487	-678	-457	-648	pS
0.1	-100	-1125	-970	-1095	-940	-1065	pS

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded „VREF(dc) to AC region", use nominal slew rate for derating value.

If the actual signal is later than the nominal slew rate line anywhere between shaded „VREF(dc) to AC region", the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded „DC to VREF(dc) region", use nominal slew rate for derating value.

If the actual signal is earlier than the nominal slew rate line anywhere between shaded „DC to VREF(dc) region", the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in above tIS/tIH derating values for DDR2-667 and DDR2-800 table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

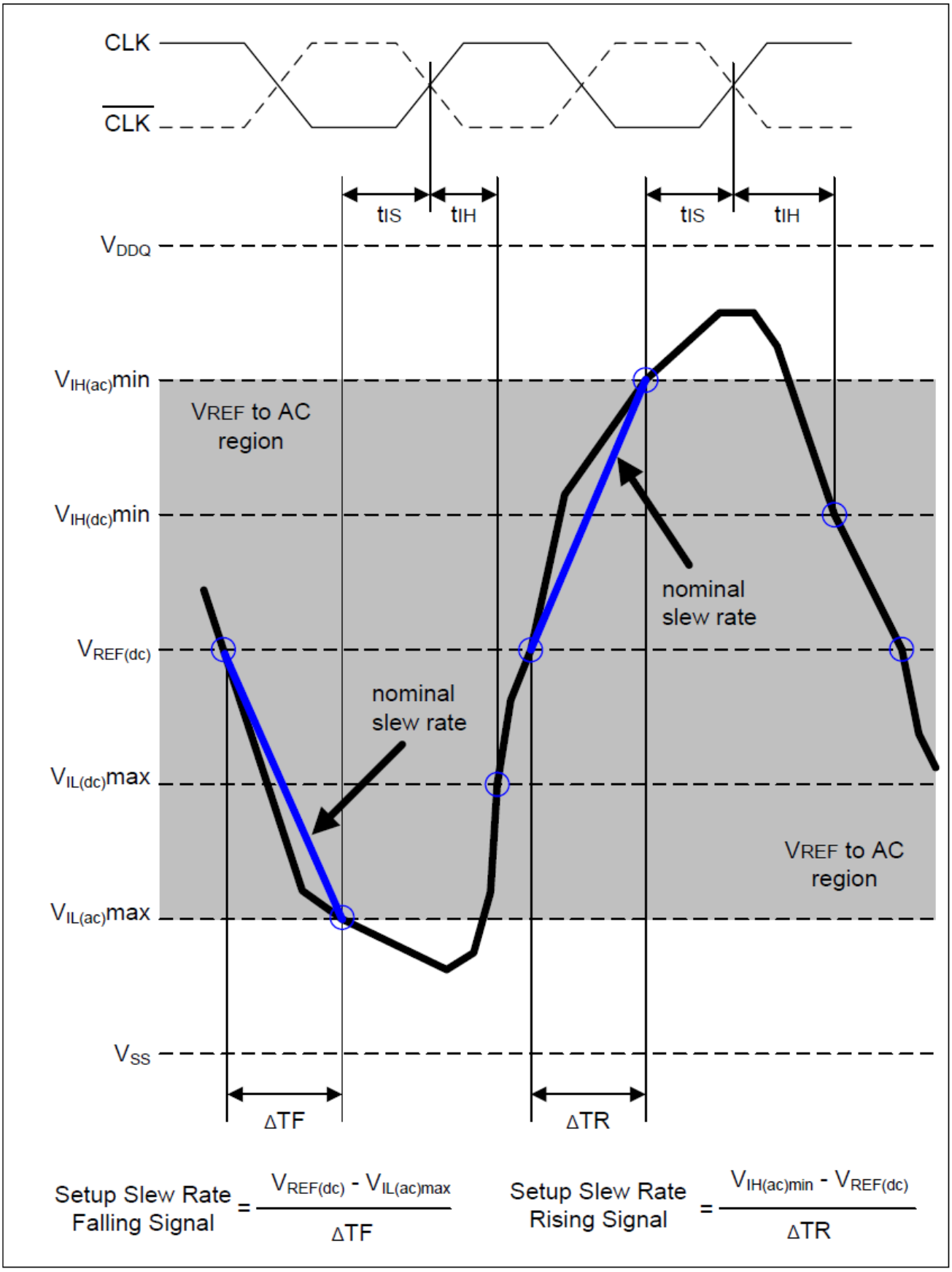


Illustration of nominal slew rate for tIS

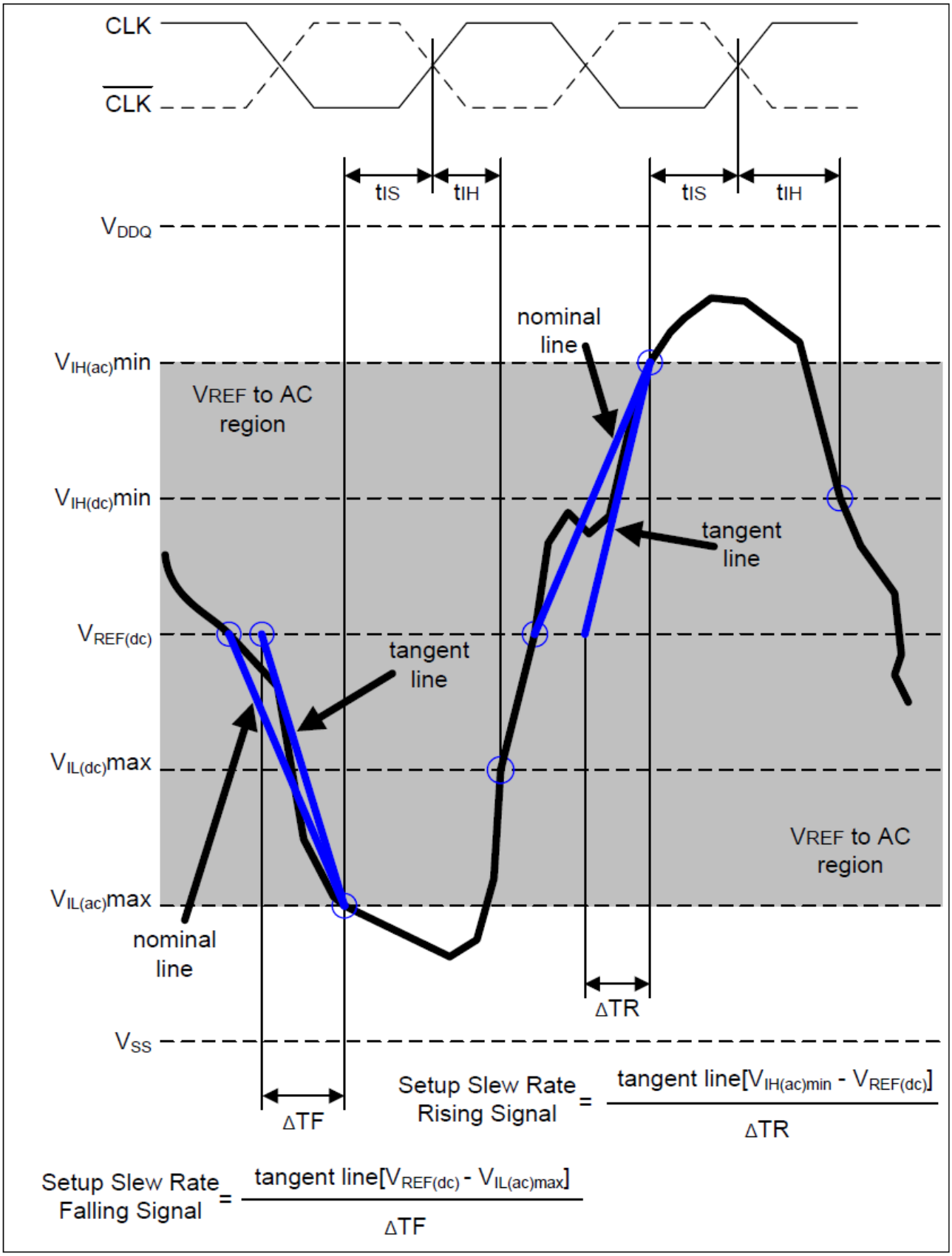


Illustration of tangent line for tIS

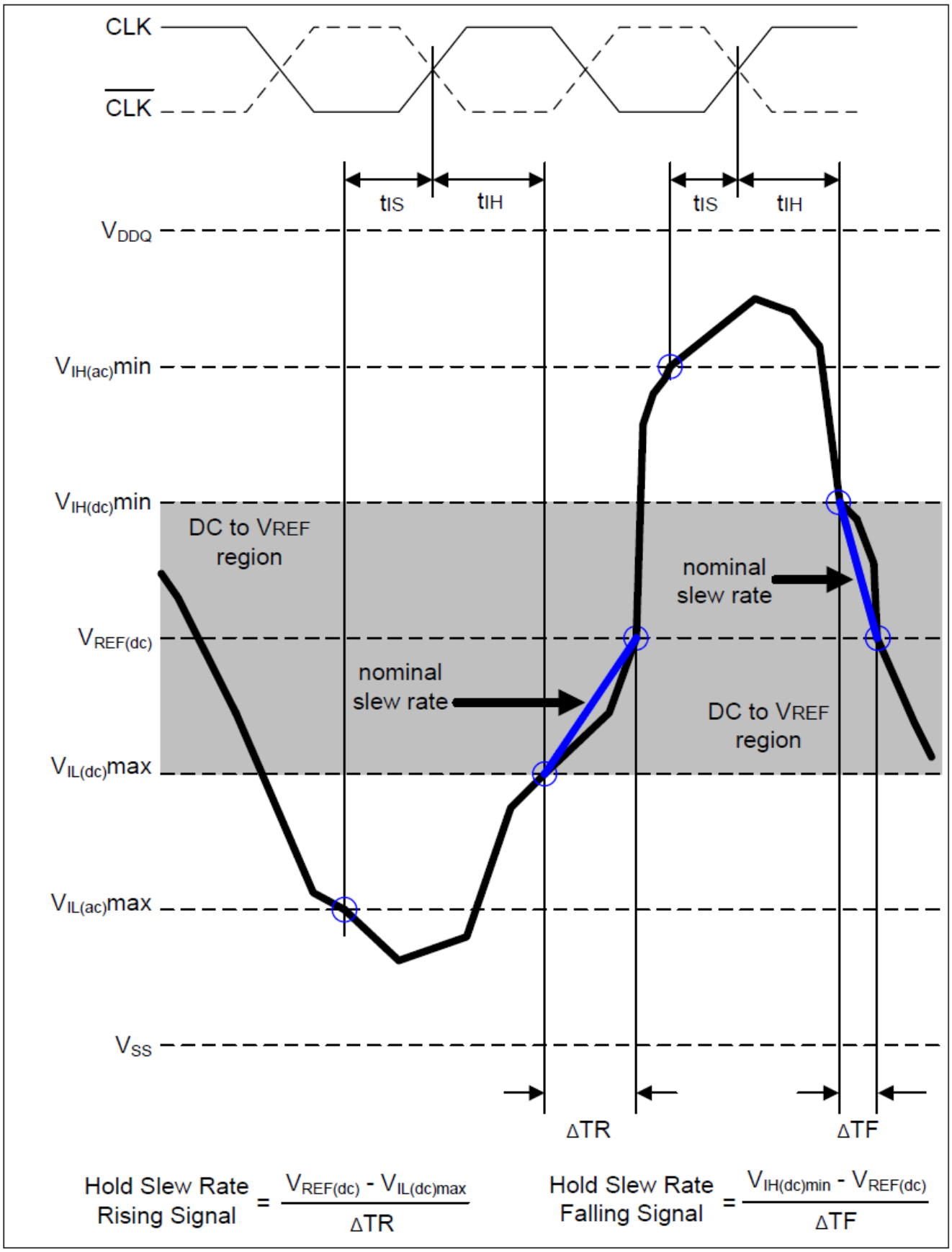


Illustration of nominal slew rate for tIH

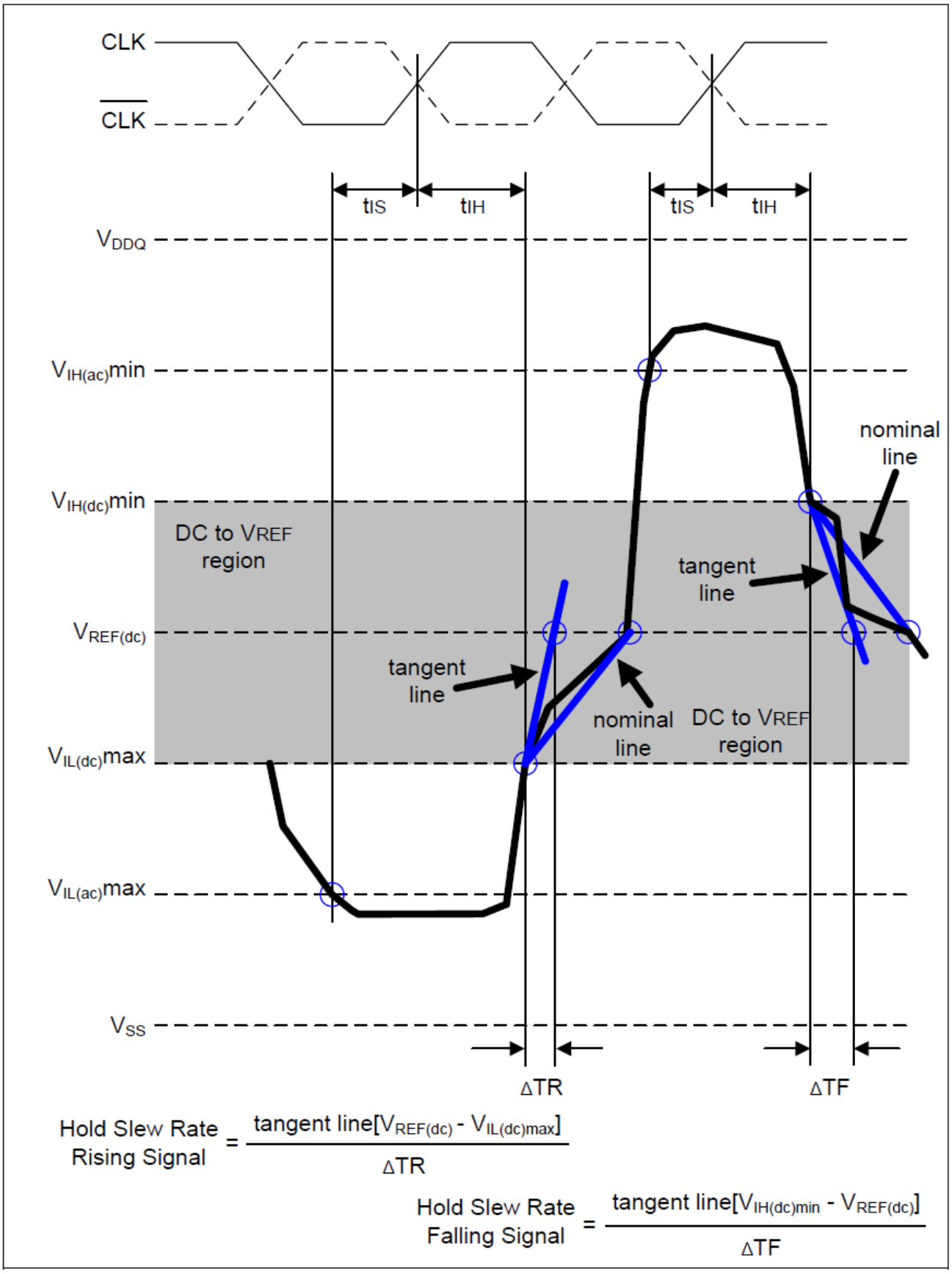


Illustration of tangent line for tIH

Note 44. Data setup and hold time derating.

DQ Slew Rate (V/nS)	ΔtDS, ΔtDH Derating Values for DDR2-667 and DDR2-800 (All units in „pS"; the note applies to the entire table)																	
	DQS/ /DQSDifferential Slew Rate																	
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS		0.8 V/nS	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded „VREF(dc) to AC region", use nominal slew rate for derating value.

If the actual signal is later than the nominal slew rate line anywhere between shaded VREF(dc) to AC region , the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc) max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded „DC level to VREF(dc) region", use nominal slew rate for derating value.

If the actual signal is earlier than the nominal slew rate line anywhere between shaded DC to VREF(dc) region, the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in above DDR2-667 and DDR2-800 tDS/tDH derating with differential data strobe table, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization

Note 45. Slew Rate Measurement Levels:

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.

For differential signals (e.g. DQS - /DQS) output slew rate is measured between DQS - /DQS = - 500 mV and DQS – /DQS = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

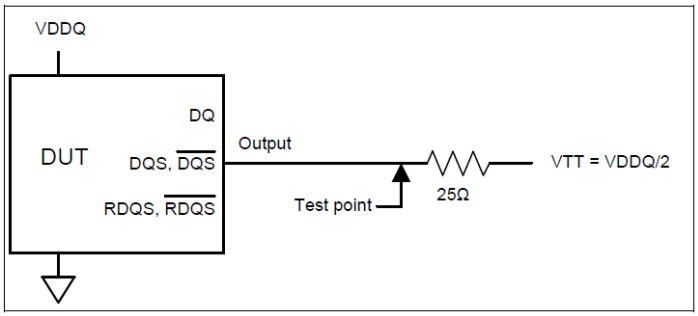
b) Input slew rate for single ended signals is measured from VREF(dc) to VIH(ac),min for rising edges and from VREF(dc) to VIL(ac),max for falling edges.

For differential signals (e.g. CLK - /CLK) slew rate for rising edges is measured from CLK - /CLK = - 250 mV to CLK - /CLK = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CLK and the input voltage on /CLK , or between DQS and /DQS for differential strobe.

Note 46. DDR2 SDRAM output slew rate test load:

Output slew rate is characterized under the test conditions as shown in below figure.



Note 47. Differential data strobe:

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the cross point of DQS and its complement, /DQS . This distinction in timing methods is guaranteed by design and characterization.

Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, /DQS , must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.

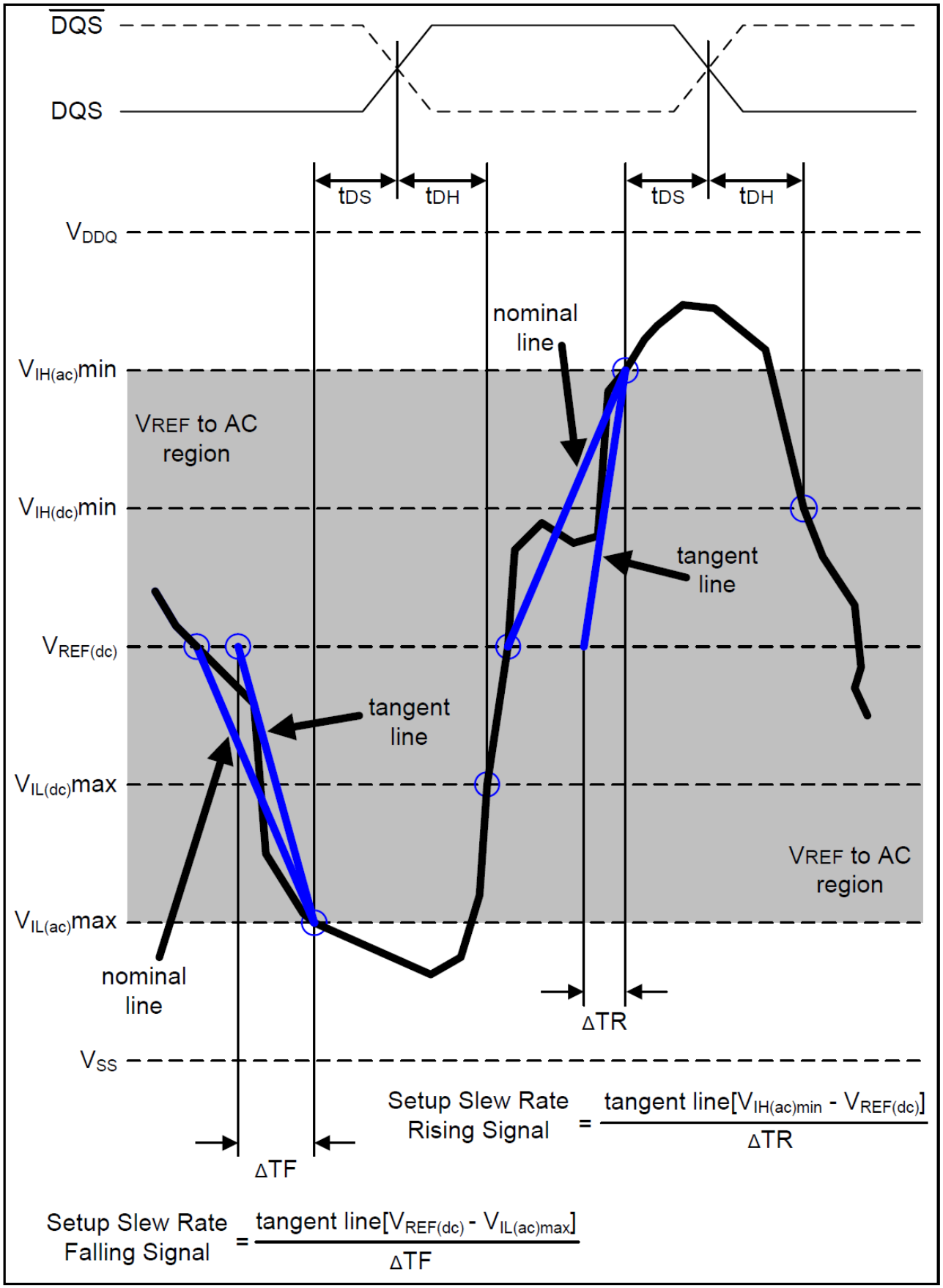


Illustration of nominal slew rate for tDS (differential DQS,/DQS)

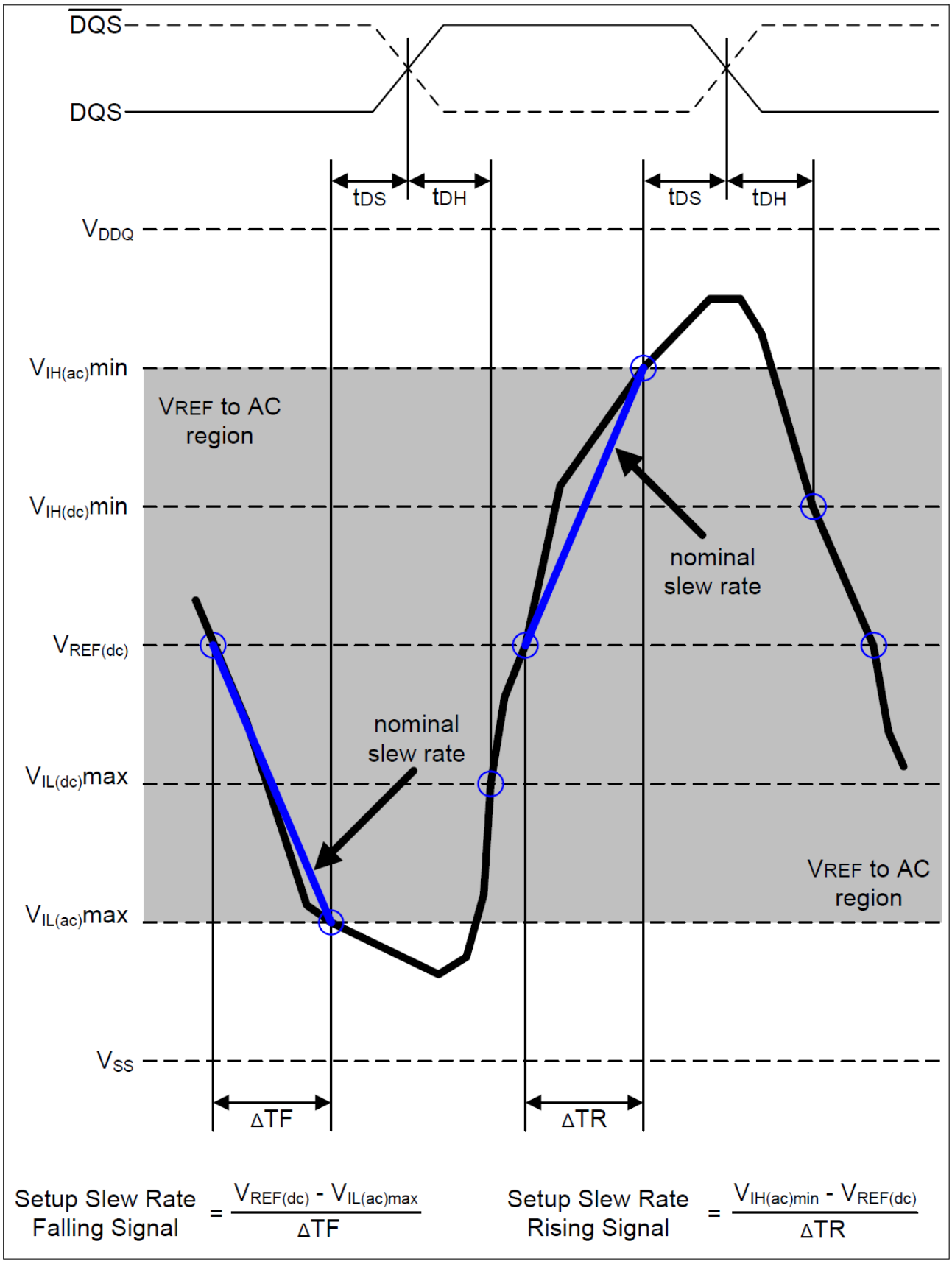


Illustration of tangent line for tDS (differential DQS,/DQS)

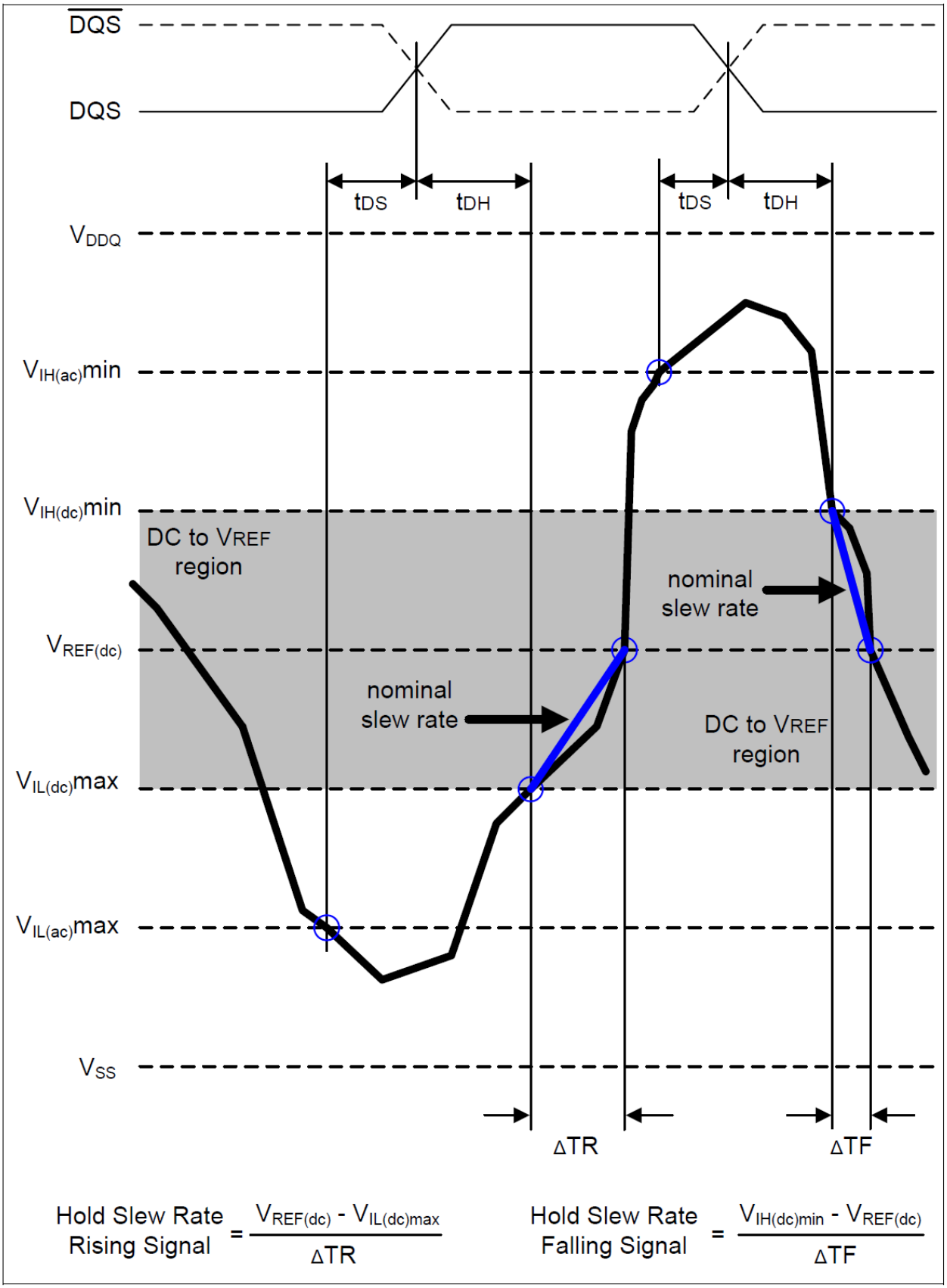


Illustration of nominal slew rate for tDH (differential DQS,/DQS)

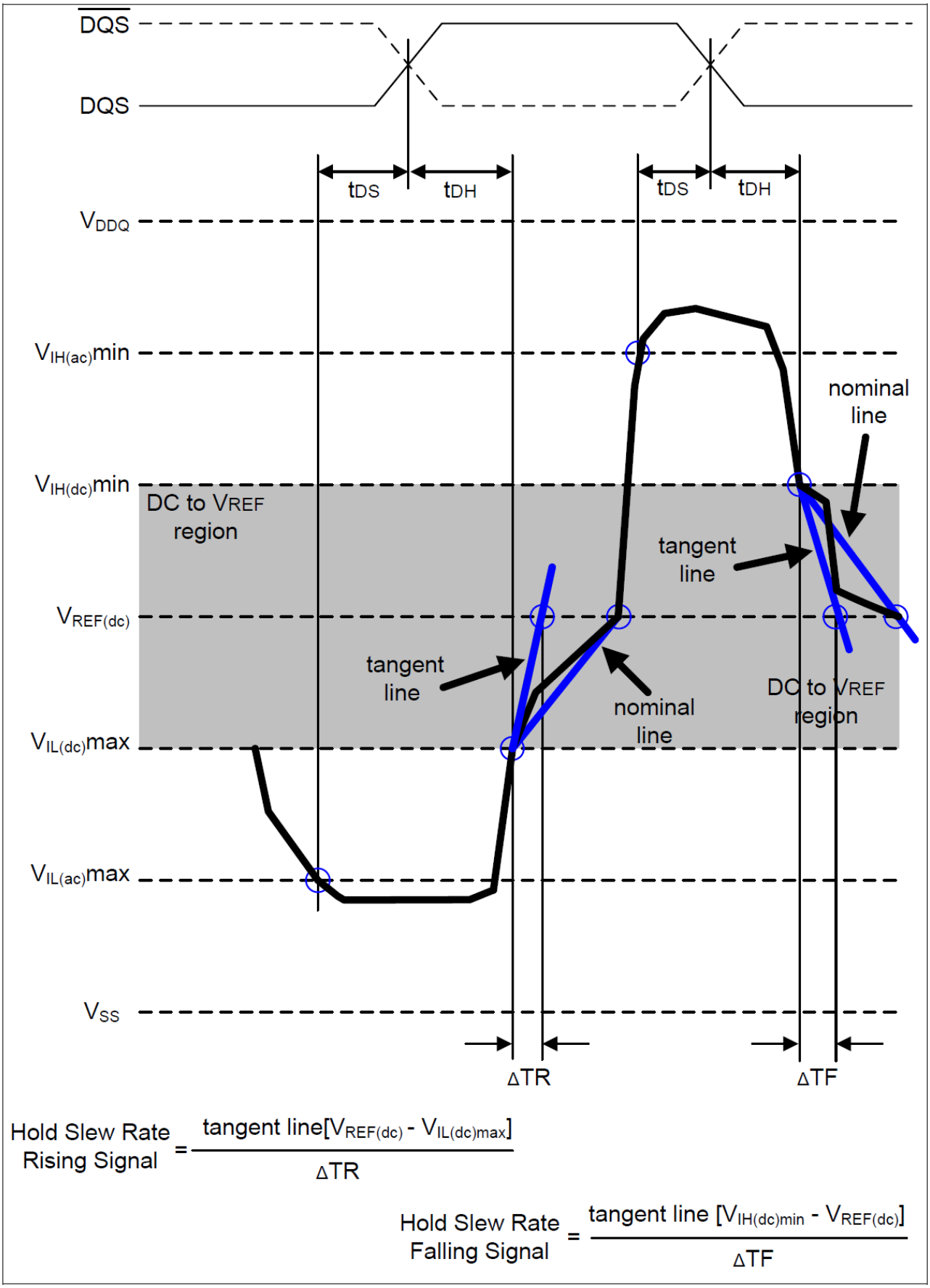
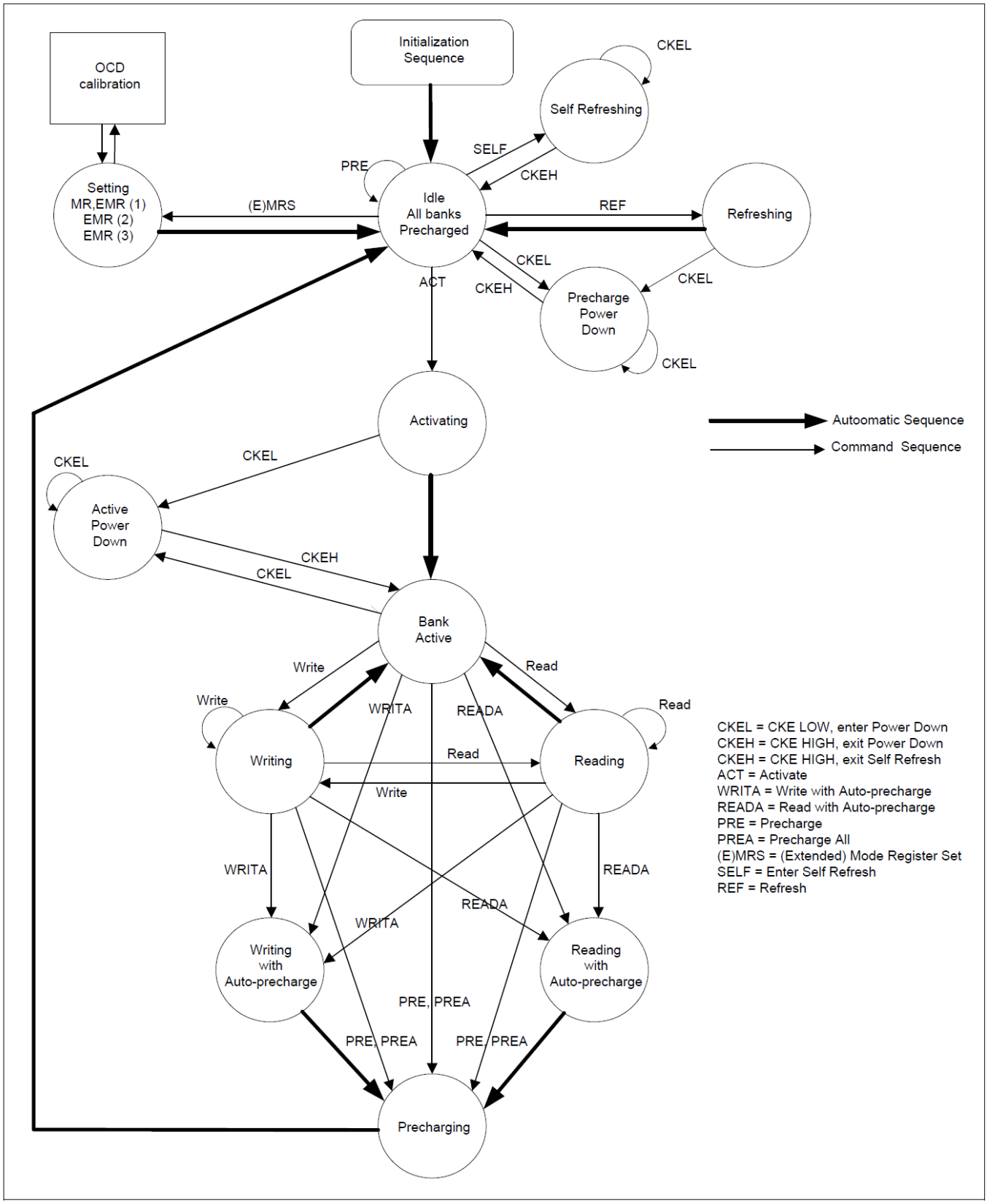


Illustration tangent line for tDH (differential DQS,/DQS)

Simplified State Diagram



Command Truth Table

Command	CKE		BA1 BA0	A13 A12 A11	A10	A9-A0	/CS	/RAS	/CAS	/WE	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	BA	Row Address			L	L	H	H	1,2
Single Bank Precharge	H	H	BA	X	L	X	L	L	H	L	1,2
Precharge All Banks	H	H	X	X	H	X	L	L	H	L	1
Write	H	H	BA	Column	L	Column	L	H	L	L	1,2,3
Write with Auto-precharge	H	H	BA	Column	H	Column	L	H	L	L	1,2,3
Read	H	H	BA	Column	L	Column	L	H	L	H	1,2,3
Read with Auto-precharge	H	H	BA	Column	H	Column	L	H	L	H	1,2,3
(Extended) Mode Register Set	H	H	BA	OP Code			L	L	L	L	1,2
No Operation	H	X	X	X	X	X	L	H	H	H	1
Device Deselect	H	X	X	X	X	X	H	X	X	X	1
Refresh	H	H	X	X	X	X	L	L	L	H	1
Self Refresh Entry	H	L	X	X	X	X	L	L	L	H	1,4
Self Refresh Exit	L	H	X	X	X	X	H	X	X	X	1,4,5
							L	H	H	H	
Power Down Mode Entry	H	L	X	X	X	X	H	X	X	X	1,6
							L	H	H	H	
Power Down Mode Exit	L	H	X	X	X	X	H	X	X	X	1,6
							L	H	H	H	

Note 1. All DDR2 SDRAM commands are defined by states of CS , RAS , CAS, WE and CKE at the rising edge of the clock.

Note 2. Bank addresses BA [1:0] determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Note 3. Burst reads or writes at BL = 4 can not be terminated or interrupted.

Note 4. VREF must be maintained during Self Refresh operation.

Note 5. Self Refresh Exit is asynchronous.

Note 6. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements.

CKE Truth Table

Current State	CKE		Command /RAS, /CAS, /WE, /CS	Action	Notes
	Previous Cycle	Current Cycle			
Power Down	L	L	X	Maintain Power Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Power Down	11, 15,16
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4, 8, 10, 11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Down Entry	4, 8, 10, 11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11, 13
	H	H	Refer to the Command Truth Table		7

Note 1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.

Note 2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.

Note 3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).

Note 4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note 5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.

Note 6. Self Refresh mode can only be entered from the All Banks Idle state.

Note 7. Must be a legal command as defined in the Command Truth Table.

Note 8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.

Note 9. Valid commands for Self Refresh Exit are NOP and DESELECT only.

Note 10. Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress.

Note 11. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

Note 12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note 13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements.

Note 14. CKE must be maintained HIGH while the SDRAM is in OCD calibration mode.

Note 15. “X” means “don"t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMR (1)).

Note 16. VREF must be maintained during Self Refresh operation

Operative Command Table

Current State	/CS	/RAS	/CAS	/WE	Addr.	Command	Action	Notes
Idle	H	X	X	X	X	DESL	NOP or Power down	
	L	H	H	H	X	NOP	NOP or Power down	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA/RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PREA	Precharge/ Precharge all banks	
	L	L	L	H	X	AREF/SELF	Auto Refresh or Self Refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode/Extended register accessing	
Banks Active	H	X	X	X	X	DSL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	Precharge/ Precharge all banks	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	Burst interrupt	1,3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Burst interrupt	1,3
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Current State	/CS	/RAS	/CAS	/WE	Addr.	Command	Action	Notes
Read with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharge	H	X	X	X	X	DSL	NOP-> Idle after tRP	
	L	H	H	H	X	NOP	NOP-> Idle after tRP	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	NOP-> Idle after tRP	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row Activating	H	X	X	X	X	DSL	NOP-> Row active after tRCD	
	L	H	H	H	X	NOP	NOP-> Row active after tRCD	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Current State	/CS	/RAS	/CAS	/WE	Addr.	Command	Action	Notes
Write Recovering	H	X	X	X	X	DSL	NOP-> Bank active after tWR	
	L	H	H	H	X	NOP	NOP-> Bank active after tWR	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
WriteRecovering with Auto-precharge	H	X	X	X	X	DSL	NOP-> Precharge after tWR	
	L	H	H	H	X	NOP	NOP-> Precharge after tWR	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	NOP-> Idle after tRC	
	L	H	H	H	X	NOP	NOP-> Idle after tRC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DSL	NOP-> Idle after tMRD	
	L	H	H	H	X	NOP	NOP-> Idle after tMRD	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Note 1. This command may be issued for other banks, depending on the state of the banks.

Note 2. All banks must be in "IDLE".

Note 3. Read or Write burst interruption is prohibited for burst length of 4 and only allowed for burst length of 8. Burst read/write can only be interrupted by another read/write with 4 bit burst boundary. Any other case of read/write interrupt is not allowed. Remark: H = High level, L = Low level, X = High or Low level (Don"t Care), V = Valid data.

Power-up and Initialization Sequence

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for Power-up and Initialization.

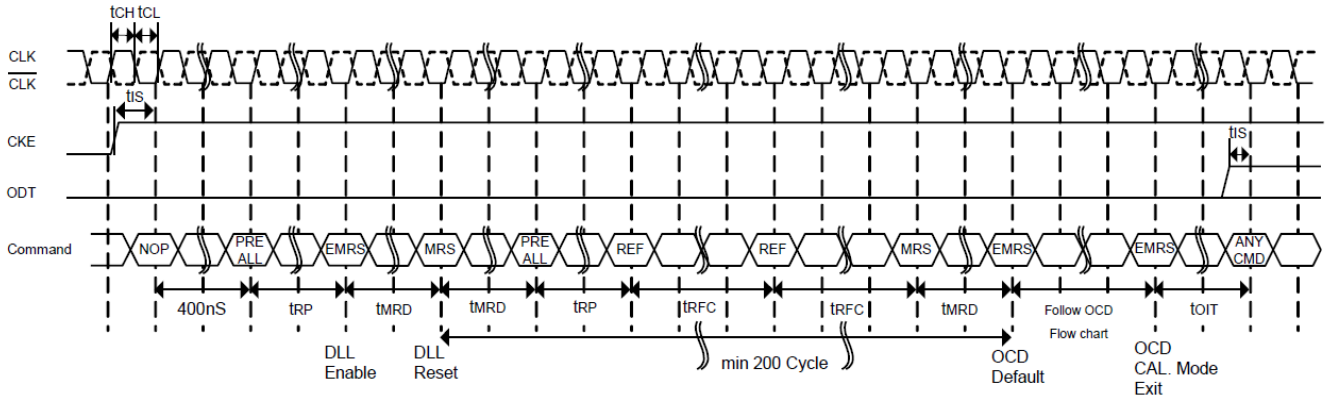
1. Apply power and attempt to maintain CKE below 0.2 × V_{DDQ} and ODT*1 at a LOW state (all other inputs may be undefined.) Either one of the following sequence is required for Power-up.
   A. The V_{DD} voltage ramp time must be no greater than 200 mS from when V_{DD} ramps from 300 mV to V_{DD} min; and during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3$ volts.
      - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V max
      - V_{REF}*2 tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times
   B. Voltage levels at I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete.
      - Apply V_{DD}/V_{DDL}*3 before or at the same time as V_{DDQ}
      - Apply V_{DDQ}*4 before or at the same time as V_{TT}
      - V_{REF}*2 tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times
2. Start Clock and maintain stable condition for 200 µS (min.).
3. After stable power and clock (CLK,/CLK), apply NOP or Deselect and take CKE HIGH.
4. Wait minimum of 400 nS then issue precharge all command. NOP or Deselect applied during 400 nS period.
5. Issue an EMRS command to EMR (2). (To issue EMRS command to EMR (2), provide LOW to BA0 and BA2, HIGH to BA1.)
6. Issue an EMRS command to EMR (3). (To issue EMRS command to EMR (3), provide LOW to BA2, HIGH to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1-BA2 and A13. And A9=A8=A7=LOW must be used when issuing this command.)
8. Issue a Mode Register Set command for DLL reset. (To issue DLL Reset command, provide HIGH to A8 and LOW to BA0-BA2 and A13.)
9. Issue a precharge all command.
10. Issue 2 or more Auto Refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
13. The DDR2 SDRAM is now ready for normal operation.

Note 1. To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.

Note 2. VREF must be within ± 300 mV with respect to VDDQ/2 during supply ramp time.

Note 3. VDD/VDDL voltage ramp time must be no greater than 200 mS from when VDD ramps from 300 mV to VDD min.

Note 4. The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500 mS.



Initialization sequence after power-up

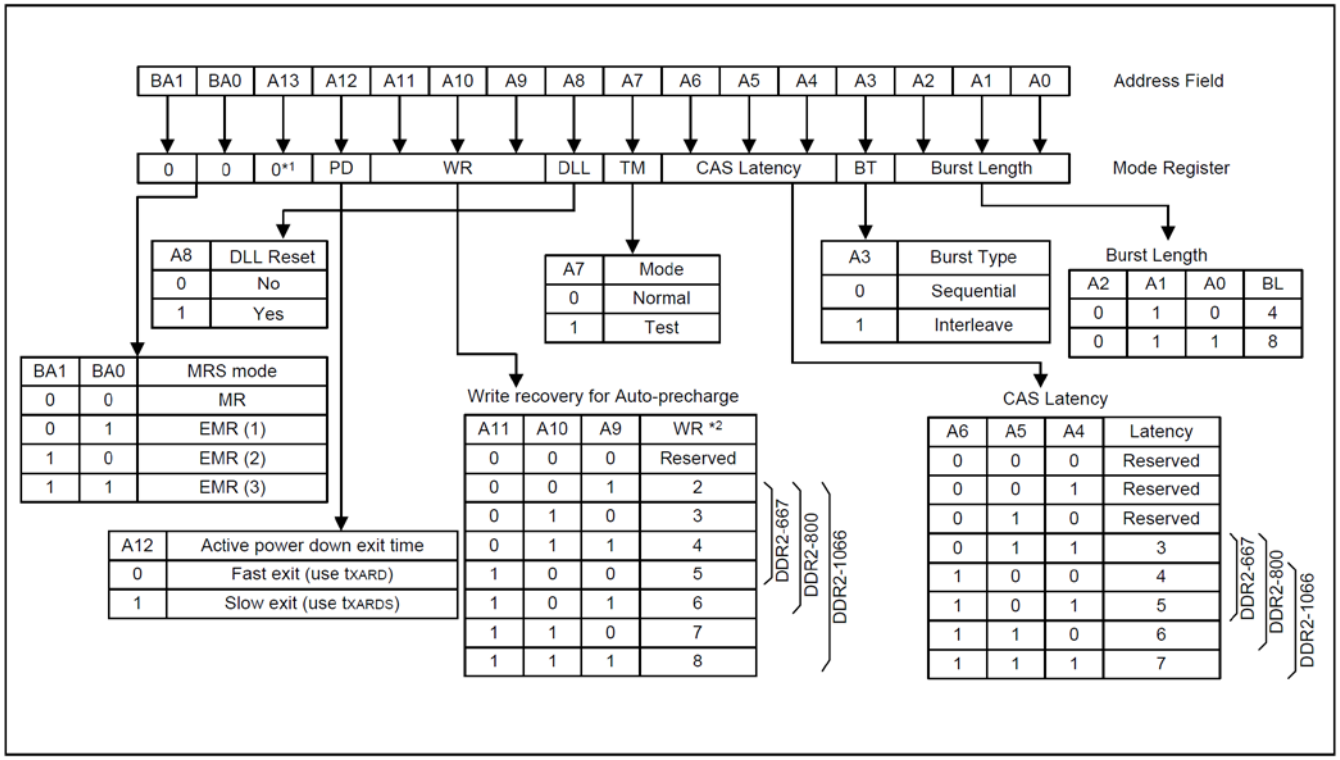
Mode Register Definition

Mode Register Set Command (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs CAS Latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value in the Mode Register after power-up is not defined, therefore the Mode Register must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

The mode register is divided into various fields depending on functionality. Burst length is defined by A[2:0] with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS Latency is defined by A[6:4]. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A[11:9]. Refer to the table for specific codes.



Mode Register Set (MRS)

Note 1. A13 reserved for future use and must be set to "0" when programming the MR.

Note 2. WR (write recovery for Auto-precharge) min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[nS] / tCK(avg)[nS] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Burst Type (A3)

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x00	0123	0123
	x01	1230	1032
	x10	2301	2301
	x11	3012	3210
8	000	01234567	01234567
	001	12305674	10325476
	010	23016745	23016745
	011	30127456	32107654
	100	45670123	45670123
	101	56741230	54761032
	110	67452301	67452301
	111	74563012	76543210

Write Recovery

WR (Write Recovery) is for Writes with Auto-Precharge only and defines the time when the device startspre-charge internally. WR must be programmed to match the minimum requirement for the analogue t_{WR} timing.

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW, along with NOP or Deselect command. CKE is not allowed to go LOW while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go LOW while any other operation such as row activation, Precharge or Auto-precharge or Auto Refresh is in progress, but power down I_{DD} specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

Extend Mode Register EMR1

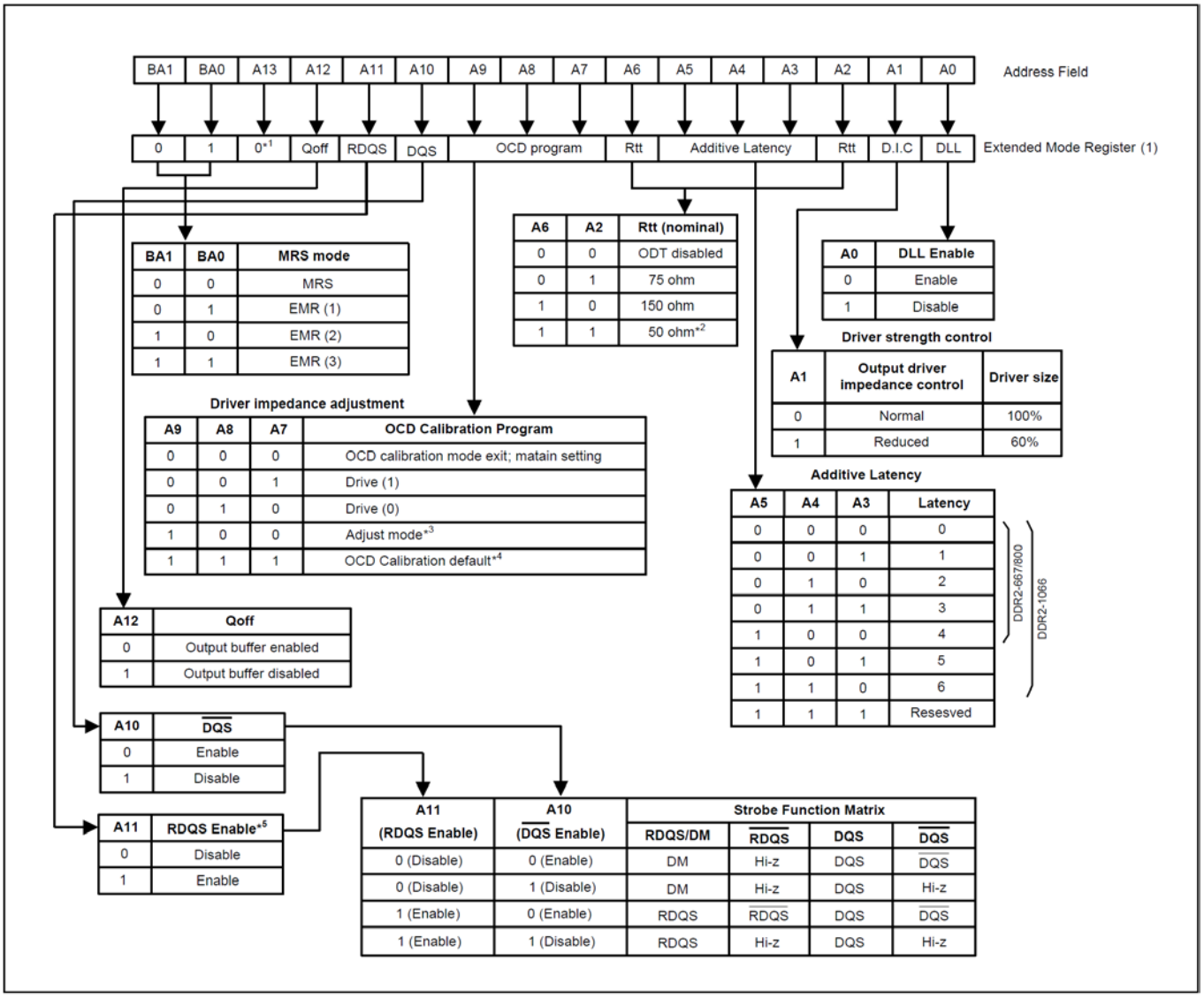
The extended mode register (1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, /DQS disable, OCD program. The default value of the extended mode register (1) is not defined, therefore the extended mode register (1) must be programmed during initialization for proper operation. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (1). Extended mode register (1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A[5:3] determines the additive latency, A[9:7] are used for OCD control, A10 is used for /DQS disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMRS(1) is set to (0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled and reset upon exit of Self Refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.



EMR (1)

Note 1. A13 reserved for future use and must be set to "0" when programming the EMR (1).

Note 2. Optional for DDR2-667, mandatory for DDR2-800 .

Note 3. When Adjust mode is issued, AL from previously set value must be applied.

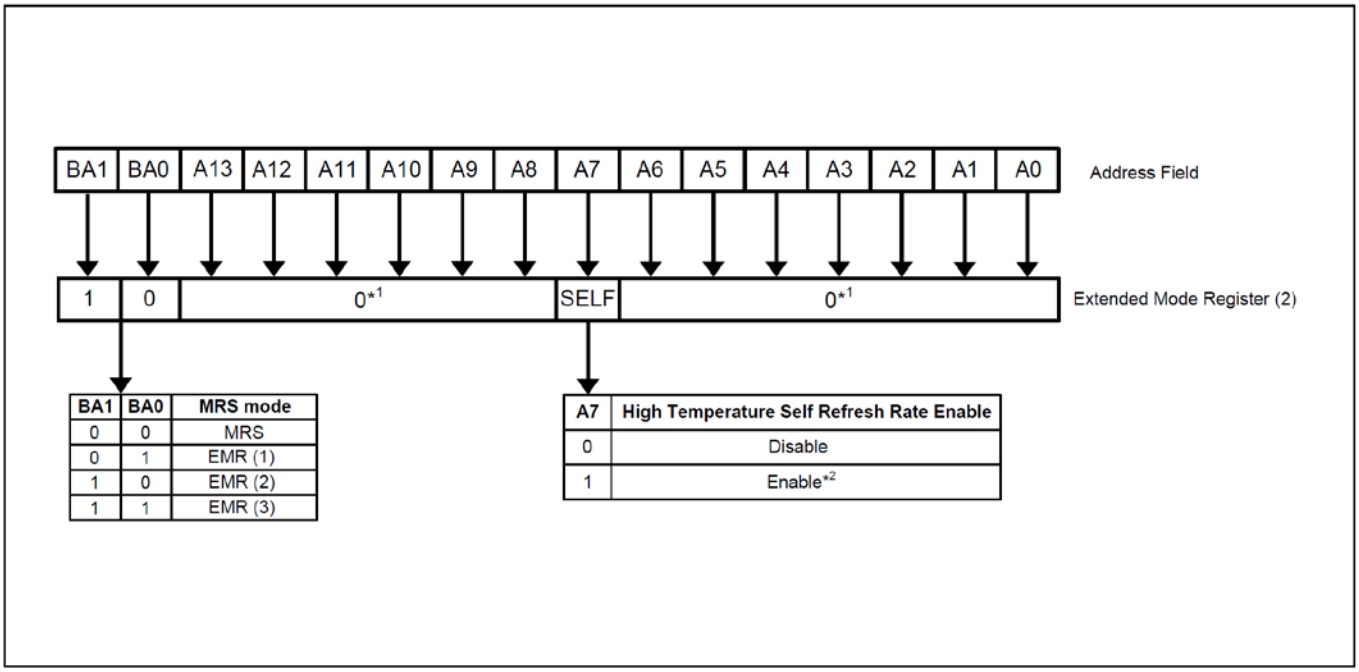
Note 4. After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000.

Note 5. If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don"t care for writes.

Extend Mode Register EMR2

The extended mode register (2) controls refresh related features. The default value of the extended mode register (2) is not defined, therefore the extended mode register (2) must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.



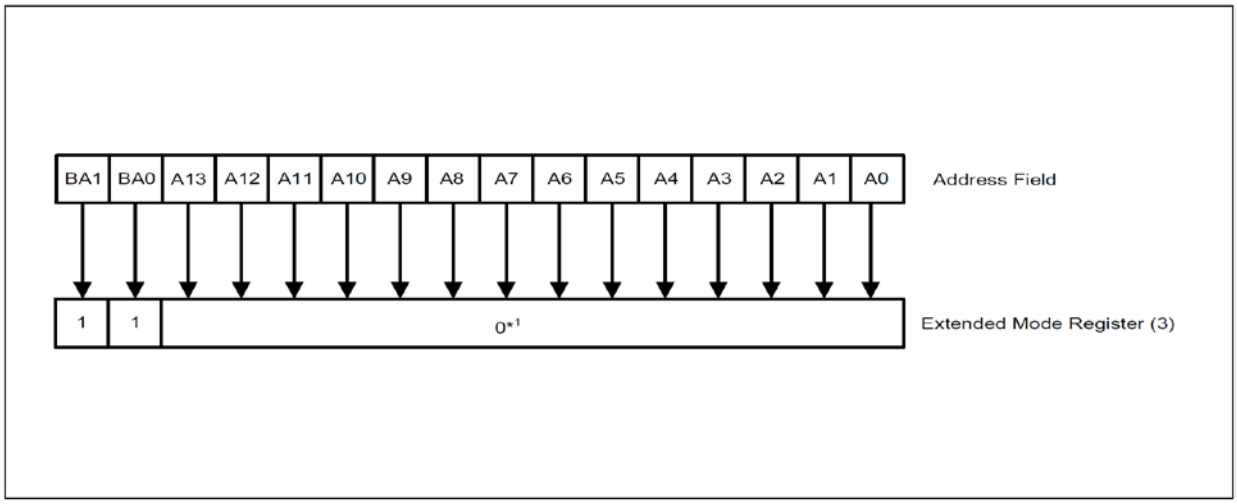
EMR (2)

Note 1. A0-A6, A8-A13 are reserved for future use and must be set to "0" when programming the EMR (2).

Note 2. When DRAM is operated at 85 °C < TCASE ≤ 95 °C the extended Self Refresh rate must be enabled by setting bit A7 to "1" before the Self Refresh mode can be entered.

Extend Mode Register EMR3

No function is defined in extended mode register (3). The default value of the EMR (3) is not defined, therefore the EMR (3) must be programmed during initialization for proper operation.



EMR (3)

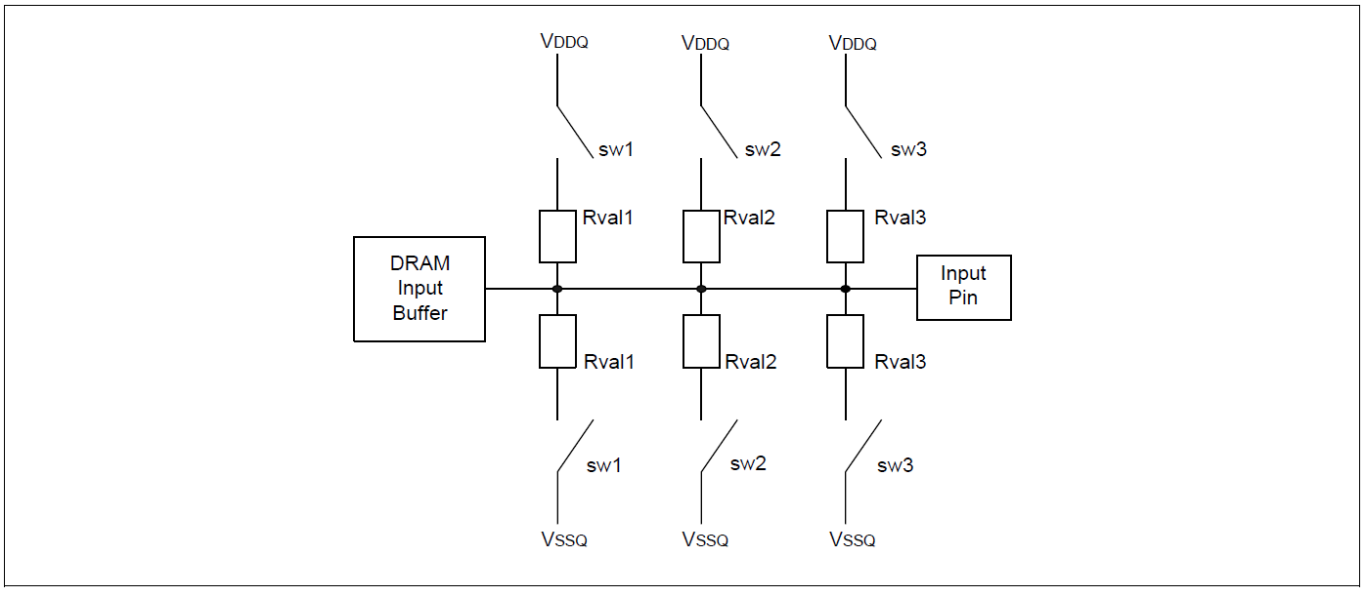
Note. All bits in EMR (3) except BA0 and BA1 are reserved for future use and must be set to "0" when programming the EMR(3).

On-Die Termination (ODT)

On-Die Termination (ODT) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, DQS/ /DQS , RDQS/ /RDQS, and DM signal via the ODT control pin.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self Refresh mode.



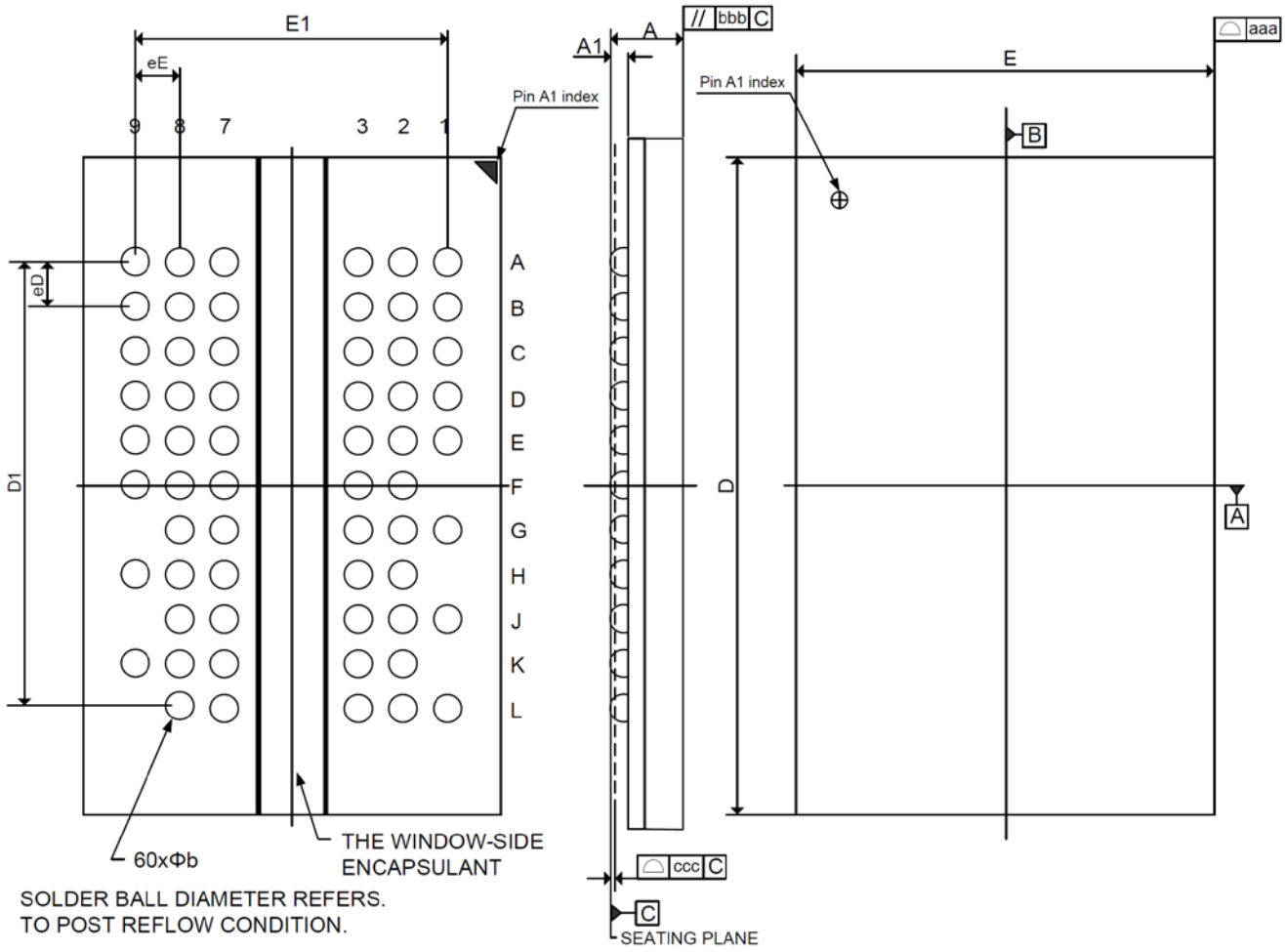
Functional Representation of ODT

Note. Switch (sw1, sw2, sw3) is enabled by ODT pin.

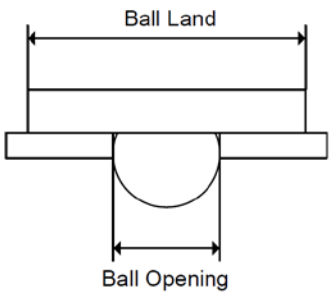
Selection among sw1, sw2, and sw3 is determined by “Rtt (nominal)” in EMR (1).

Termination included on all DQs, DM, DQS, /DQS , RDQS, and /RDQS pins.

Package Description: 60Ball-FBGA



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.25	---	0.40
b	0.40	0.45	0.50
D	12.40	12.50	12.60
E	7.90	8.00	8.10
D1	8.00 BSC.		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10



Note: 1. Ball land : 0.5mm
2. Ball opening : 0.4mm
3. PCB Ball land suggested ≤ 0.4mm

Revision History

Revision No.	History	Draft Date	Editor	Remark
0.1	Initial Release.	Sep. 2014	Hermon Chen	N/A
1.0	First SPEC. release.	Sep. 2014	Hermon Chen	N/A